ETIN80 — Algorithms in Signal Processors

Overview and Introduction

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January 20, 2014

Contact

- Weekly group discussions: day, time and location TBD.
  - Weekly discussions are for discussions and questions.
  - Problems will not be addressed outside the meeting times.
- Urgent problems and questions by e-mail.

What is a Signal Processor

- Programmable domain-specific computational unit.
    - real-time requirements
    - steam processing
    - high I/O demands
- Typical features are:
    - multiple memory banks and busses
    - multiply-accumulate
    - circular and bit-reversed addressing
    - word-oriented processing
    - single-cycle instructions
    - store-compute-load
    - separate program and data memory
    - separate data and address computation
    - zero-overhead loops
- Data driven design.

Were Are Signal Processors Used

- Multimedia applications.
  - portable audio devices
  - photo and video cameras
  - television, receivers and DVD/BD players
- Telecommunication.
  - cellular telephones
  - base stations
  - cable modems
- Automobile industry.
  - active suspension
  - engine control systems
  - anti-lock braking systems
  - electronic stability control
- Biometric and medical applications.
  - pacemaker

Signal Processor Data Types

- Integers.

b_7	b_6	b_5	b_4	b_3	b_2	b_1	b_0
-2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0 .

- Fixed point values.

b_7	b_6	b_5	b_4	b_3	b_2	b_1	b_0
-2^0 .	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}

- Floating point values.

s	e_7	e_6	$\cdots$	e_0	m_{22}	m_{21}	$\cdots$	m_0
$\{1,-1\}$	-2^7	2^5		2^0	2^{-1}	2^{-2}		2^{-23}

$$v = s \cdot (1 + m) \cdot 2^e$$

- Block-floating point buffers.

fixed point buffers with a common floating point

Signal Processor Data Types

- Full-precision multiplier.

  16 bit operands yield 32 bit product
- Extended-precision accumulator with guard-bits.

  32 bit product and 40 bit accumulator
- Guard-bits prevents saturation during accumulation.
- Saturation instead of overflow.

Signal Processor Modules

- Data processing unit for data calculation.
- Address generation unit for memory address calculation.
- I/O processor for specialized peripherals.
  - serial ports
  - DMA controller
  - timers
  - GPIO
  - clock generators

What a Signal Processor Isn’t

- Lower cost and more power efficient than general-purpose processors.
- Not a general-purpose processor.
  - low memory
  - no virtual memory
  - no memory protection
  - limited operating system
  - limited threading
  - limited run-time library

Hardware

- Analog Devices ADSP-21262 DSP.
  - 200 MHz maximum core
  - 2 MiB memory
  - 4 MiB non-volatile memory
  - 32 bit computational units
  - integer, fixed point and floating point
  - dual processing units
- Texas Instruments TLV320AIC32 audio codec.
  - 32 bit stereo codec
  - 8 kHz to 96 kHz sampling rate
  - line and microphone input
  - line and power output
- Four semi-independent audio codecs.
  - 8 input channels.
  - 8 output channels.

Hardware

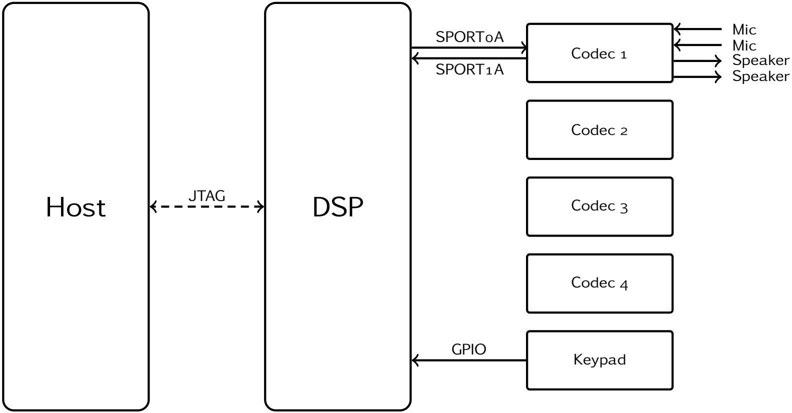
- Stereo input, configurable as line or microphone.
- Stereo output, configured as power output.
- A 4-key keypad.
- Framework to configure the DSP and the audio codecs.
- Feel free to modify the software and request other hardware configurations.

Equipment

- Hand held microphones.
- Microphone arrays.
- Headphones.
- Speakers.
- Schematics, PCB layout and manuals.

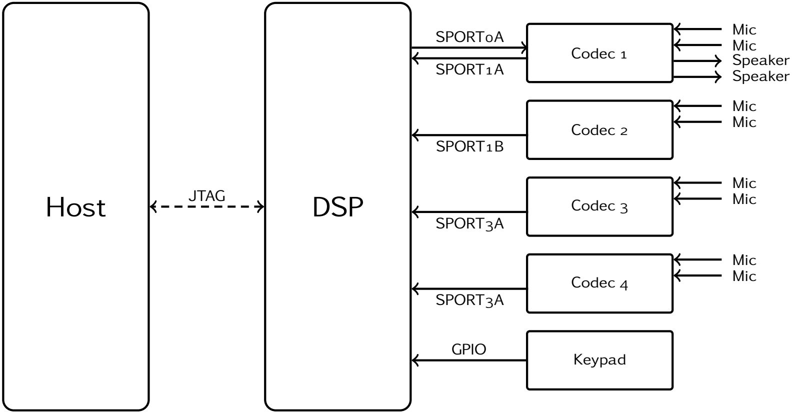
Configurations

Standard stereo configuration.



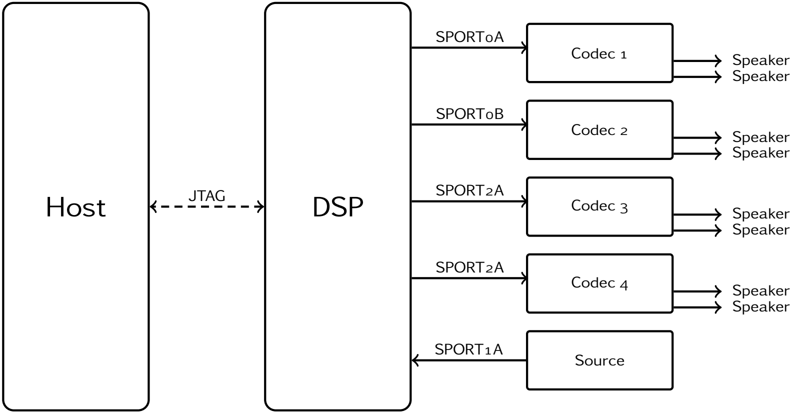
Configurations

Eight-channel beamformer.



Configurations

7.1 surround decoder.



Manuals

- Visual DSP++ 5.0 Run-Time Library Manual for SHARC Processors

  Reference manual for runtime library functions.

- ADSP-21160 SHARC DSP Instruction Set Reference

  Reference manual for the assembly language instruction set.

- ADSP-2126x SHARC Processor Hardware Reference

  Manual for the processor describing its internal structure, components and configuration registers.

- Low-Power Stereo Audio CODEC for Portable Audio/Telephony

  Manual for the audio codec describing its internal structure and configurations registers.

Signal Processing Example

$$\text{Calculate } y(n) = \sum_{k=0}^{K-1} x(n-k)h(k)$$

```
  ld i2, K
accumulate:
  mov [i0], r0;       (1)
  mov [i1], r1;       (1)
  mpy r0, r1, r1;     (2)
  add r1, r2, r2;     (3)
  inc i0;             (4)
  inc i1;             (4)
  dec i2;             (5)
  tst i1;             (5)
  jnz accumulate;     (5)
```

- General purpose processor:
  - load sample values (1)
  - multiply (2)
  - accumulate (3)
  - advance pointers (4)
  - loop control (5)

Signal Processing Example

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```
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accumulate:
  mov [i0], r0;      (1)
  mov [i1], r1;      (1)
  mpy r0, r1, r1;    (2)
  add r1, r2, r2;    (3)
  inc i0;            (4)
  inc i1;            (4)
  dec i2;            (5)
  tst i1;            (5)
  jnz accumulate;    (5)
```

- Signal processor:
  - multiply-accumulate fuses (2) and (3)
  - parallel data-address computations fuses (1) and (4)
  - parallel compute-load fuses (1)–(4)
  - zero-overhead loops eliminates (5)