Backend Tools

Place and Route
changes for ST65nm CMOS

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Design Kit Path

- Design kit root dir:
  /usr/local-eit/cad2/cmpstm/stm065v536
- 2 Process options, 3 Threshold Voltage (VT) options:
  - LP (Low Power) – Low Power Low Speed
  - GP (General Purpose) – High Power High Speed
  - High Threshold Voltage (HVT) – Lowest Power and Lowest Speed
  - Standard Threshold Voltage (HVT) – Medium Power and Medium Speed
  - Low Threshold Voltage (HVT) – High Power and High Speed
- Process option and Threshold Voltage combined yields 6 possibilites
  - GPLVT
  - GPSVT
  - GPHVT
  - LPLVT
  - LPSVT
  - LPHVT

Increasing speed
Increasing power

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Cell Libraries

- Clock cells, Core Cells, I/O Cells, Place & Route Cells are separated:
- Clock dir: DESIGN_KIT_ROOT/CLOCK65<ProcessVToption>_3.1 – Clock buffer & Inverter
- Core dir: DESIGN_KIT_ROOT/CORE65<ProcessVToption>_5.1 – Logical and arithmetic gates, registers, e.g., NAND, NOR, XOR, DFF …
- I/O dir: DESIGN_KIT_ROOT/IO65LPHVT_SF_1V8_50A_7M4X0Y2Z_7.0 – Signal Pads, Core supply pads
- I/O dir: DESIGN_KIT_ROOT/IO65LP_SF_BASIC_50A_ST_7M4X0Y2Z_7.2 – I/O Fillers, Corner Pads, Supply for Pad Ring
- Place & Route dir: DESIGN_KIT_ROOT/PRHS65_7.0.a – Well Taps, I/O Filler, Fillers, De-coupling capacitors

- Use LPHVT for lowest power.

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Cell Libraries cont'd

- Cell library directory structure:
  - behaviour – Behavioural model for logic gates
  - CADENCE/LEF – Physical information for Place & Route
  - doc – Documentation of cells in library
  - libs – Timing information for Synthesis, Place & Route

- Variation key for timing libraries
  - <LibraryName>65<ProcessVToption>_<corner>_<Voltage>_<temperature>_<age>.lib
  - LibraryName: CORE, CLOCK
  - ProcessVToption: LPHVT, LPSVT, LPLVT, GPHVT, GPSVT, GPLVT (use same for all libraries)
  - Corners: Worst Case (wc), nominal (nom), Best Case (bc),
  - Voltage: 0.90V (wc) – 1.30V (bc)
  - Temperature: -40°C (m40C) to 125°C (125C)
  - Age: 10 years aging (10y)
  - CORE65LPHVT_wc_1.05V_m40C_10y.lib

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Import Design

- LEF Files:
  - DESIGN_KIT_ROOT/EncounterTechnoKit_cmos065_7m4x0y2z_AP@5.3.1/TECH/cmos065_7m4x0y2z_AP_Worst.lef - Header LEF
  - CORE65<ProcessVToption>_5.1/CADENCE/LEF/CORE65<ProcessVToption>_soc.lef
  - CLOCK65<ProcessVToption>_3.1/CADENCE/LEF/CLOCK65<ProcessVToption>_soc.lef
  - PRHS65_7.0.a/CADENCE/LEF/PRHS65_soc.lef
  - IO65LPHVT_SF_1V8_50A_7M4X0Y2Z_7.0/CADENCE/LEF/IO65LPHVT_SF_1V8_50A_7M4X0Y2Z_soc.lef
  - IO65LP_SF_BASIC_50A_ST_7M4X0Y2Z_7.2/CADENCE/LEF/IO65LP_SF_BASIC_50A_ST_7M4X0Y2Z_soc.lef

- Libraries to use for MMMC analysis:
  - Pick a combination of a wc and bc library e.g.,
  - SS – wc, 1.05V, m40C, 10y
  - FF – bc, 1.25V, 125C

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Import Design

- In Slide 10 also add a Cap Table and QRC Technology file:
  - Cap Table: DESIGN_KIT_ROOT/ EncounterTechnoKit_cmos065_7m4x0y2z_AP@5.3.1/TECH/ cmos065_7m4x0y2z_AP_<Worst/Best>.captable
  - QRC Tech File: /usr/local-eit/cad2/cmpstm/stm065v536/ SignOffTechnoKit_cmos065lp_7m4x0y2z@5.3.4/etc/QrcTechLibs/RC<MIN/MAX>/ qrcTechFile

Changes during Place & Route

- Global Net Connect:
  - Use Pin “vdd” and “gnd” instead of VCC and GND.
- Place Well Taps:
  - Use Welltap cell: HS65_LH_FILLERNPWPFP4
- Design Clock:
  - Mark all Clock Network buffers, inverters:
    - » HS65_LH_CNBF*, HS65_LH_CNIV*
  - Avoid regular inverters and buffers (HS65_LH_IV*, HS65_LH_BF*)
  - Also avoid special clock buffers (HS65_LH_BFX38_*)

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Changes during Place & Route cont'd

- I/O Filler cells:
  - Use IOFILLER<1, 2, 4, 8, 16, 32, 64>_ST_SF_LIN
- Filler cells:
  - Use FILLERPFOP<8, 9, 12, 16, 32, 64>
  - And HS65_L(H|S|L)_FILLERPFP<1-4>

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