



LUND
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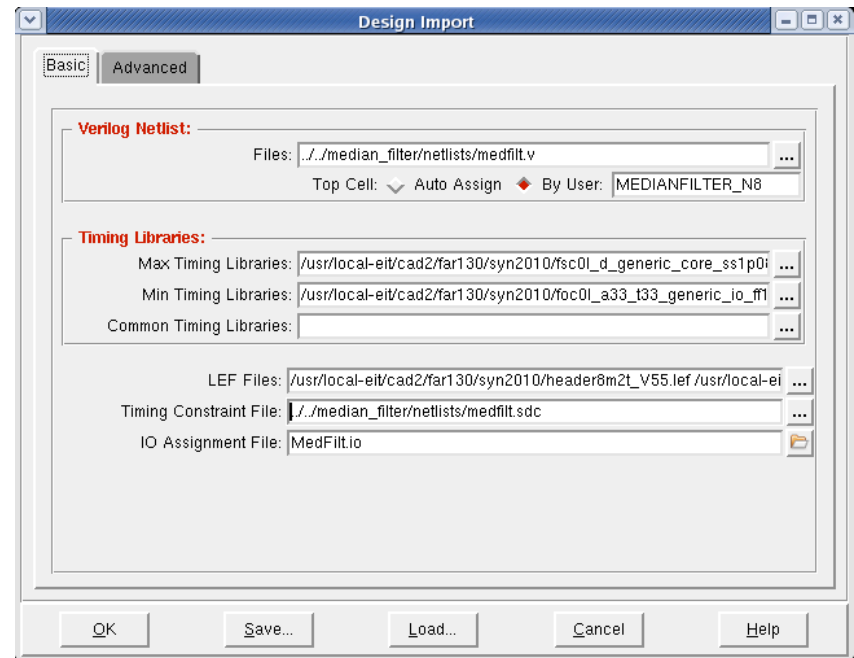
Backend Tools

Place and Route

Oskar Andersson

Load Design

- Design -> Import Design
- Specify Netlist, Timing libraries, LEF files, Timing constraints, IO file
- Max timing = worst case (slowest)
- Min timing = best case (fastest)



Load Design

- Folder for backend files:
 - /usr/local-eit/cad2/far130/syn2010/
- Libs:
 - fsc0l_d_generic_core_xx.lib
 - foc0l_a33_t33_generic_io_xx.lib
- MAX-timing = worst timing =>
 - ss1p08v125c (slow-slow) (1.08V) (125 °C)
- Min-Timing = best timing =>
 - ff1p32vm40c (fast-fast) (1.32V) (- 40°C)



Load Design

- Folder for backend files:
 - /usr/local-eit/cad2/far130/syn2010/
- LEFs:
 - header8m2t_V55.lef
 - fsc0l_d_generic_core.lef
 - FSC0L_D_GENERIC_ANT_V55.8m2t.lef
 - foc0l_a33_t33_generic_io.8m2t.lef
 - FOC0L_A33_T33_GENERIC_IO_ANT_V55.8m2t.lef



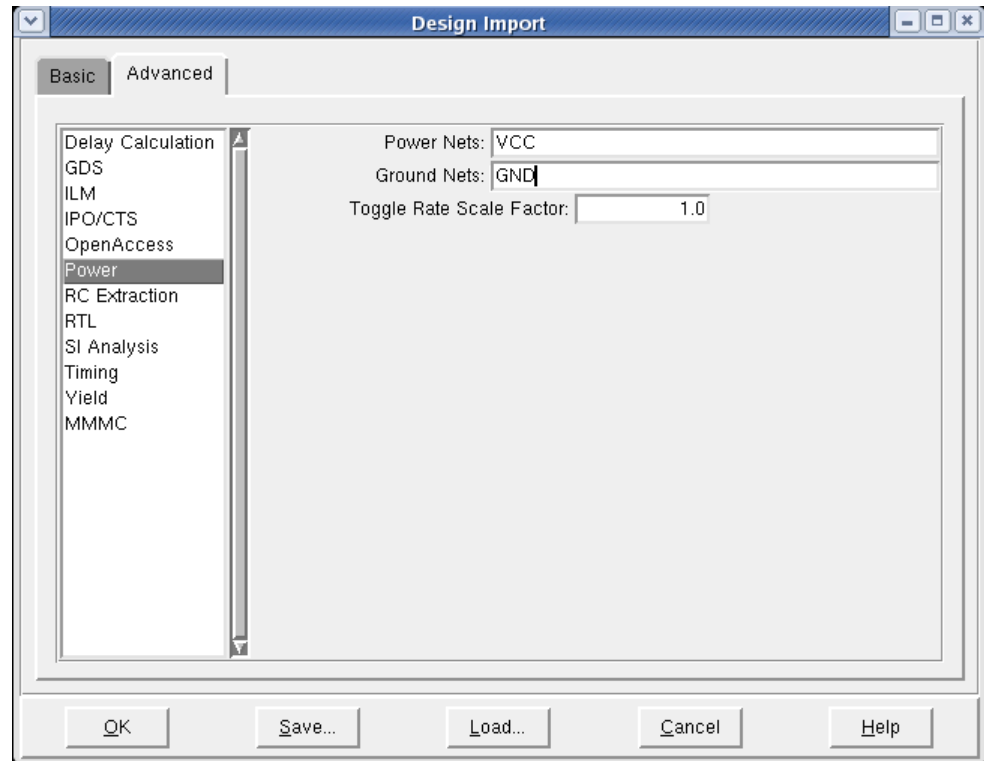
Load Design - Memories

- Libs and Lef in mem.tar.gz



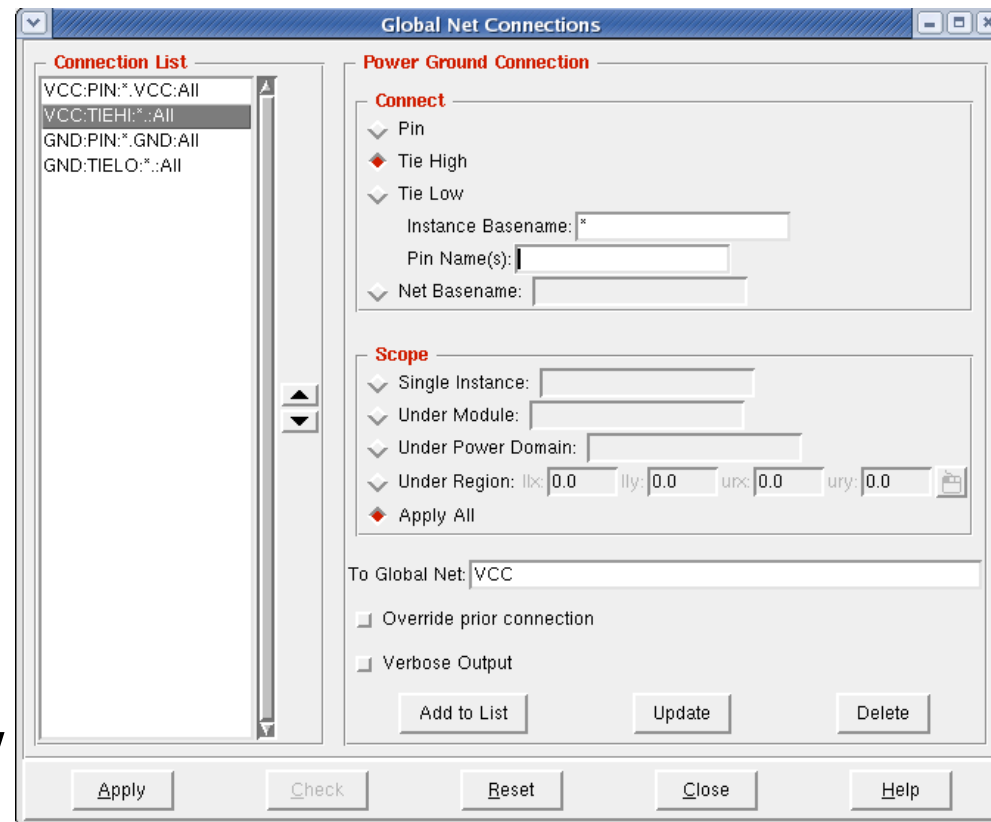
Load Design – Power networks

- Choose Advanced Tab:
 - Add power nets call them something like:
VCC & GND

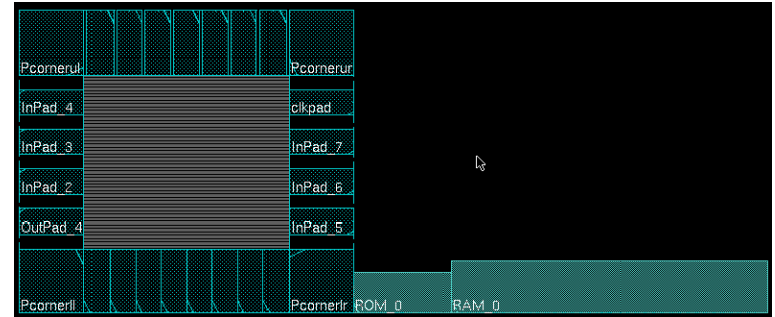


Global Net Connect

- To connect the power networks:
Floorplan ->
Connect Global Nets...
- Two types: Pin & TieHi/Low
- Power network, e.g., VCC connect to TIEHI, Pin VCC.
- Ground network, e.g., GND connects to TIELO, Pin GND.
- Scope: Apply All



Floorplan



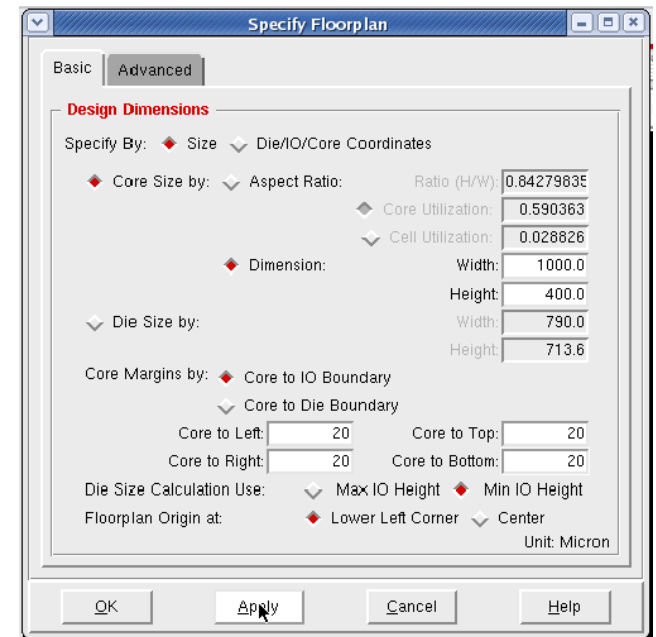
- Resize floorplan to fit memories
- Floorplan -> Specify Floorplan

- The size of memories can be measured with the ruler tool. 


- To zoom use the zoom buttons:

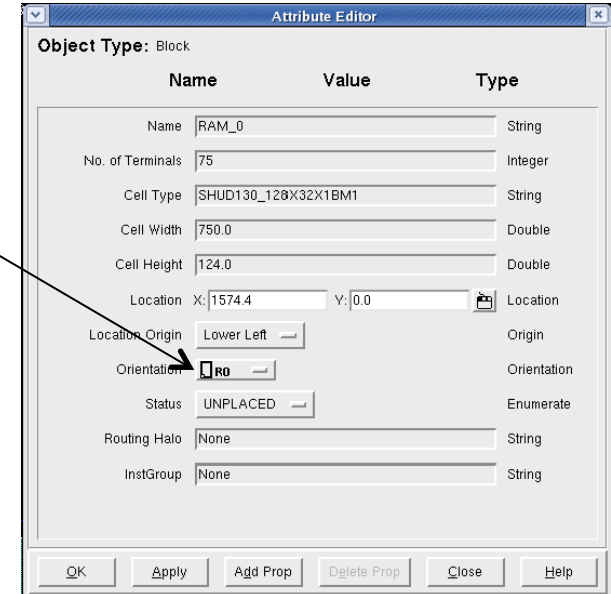
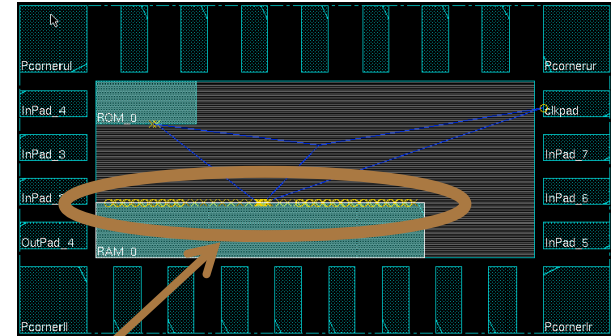


- Zoom in (z), Zoom out (shift+z), Fit to screen (f),



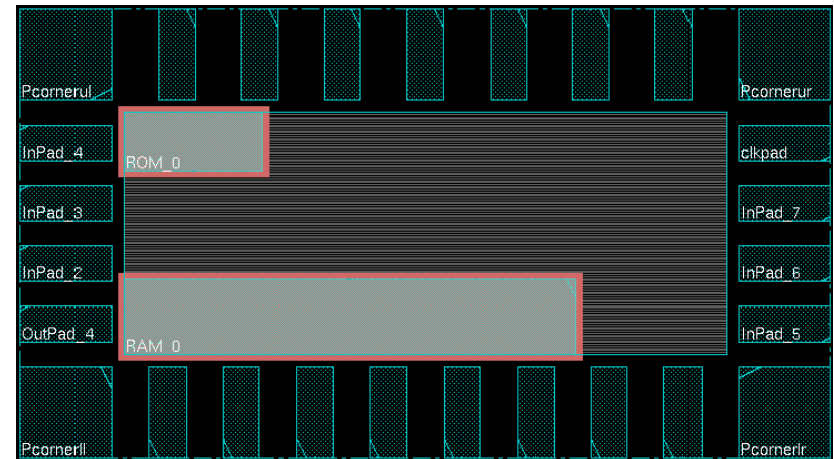
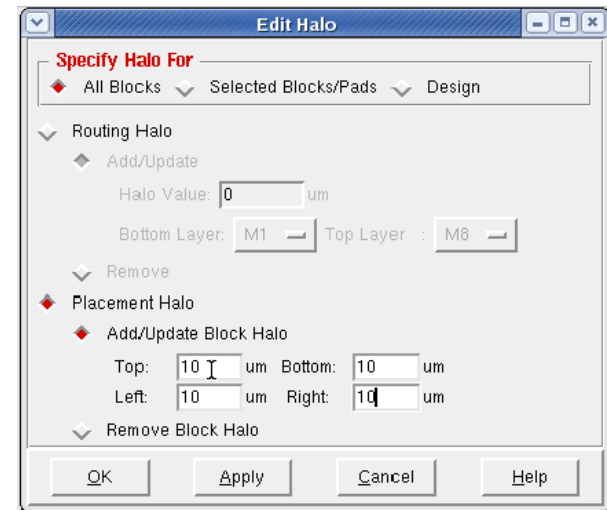
Place and rotate memories

- Move memories by selecting movement tool  or press "Shift+R".
- Need to rotate memories to have pin connections inside the core.
- Rotate memories by edit properties for selected object by pressing "q".
- Orientation set to **R180** for 180 degree rotation.



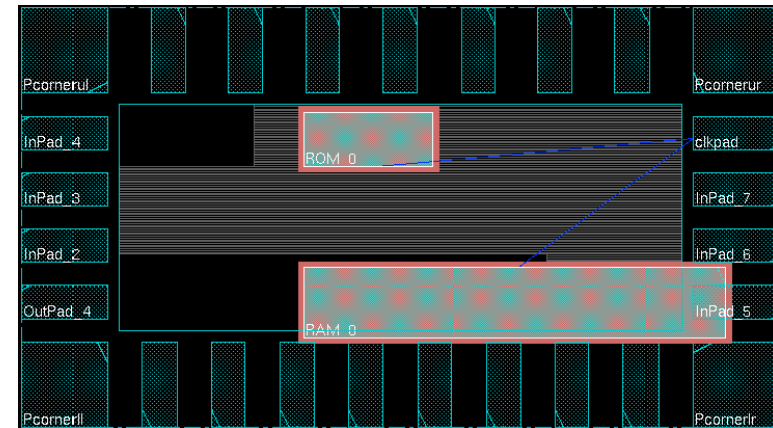
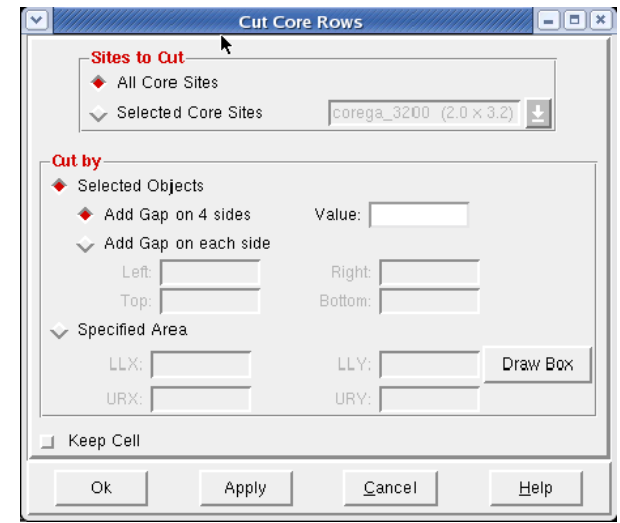
Add Halo

- Floorplan -> Edit Floorplan -> Edit Halo
- To create a ring around the memory macro, where no standard cells can be placed.
- Routing is still possible
- Be sure to specify a distance, e.g. 10 μm .



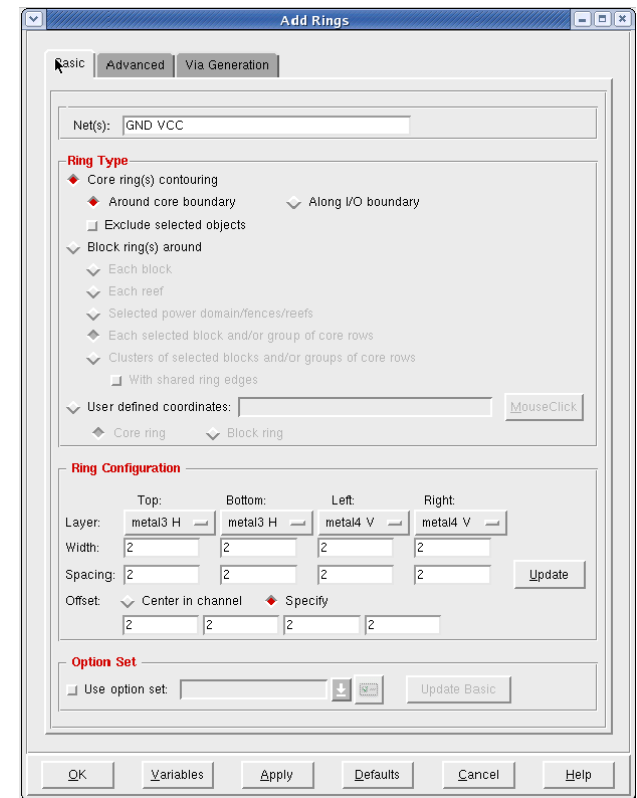
Cut Rows

- Floorplan -> Edit Floorplan -> Core Row -> Cut
- Deletes core rows beneath memories.
- By moving memories, the cut rows are shown.
- Now is a good time to save the design:
Design -> Save Design As -> SoCE
- To restore:
Design -> Restore Design -> SoCE



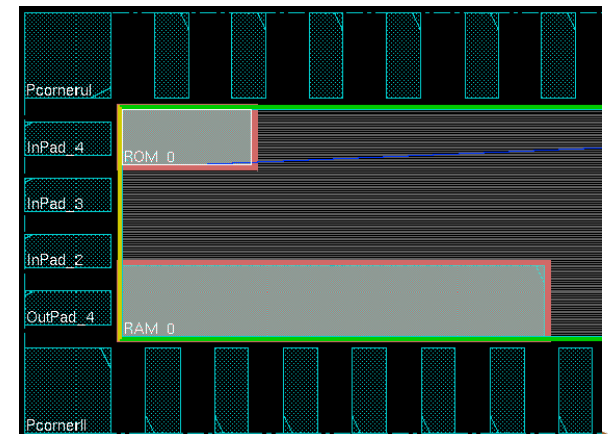
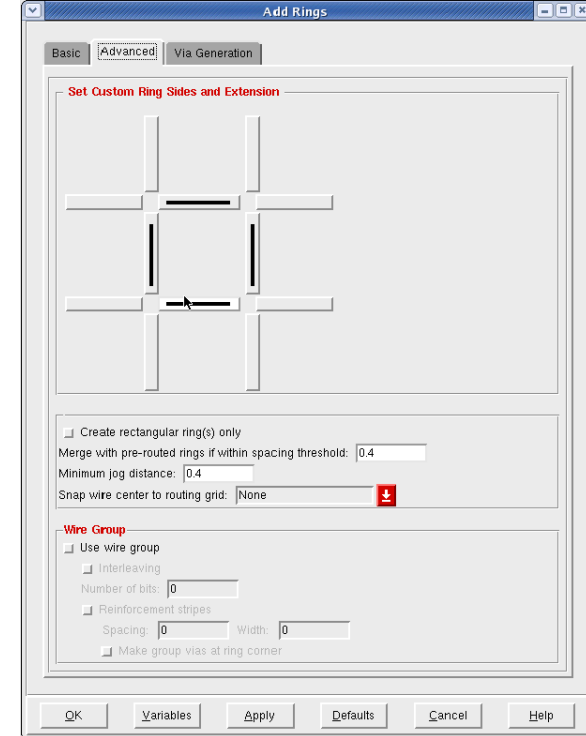
Power rings

- Power -> Power Planning -> Add Rings
- To add Power rings around core specify Width: 2, Spacing: 2, Offset 2.
- Use metal3 for Horizontal wires and metal4 for Vertical wires.



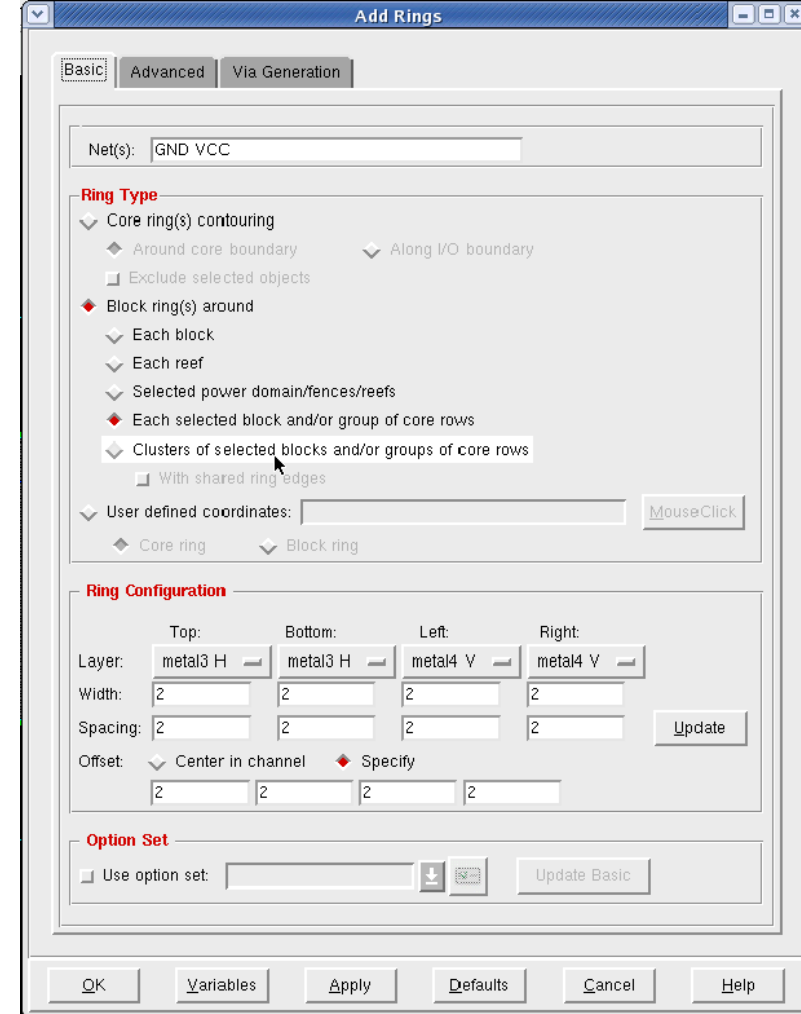
Power rings

- Make sure that an entire ring is visible under the advanced tab.
- If applied correctly your design should look like this.



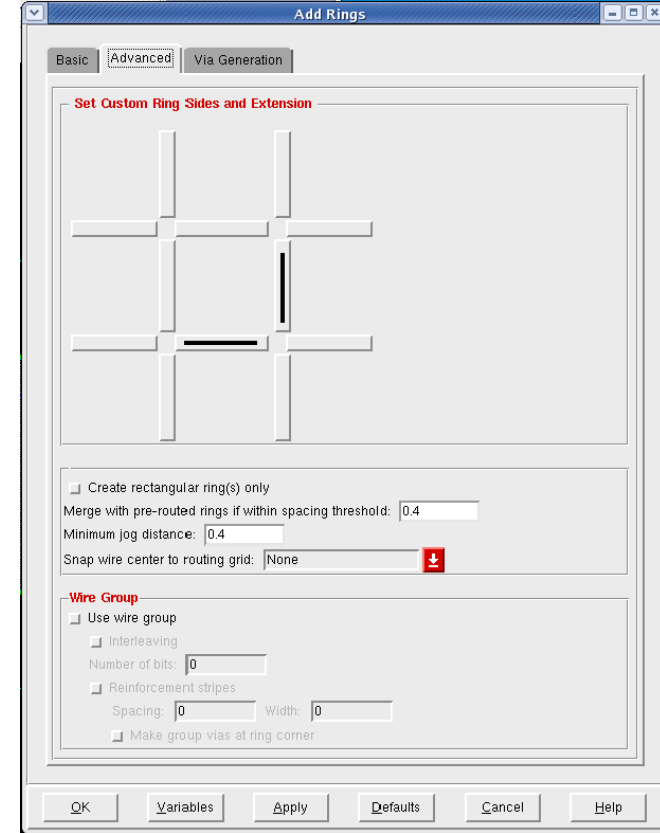
Power rings

- Select the memory macros and select as in the figure.
- This will create a core ring around the memory block
- If memories are placed in corners the layout of power power rings can be changed according to figure on next slide.



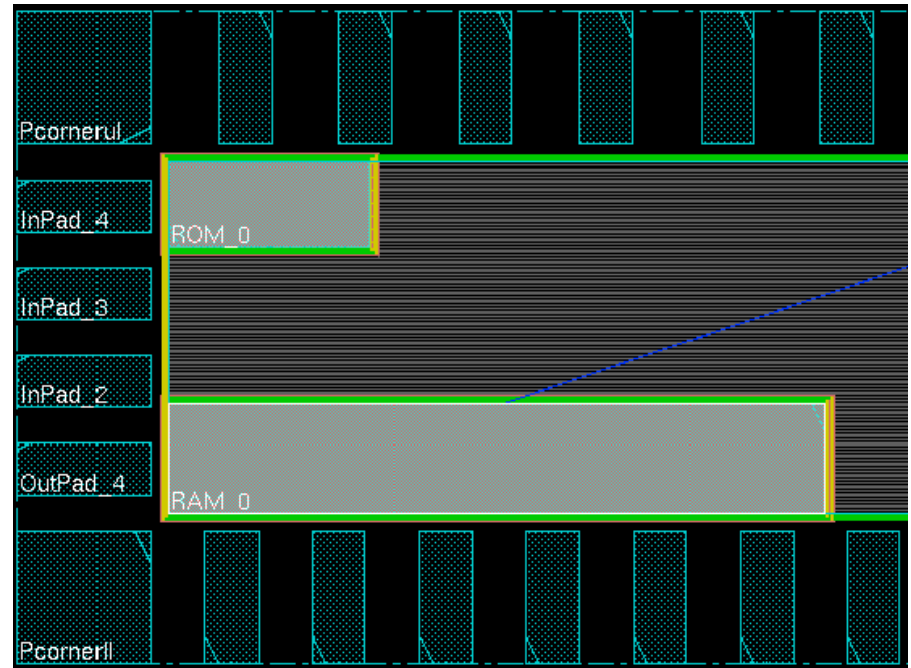
Power rings

- For the upper memory no extra power routes are necessary for the top and left sides.



Power rings

- If successful the design should look like the picture.
- If not, type the command: "deleteAllPowerPreroutes", use Tab key to autocomplete.
- This command clears all power routing.

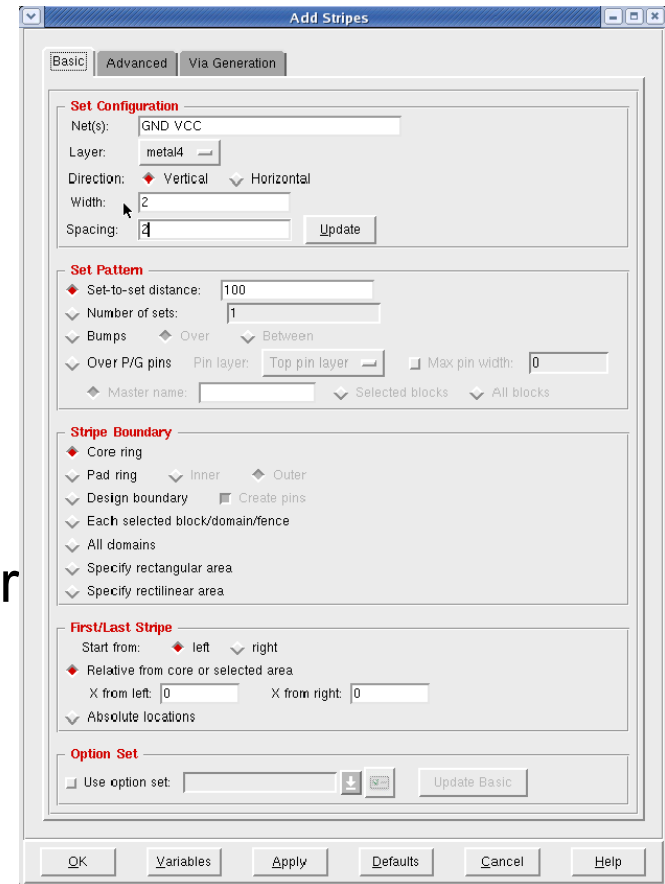
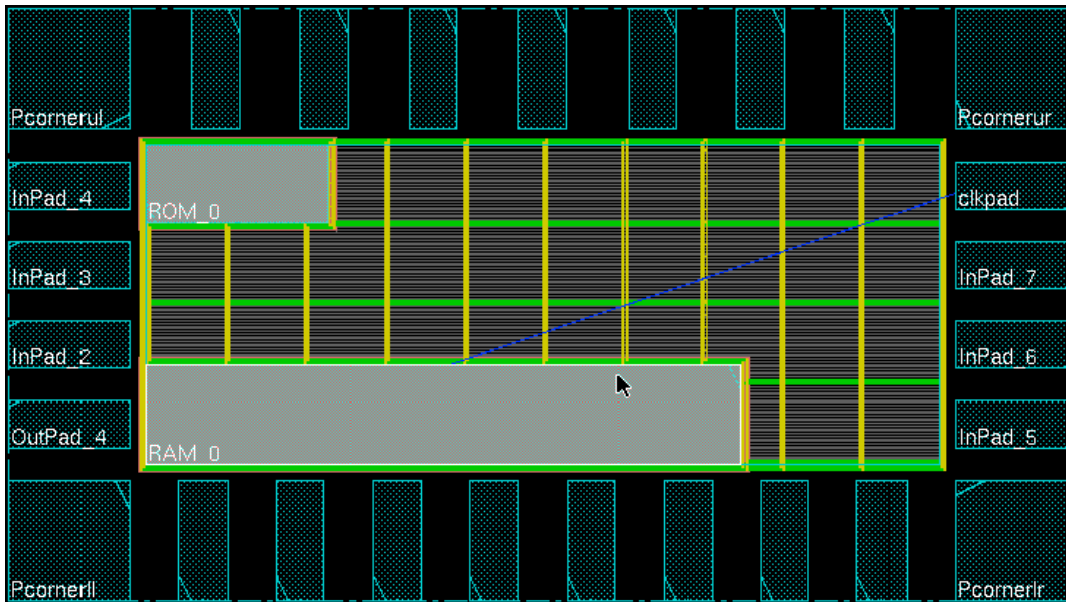


```
eit-oea@ylva:~/test/soc
File Edit View Terminal Tabs Help
deleteFPObject          deleteSdpObject
deleteFiller           deleteSelectedFromFPPlan
deleteHaloFromBlock    deleteShield
deleteInst             deleteSpareModule
deleteInstFromInstGroup deleteTSV
deleteInstGroup        deleteTieHiLo
deleteInstPad          deleteWhatIfTimingAssertions
deleteIoFiller         delete_path_category
deleteIoInstance
deleteIoRowFiller
velocity 3> deleteAll
deleteAllCellPad      deleteAllPtnCuts
deleteAllDensityAreas deleteAllPtnFeedthroughs
deleteAllFPObjects    deleteAllRouteBlks
deleteAllInstGroups   deleteAllScanCells
deleteAllMsConstraints deleteAllSignalPreroutes
deleteAllPartitions
deleteAllPowerPreroutes
velocity 3> deleteAllPowerPreroutes
```



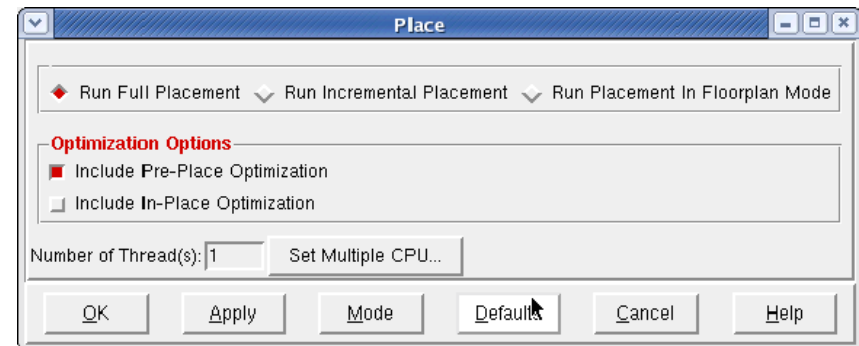
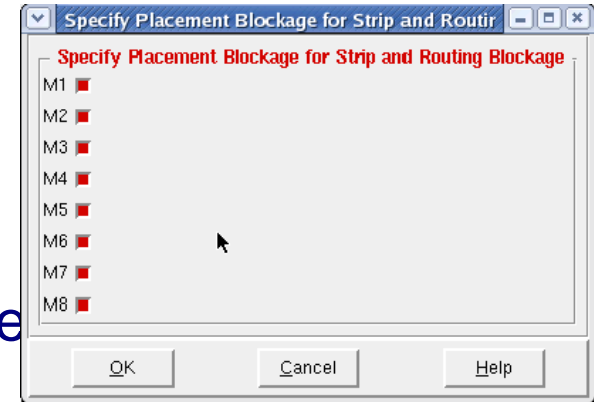
Power stripes

- Power -> Power Planning -> Add Stripes
- Select metal4 for vertical and metal3 for horizontal



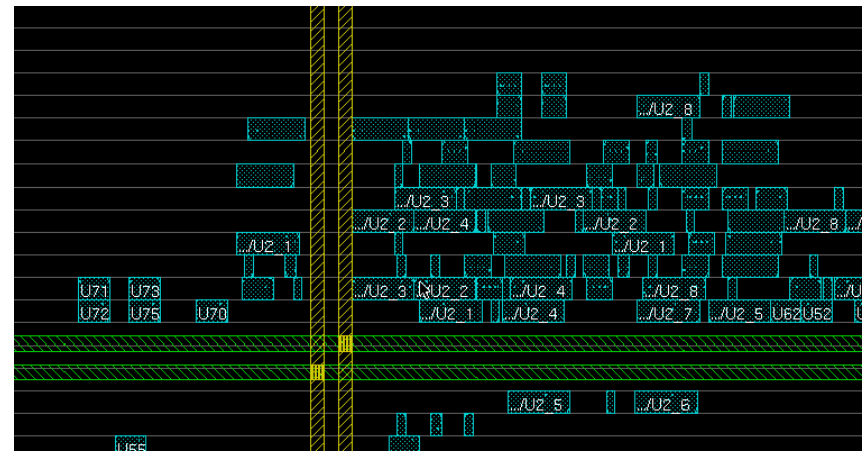
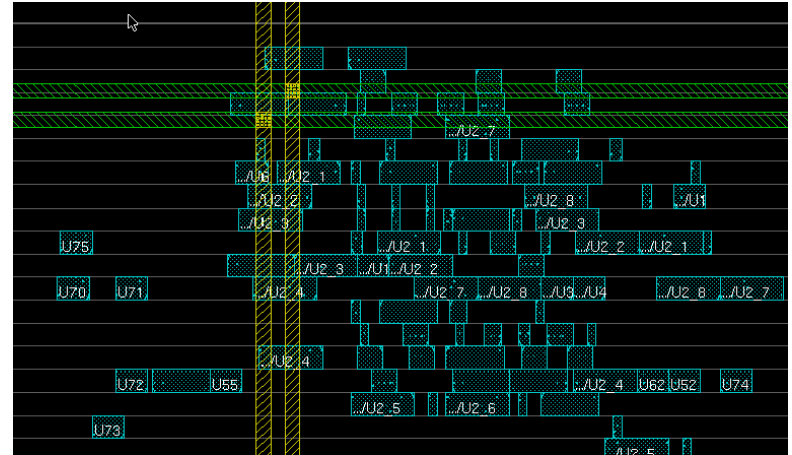
Place standard cells

- Place -> Specify -> Placement Blockage
- Place -> Standard cells
- Change to physical view to see placed cells:



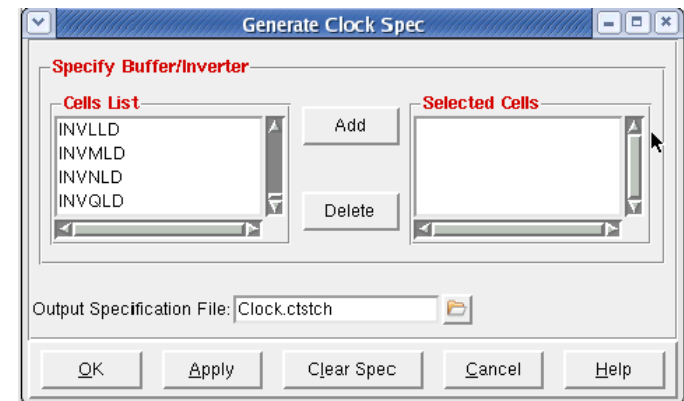
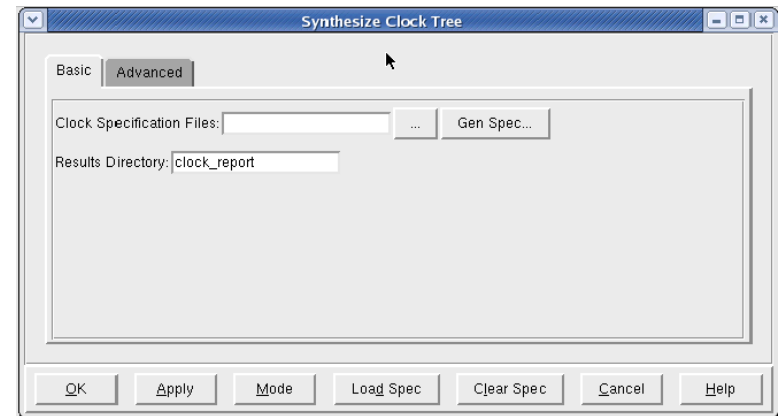
Place standard cells

- Avoids placement underneath power stripes



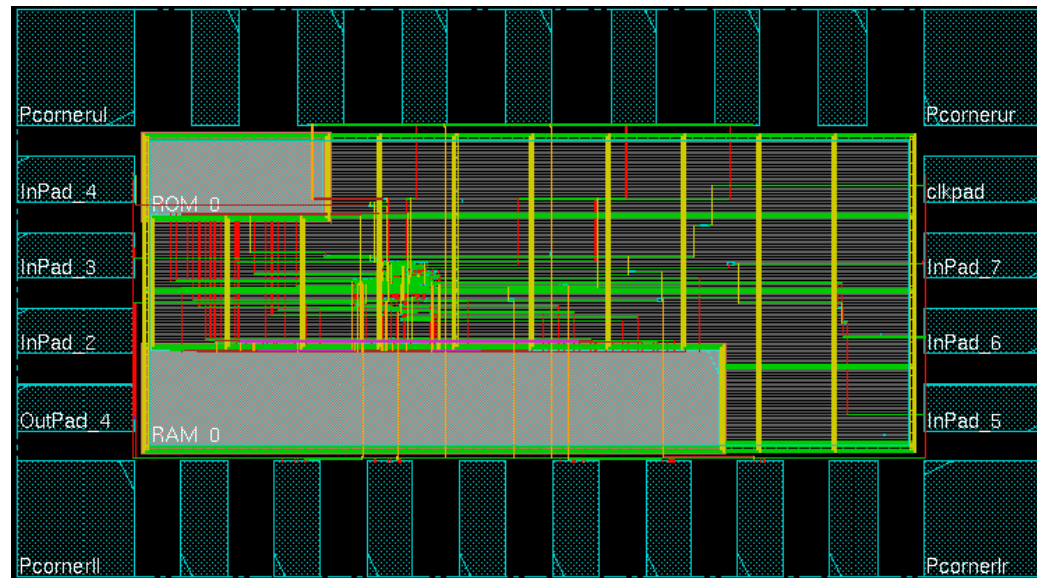
Design Clock

- Clock -> Design Clock
- Click on Gen Spec and add all cells
- Second time use the (...) button to open your .CTSTCH file.



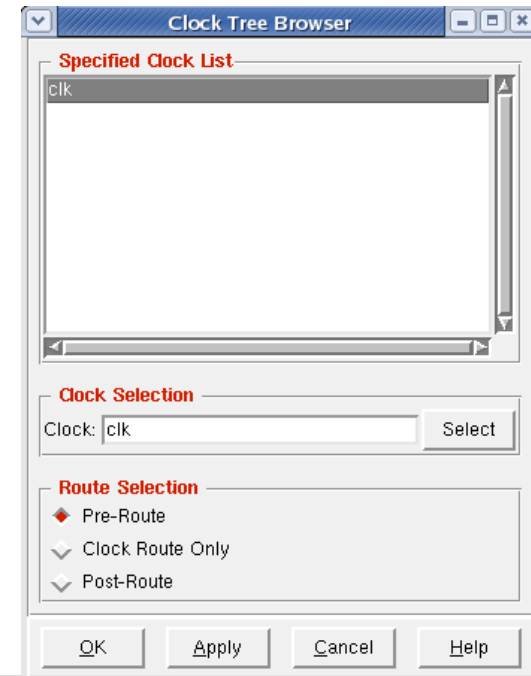
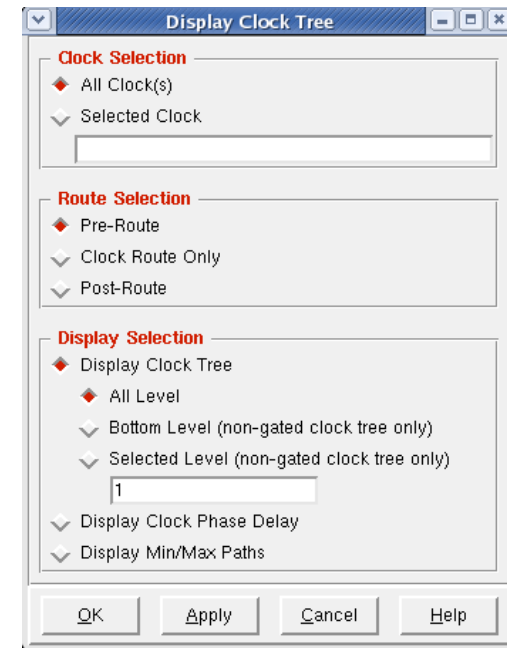
Design Clock

- Shows the designed clock including a trial route.
- Type "deleteTrialRoute" to delete this.



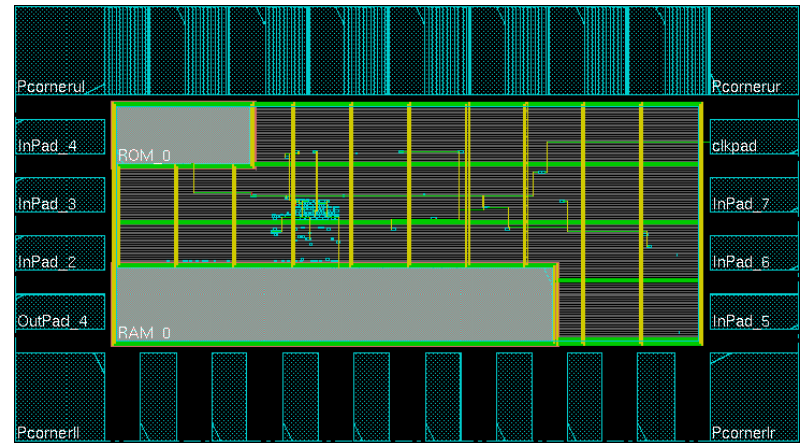
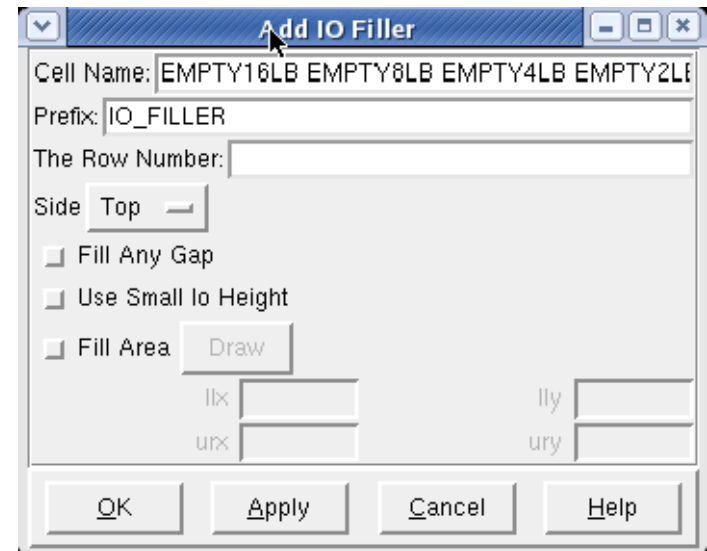
Design Clock

- It is possible to highlight the clock tree:
Clock -> Display -> Display Clock Tree...
- Choose all clocks and All Level
- Clear it with
Clock -> Display -> Clear Clock Tree Display.
- Clock tree Browser is shown from:
Clock -> Clock Tree Browser



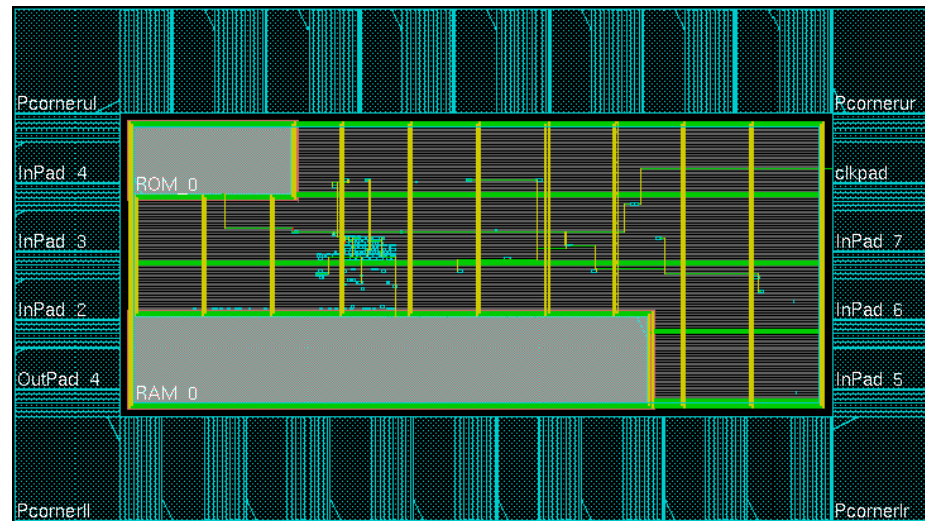
IO Filler cells

- Place -> Physical Cells -> Add IO Filler
- Cells are named:
EMPTY16LB EMPTY8LB
EMPTY4LB EMPTY2LB
EMPTY1LB
- Tick Fill Any Gap
- Select which side to add to,
add to all sides.



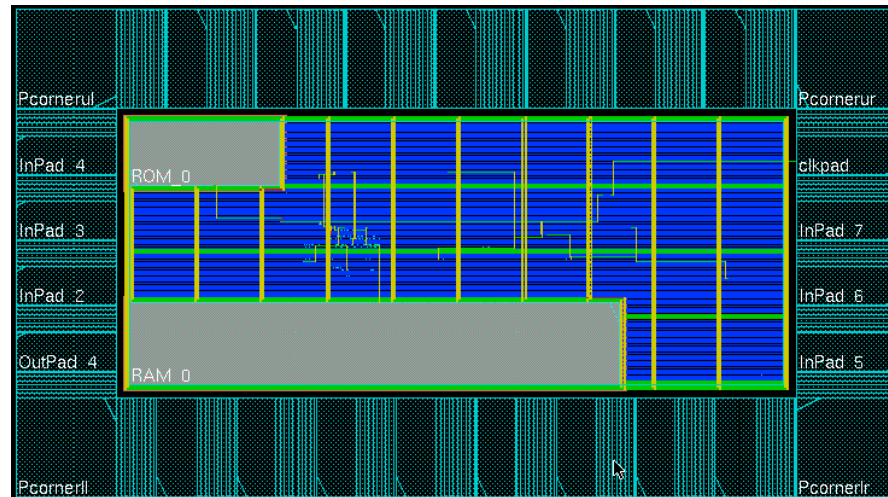
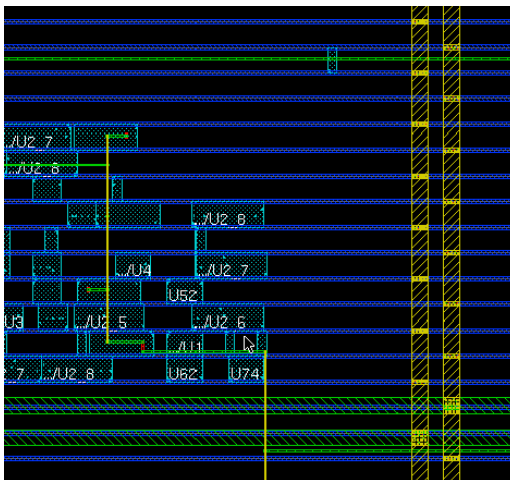
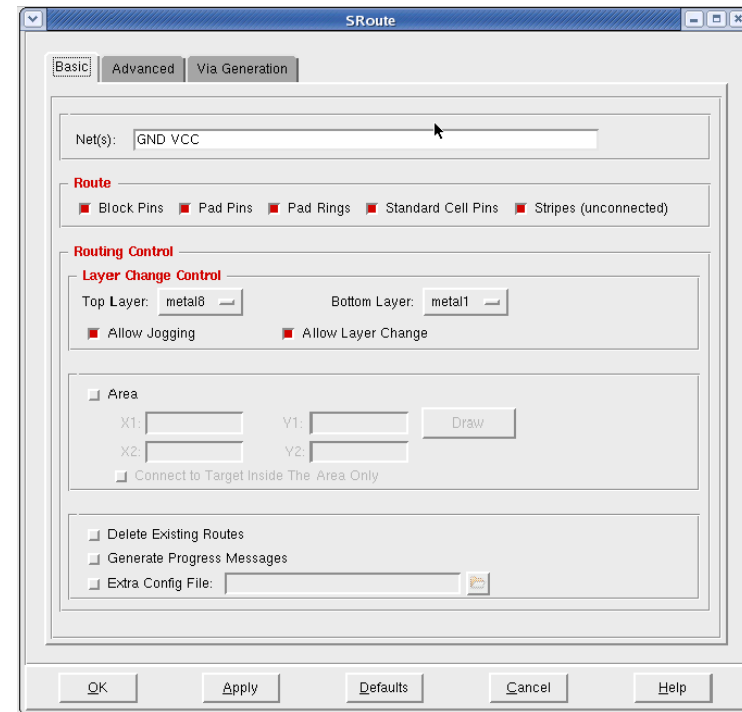
IO Filler cells

- If successful design should look as in picture.



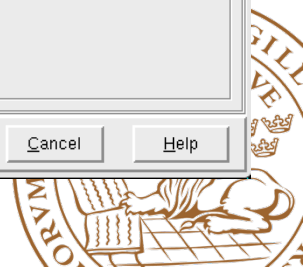
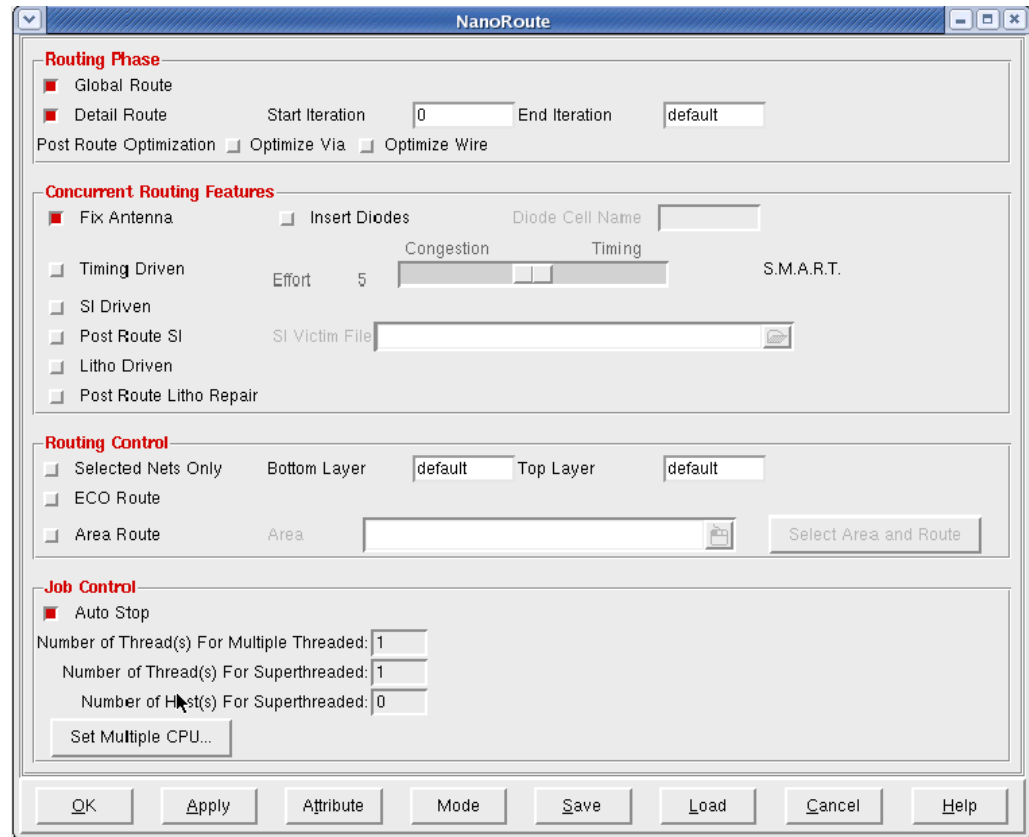
Special Route

- Route -> Special Route
- Routes GND and VCC net for powering of standard cells.



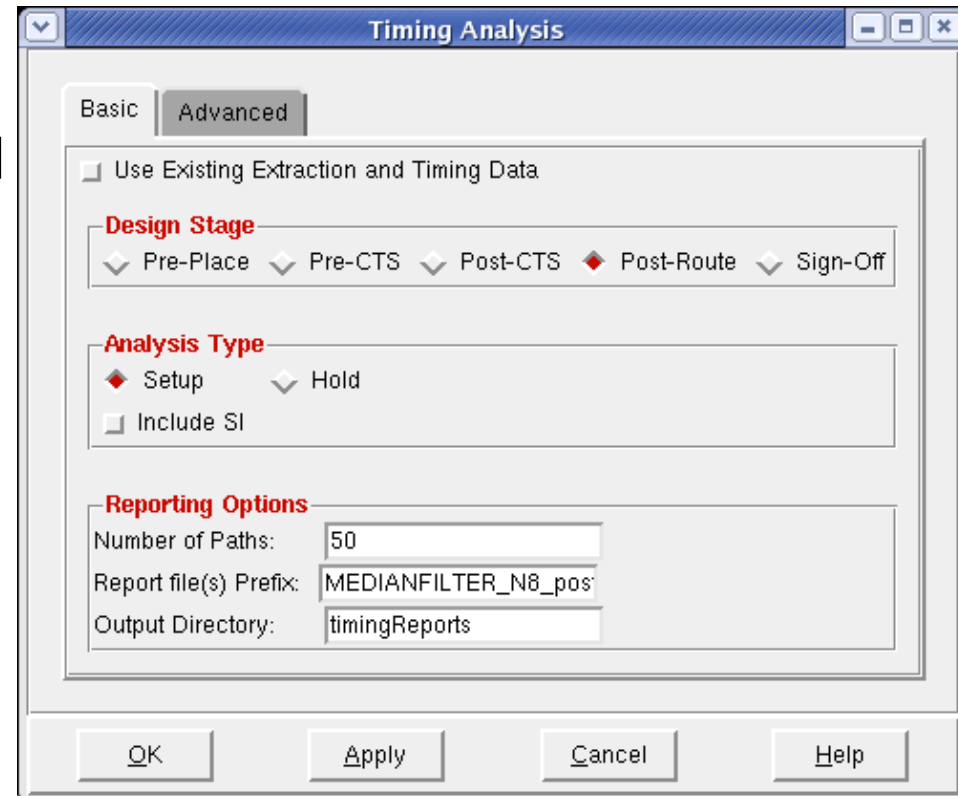
Route normal nets

- Route -> Nanoroute -> Route
- Run with default options.



Analyze Timing

- Before adding fillers we need to make sure that we meet timing, both setup and hold.
- **Timing -> Analyze Timing**
- Choose which design stage we are in, at this point Post-Route.
- Select both Setup and Hold, one after each other.



Analyze Timing cont'd

- Make sure that we have no setup nor hold violations.
- WNS stands for Worst Negative Slack
- TNS stands for Total Negative Slack.
- If we do we need to run optimize timing, to solve this issue.

optDesign Final Summary

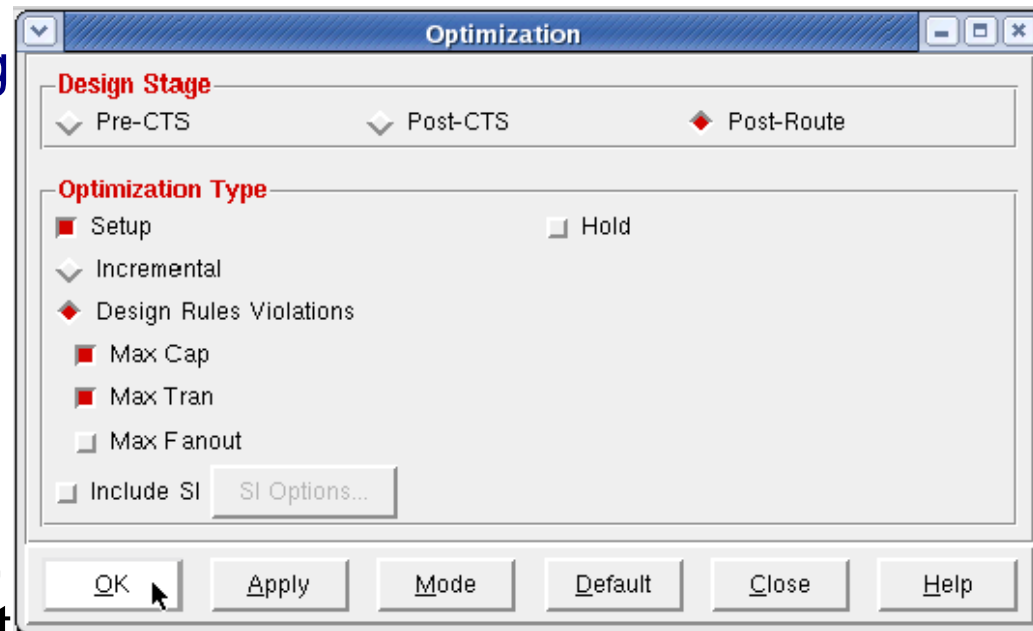
Setup mode	all	reg2reg	in2reg	reg2out	in2out	clkgate
WNS (ns):	5.242	5.242	15.707	N/A	N/A	N/A
TNS (ns):	0.000	0.000	0.000	N/A	N/A	N/A
Violating Paths:	0	0	0	N/A	N/A	N/A
All Paths:	83	75	8	N/A	N/A	N/A

Hold mode	all	reg2reg	in2reg	reg2out	in2out	clkgate
WNS (ns):	-0.019	-0.019	0.074	N/A	N/A	N/A
TNS (ns):	-0.041	-0.041	0.000	N/A	N/A	N/A
Violating Paths:	4	4	0	N/A	N/A	N/A
All Paths:	83	75	8	N/A	N/A	N/A



Fix Timing Violations

- Timing -> Optimize Timing
- Select your design stage, Post-Route.
- Select which violation you which to fix, such as Hold.
- Make sure to fix Max Cap, Max Tran and Max Fanout as well.
- Do not run all things at once.



Fix Timing Violations cont'd

- Make sure that all violations are fixed.
- If not re-run optimize timing, and select the method to fix.
- If running only setup time make sure to run analyze timing for hold violations afterwards.

optDesign Final Summary

Setup mode	all	reg2reg	in2reg	reg2out	in2out	clkgate
WNS (ns):	5.049	5.049	15.699	N/A	N/A	N/A
TNS (ns):	0.000	0.000	0.000	N/A	N/A	N/A
Violating Paths:	0	0	0	N/A	N/A	N/A
All Paths:	83	75	8	N/A	N/A	N/A

Hold mode	all	reg2reg	in2reg	reg2out	in2out	clkgate
WNS (ns):	0.008	0.008	0.077	N/A	N/A	N/A
TNS (ns):	0.000	0.000	0.000	N/A	N/A	N/A
Violating Paths:	0	0	0	N/A	N/A	N/A
All Paths:	83	75	8	N/A	N/A	N/A



Fix Timing Violations cont'd

- If no reg2out, in2reg paths are found, input delay and/or output delay are missing.
- See synthesis slides.

optDesign Final Summary

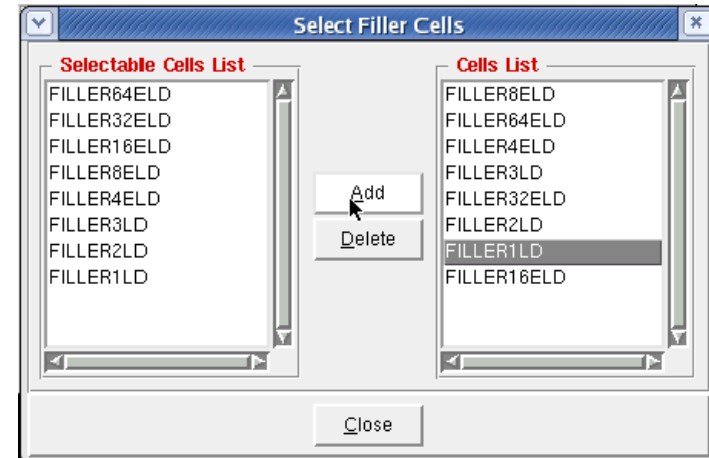
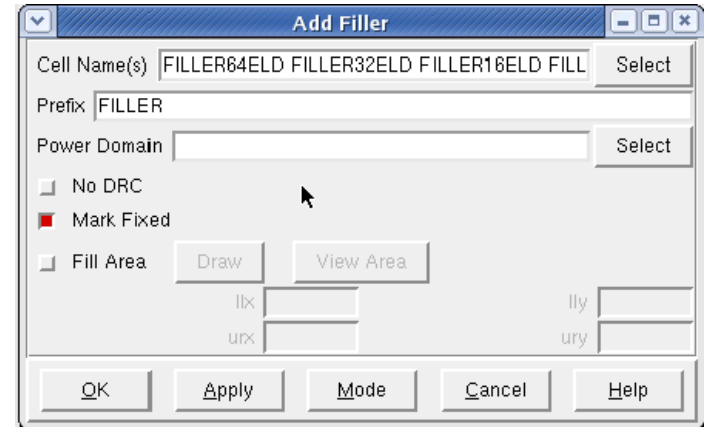
Setup mode	all	reg2reg	in2reg	reg2out	in2out	clkgate
WNS (ns):	5.049	5.049	15.699	N/A	N/A	N/A
TNS (ns):	0.000	0.000	0.000	N/A	N/A	N/A
Violating Paths:	0	0	0	N/A	N/A	N/A
All Paths:	83	75	8	N/A	N/A	N/A

Hold mode	all	reg2reg	in2reg	reg2out	in2out	clkgate
WNS (ns):	0.008	0.008	0.077	N/A	N/A	N/A
TNS (ns):	0.000	0.000	0.000	N/A	N/A	N/A
Violating Paths:	0	0	0	N/A	N/A	N/A
All Paths:	83	75	8	N/A	N/A	N/A



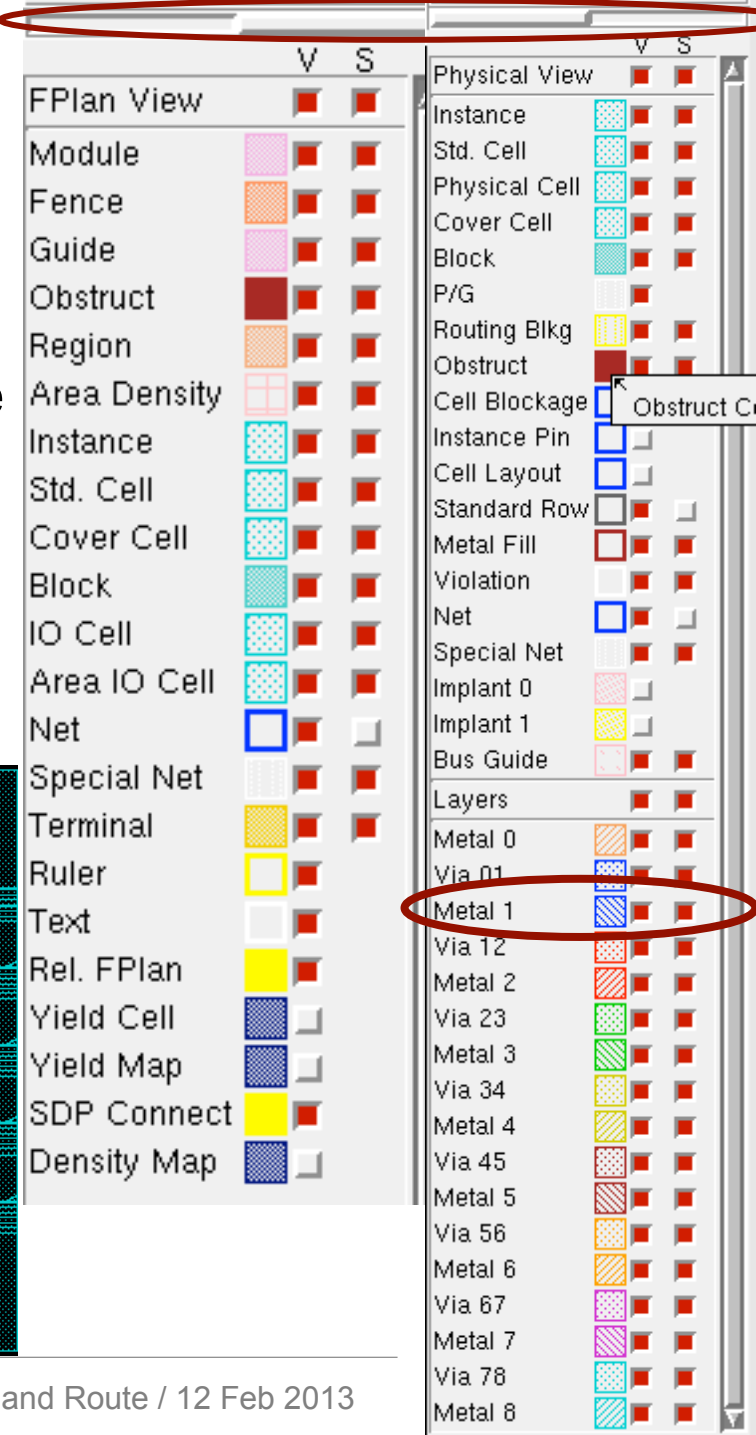
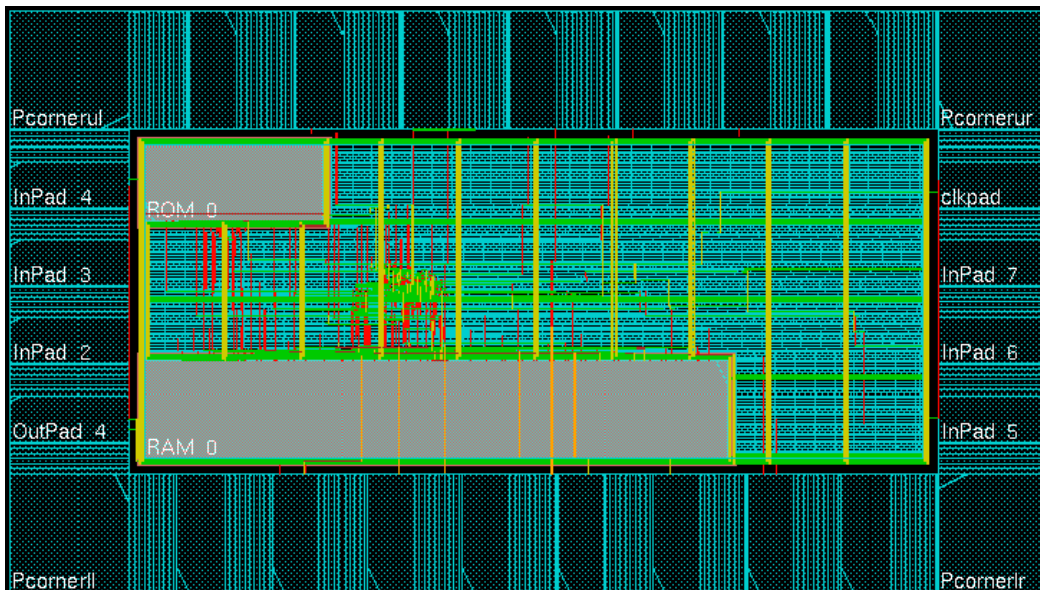
Add Filler cells

- Place -> Physical Cells -> Add Filler.
- Be sure to select the largest fillers first to use them when possible



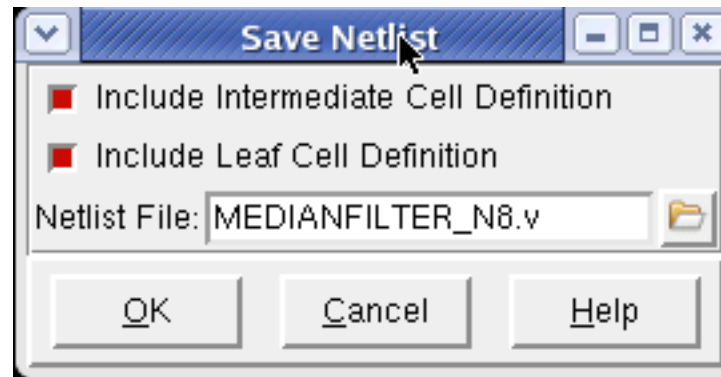
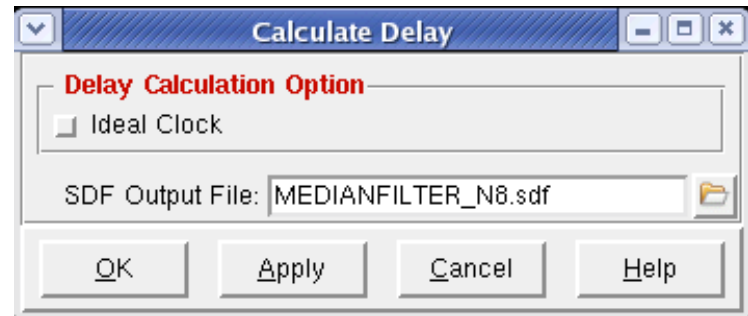
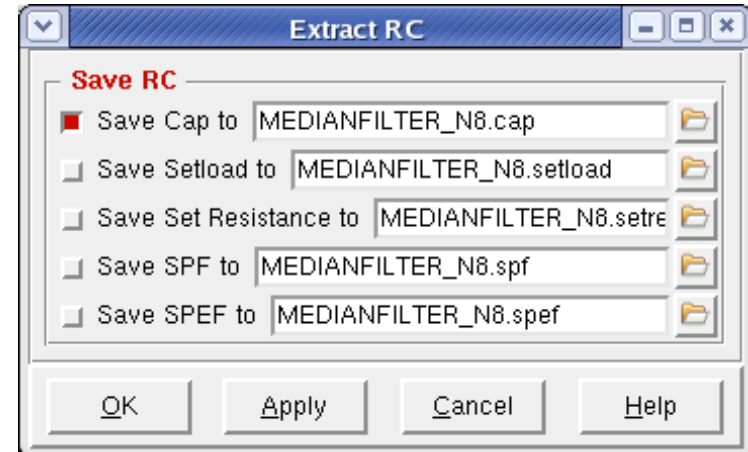
Add Filler cells

- Final design should look as in picture if Metal 1 is set to not visible in the drawer in the right hand side of SoC Encounter.



Export Netlist and SDF

- To simulate your design in Modelsim with correct timing annotation, you need to export a netlist (your design) and SDF (Synopsys Delay Format, timing annotation).
- Timing -> Extract RC
- Timing -> Delay Cal
- Design -> Save -> Netlist



Save Design and Restore Design

- To save and restore your design use:
- Save
 - Design -> Save Design As -> SoCE
- Restore
 - Design -> Restore Design -> SoCE



Re-run entire placement

- When developing a chip, placement might be run many times and each individual step may take a long time a few hours is not uncommon.
- To avoid having to wait for each step to finish running a script is easier.
- Encounter saves all commands entered in a file called **encounter.cmd** with an added digit for every run, i.e. **encounter.cmd23** if you you are running for the 23rd time in the same directory.
- **IMPORTANT!** Don't re-run this file directly as it contains every single change performed, including zooming in and out.
- Edit the file and remove unnecessary commands, e.g. zoom, fit.
- Type **source filename.cmd** to execute an encounter script.

