

# **Backend Tools**

**Place and Route** 

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# Load Design

- Design -> Import Design
- Specify Netlist, Timing libraries, LEF files, Timing constraints, IO file
- Max timing = worst case (slowest)
- Min timing = best case (fastest)

Design Import	/// = = ×
Basic Advanced	
	[
- Verilog Netlist:	
Files: ././median_filter/netlists/medfilt.v	
Top Cell: 💸 Auto Assign 🔶 By User: MEDIANFILTER_	_N8
Timing Libraries: —	
Max Timing Libraries: /usr/local-eit/cad2/far130/syn2010/fsc0l_d_generic_core_ss	1p0;
Min Timing Libraries: /usr/local-eit/cad2/far130/syn2010/foc0l_a33_t33_generic_ir	o_ff1
Common Timing Libraries:	
LEF Files: //usr/local-eit/cad2/far130/svn2010/header8m2t_V55.lef./usr/lo	cal-ei
Timing Constraint File: 1/ /median_filter/netlists/medfilt_sdc	
OK Save Load Cancel	Help



# Load Design

Folder for backend files:

- /usr/local-eit/cad2/far130/syn2010/

- Libs:
  - fsc0l\_d\_generic\_core\_xx.lib
  - foc0l\_a33\_t33\_generic\_io\_xx.lib
- MAX-timing = worst timing =>
  - ss1p08v125c (slow-slow) (1.08V) (125 °C)
- Min-Timing = best timing =>
  - ff1p32vm40c (fast-fast) (1.32V) (- 40°C)





# Load Design

Folder for backend files:

- /usr/local-eit/cad2/far130/syn2010/

- LEFs:
  - header8m2t\_V55.lef
  - fsc0l\_d\_generic\_core.lef
  - FSC0L\_D\_GENERIC\_ANT\_V55.8m2t.lef
  - foc0l\_a33\_t33\_generic\_io.8m2t.lef
  - FOC0L\_A33\_T33\_GENERIC\_IO\_ANT\_V55.8m2t.lef



## Load Design - Memories

• Libs and Lef in mem.tar.gz



#### Load Design – Power networks

- Choose Advanced Tab:
  - Add power nets call them something like:
     VCC & GND

$\mathbf{\overline{\mathbf{v}}}$	Design Import	// <b> ×</b>
Basic Advanced		1
Delay Calculation GDS ILM IPO/CTS OpenAccess Power RC Extraction RTL SI Analysis Timing Yield MMMC	Power Nets: VCC Ground Nets: GND Toggle Rate Scale Factor: 1.0	
<u>0</u> K	Save Load Cancel	<u>H</u> elp





- Power network, e.g., VCC connect to TIEHI, Pin VCC.
- Ground network, e.g., GND connects to TIELO, Pin GND.
- Scope: Apply All



# Floorplan

- Resize floorplan to fit memories
- Floorplan -> Specify Floorplan
- The size of memories can be measured with the ruler tool.
- Zoom in (z), Zoom out (shift+z), Fit to screen (f),





🔶 Lower Left Corner 📣 Center

<u>C</u>ancel

Floorplan Origin at:

Apply

<u>0</u>K



Unit: Micron

<u>H</u>elp

#### **Place and rotate memories**

- Move memories by selecting movement tool is or press "Shift+R".
- Need to rotate memories to have pin connections inside the core.
- Rotate memories by edit proporties for selected object by pressing "q".
- Orientation set to R180 for 180 degree rotation.



	Attribut	e Editor			x			
Object Type: Block								
Na	Name Value Ty							
Name	RAM_0			String				
No. of Terminals	75			Integer				
Cell Type	SHUD130_128X32X	1BM1		String				
Cell Width	750.0			Double				
Cell Height	124.0	Double						
Location	X: 1574.4	Y: 0.0	è	Location				
Location Origin	Lower Left 🛁			Origin				
Orientation				Orientation				
Status	UNPLACED -			Enumerate				
Routing Halo	None			String				
InstGroup	None			String				
<u>OK</u> <u>A</u> pply	A <u>d</u> d Prop	D <u>e</u> lete Prop	<u>C</u> lose	Help				



#### Add Halo

- Floorplan -> Edit Floorplan -> Edit Halo
- To create a ring around the memory macro, where no standard cells can be placed.
- Routing is still possible
- Be sure to specify a distance, e.g. 10 μm.







#### **Cut Rows**

- Floorplan -> Edit Floorplan -> Core Row
   -> Cut
- Deletes core rows beneath memories.
- By moving memories, the cut rows are shown.
- Now is a good time to save the design: Design -> Save Design As -> SoCE
- To restore: Design -> Restore Design -> SoCE







- Power -> Power Planning -> Add Rings
- To add Power rings around core specify Width: 2, Spacing: 2, Offset 2.
- Use metal3 for Horizontal wires and metal4 for Vertical wires.

Net(s):	GND VCC						
Ring Ty	ie						
Core	ring(s) contouri	ng					
A	round core bou	ndary	Ŷ	Along I/O bo	undary		
L D	clude selected	objects					
BIOCH	nng(s) around						
	ach block						
V S							
• E		ock and/or		of core rows			
\$ C	lusters of select	ed blocks		roups of core			
1	With shared ri	ng edges					
🗢 User	defined coordin	ates:					MouseClick
	Core ring	Slock					
Ding C-	figuration						
ning Co	mgarauun						
	Top:	Bottom	:	Left:	Righ	nt:	1
.ayer:	metal3 H	metal3	н _	metal4 V	meta	al4 V 💷	]
Width:	2	2	_	2	2	_	
Spacing:	2	2		2	2		<u>U</u> pdate
Offset:	💠 Center in c	nannel	🔶 Spe	cify			
	2	2	2	2			
	Set						
Ontion							1
Option	ntion ont			57 M			



- Make sure that an entire ring is visible under the advanced tab.
- If applied correctly your design should look like this.



- Select the memory macros and select as in the figure.
- This will create a core ring around the memory block
- If memories are placed in corners the layout of power power rings can be changed according to figure on next slide.

asic A	dvanced Via Generation
Net(s):	GND VCC
Ring Ty	pe
🔶 Core	ring(s) contouring
- • /	Around core boundary 🔷 Along I/O boundary
E E	xclude selected objects
<ul> <li>Bloc</li> </ul>	k ring(s) around
- 🔶 E	ach block
- 🔶 E	Each reef
_	Selected power domain/fences/reefs
🔶 E	ach selected block and/or group of core rows
$\diamond$	Clusters of selected blocks and/or groups of core rows
	With shared ring edges
🔷 User	defined coordinates: MouseClick
•	Core ring 🕹 Block ring
· Ring Co	onfiguration
	Top: Bottom: Left: Right:
Layer:	metal3 H 🛶 🛛 metal3 H 🛶 🖉 metal4 V 🛶 🖉 metal4 V 🛶
Width:	2 2 2
Spacing	2 2 2 Update
Offect.	← Center in channel ▲ Specify
Oliser.	
Option	Set
T Lise i	notion set



• For the upper memory no extra power routes are necessary for the top and left sides.

		Add	lings	<i>liliitiili</i> E
Basic A	dvanced Via G	ieneration		
C Set Cus	tom Ring Sides :	and Extension —		 
Create Merge wit	e rectangular ring h pre-routed rings	(s) only s if within spacing	threshold: 0.4	 
Minimum j	og distance: 0.4			
Snap wire	center to routing	grid: None		
Wire Gro	up ire group erleaving			
Numb	er of bits: 0			
📑 Re	inforcement strips	as		
S	bacing: 0	Width: 0		
	Make group via	s at ring corner		



- If successfull the design should look like the picture.
- If not, type the command: "deleteAllPowerPreroutes", use Tab key to autocomplete.
- This command clears all power routing.



×					eit-oae@ylva:~/test/soc	- 0	×
<u>F</u> ile	<u>E</u> dit	<u>V</u> iew	<u>T</u> erminal	Ta <u>b</u> s	<u>H</u> elp		
dele	teFP0b	ject			deleteSdp0bject		-
dele	teFill	er			deleteSelectedFromFPlan		
dele	teHalo	FromB	lock		deleteShield		
dele	teInst				deleteSpareModule		
dele	teInst	FromI	nstGroup		deleteTSV		
dele	teInst	Group			deleteTieHiLo		
dele	teInst	Pad			deleteWhatIfTimingAssertions		
dele	teIoFi	ller			delete_path_category		
dele	teIoIr	nstanc	e				
dele	teIoRo	wFill	er				
velo	city 3	8> del	eteAll				
dele	teAllC	CellPa	d	del	eteAllPtnCuts		
dele	teAllD	)ensit	yAreas	del	eteAllPtnFeedthroughs		
dele	teAllF	PObje?	cts	del	eteAllRouteBlks		
dele	teAllI	InstGr	oups	del	eteAllScanCells		
dele	teAllM	IsCons	traints	del	eteAllSignalPreroutes		
dele	teAllF	Partit	ions				
dele	teAllF	PowerP	reroutes	_			2
velo	city 3	8> del	eteAllPow	verPre	routes []		*
							•

#### **Power stripes**

- Power -> Power Planning -> Add Stripes
- Select metal4 for vertical and metal3 for horizontal



asic Adva	nced Via Generation
Set Config	uration
Net(s):	GND VCC
Layer:	metal4 🛁
Direction:	🔶 Vertical 🛛 🗸 Horizontal
Width:	2
Spacing:	2 Update
Set Patter	n
<ul> <li>Set-to-si</li> </ul>	et distance: 100
🔶 Number	of sets: 1
🔶 Bumps	🔶 Over 🛛 🕹 Between
🔷 Over P/	Gipins Pin layer: Top pin layer 💷 🔄 Max pin width: 🛛
Masi	er name:
<ul> <li>Pauring</li> <li>Design I</li> <li>Each se</li> <li>All doma</li> <li>Specify</li> </ul>	inter Clair     coundary     Create pins     lected block/domain/fence     ins     rectangular area
🔶 Specify	rectilinear area
First/Last	Stripe
Start from	: 🔶 left 💊 right
<ul> <li>Relative</li> </ul>	from core or selected area
X from I	eft:  0 X from right:  0
Absolute	locations
Option Set	
🔄 Use optio	n set: Update Basic





- Place -> Standard cells
- Change to physical view to see placed cells:







#### **Place standard cells**

 Avoids placement underneath power stripes







# **Design Clock**

- Clock -> Design Clock
- Click on Gen Spec and add all cells
- Second time use the (...) button to open your .CTSTCH file.

		Syı	nthesize Clock Tr	ee		/// = =
Basic Adv	anced		k			
Clock Specifi	cation Files:			Gen Spec		
Results Direc	tory: clock_repo	rt	_			
<u>o</u> k	Apply	Mode	Loa <u>d</u> Spec	C <u>l</u> ear Spec	<u>C</u> ancel	<u>H</u> elp





# **Design Clock**

- Shows the designed clock including a trial route.
- Type "deleteTrialRoute" to delete this.



# **Design Clock**

- It is possible to highlight the clock tree: Clock -> Display -> Display Clock Tree...
- Choose all clocks and All Level
- Clear it with Clock -> Display -> Clear Clock Tree Display.
- Clock tree Browser is shown from: Clock -> Clock Tree Browser



- opecinieu (			
-			
<b>∡</b>			
✓I ✓I Clock Select	ction ———		
<b>≤ Clock Seler</b> Clock: clk	ction ———		Select
✓I Clock Select Clock: Clk	ction		Select
Clock Select Clock: Clk	ction		Select
<ul> <li>Clock Select</li> <li>Clock: Clk</li> <li>Route Selet</li> <li>Pre-Rout</li> </ul>	ction		Select
Clock Selec Clock: Clk Route Sele Pre-Rout Clock Ro	ction		Select
Clock Select Clock: Clk  Route Select  Clock Re  Clock Re  Clock Re  Clock Re  Clock Re  Clock Re	ction ction te oute Only ite		Select
Clock Selec Clock: cik Route Sele Pre-Rout Clock Ro Post-Rou	ction ction e oute Only ite	Cancel	Select

# **IO Filler cells**

- Place -> Physical Cells -> Add IO Filler
- Cells are named: EMPTY16LB EMPTY8LB EMPTY4LB EMPTY2LB EMPTY1LB
- Tick Fill Any Gap
- Select which side to add to, add to all sides.







## **IO Filler cells**

• If successfull design should look as in picture.





# **Special Route**

- Route -> Spceial Route
- Routes GND and VCC net for powering of standard cells.

2	SRoute	- • ×
	Basic Advanced Via Generation	
		[
	Net(s): GND VCC	
	Route	
	Routing Control	
	Ton Layer metals Bottom Layer metal	
	Allow Jagging     Allow Jagging     Allow Jagging	
	Area	
	X1: V1: Draw	
	X2: Y2:	
	Connect to Target Inside The Area Only	
	Delete Existing Routes	
	L Extra Confin File:	
	<u>QK</u> <u>Apply</u> <u>Defaults</u> <u>Cancel</u> <u>Hel</u>	р









#### **Route normal nets**

- Route -> Nanoroute -> Route
- Run with default options.

	<u> And And And And And And And And And And</u>	<u>lelelelelelelelelele</u> le	Nanc	Route	<u>an an a</u>	<u> And And And And And And And And And And</u>	
-Ro	u <mark>ting Phase</mark> Global Route						
	Detail Route	Start Iteration	0	End Iteration	default		
Pos	t Route Optimization 📋	Optimize Via 🔲 C	Optimize Wire				
6	neumont Pouting Fostu	MOC					
	Fix Antenna	I Insert Diod	es	Diode Cell Name		-	
	Timing Driven	Effort 5	Congestion	Timing	_	S.M.A.R.T.	
	SI Driven		,				
	Post Route SI	SI Victim File					
	Litho Driven						
	Post Route Litho Repa	ir					
Po	uting Control						
	Selected Nets Only	Bottom Layer	default	Top Layer	default	_	
	ECO Route	ŕ	1		,		
	Area Route	Area			è	Select Area and F	loute
-Jo	b Control						
	Auto Stop						
Nur	nber of Thread(s) For Mu	Itiple Threaded: 1					
	Number of Thread(s) For	Superthreaded: 1					
	Number of Hest(s) For	Superthreaded: 0					
	Set Multiple CPU						
	<u>O</u> K <u>A</u> pply	Attribute	Mode	<u>S</u> ave	<u>L</u> oad	<u>C</u> ancel	<u>H</u> elp

# Analyze Timing

- Before adding fillers we need to make sure that we meet timing, both setup and hold.
- Timing -> Analyze Timing
- Choose which design stage we are in, at this point Post-Route.
- Select both Setup and Hold, one after each other.

2	Timing Analysis									
	Basic Advanced									
	Use Existing Extraction and Timing Data									
	Design Stage									
	💠 Pre-Place 💊 Pre-CTS 💠 Post-CTS 🔶 Post-Route 🕹 Sign-Off									
	Analysis Type									
	Reporting Options									
	Number of Paths: 50									
	Report file(s) Prefix: MEDIANFILTER_N8_pos									
	Output Directory: timingReports									
	<u>OK</u> <u>Apply</u> <u>Cancel</u> <u>H</u> elp									



# Analyze Timing cont'd

- Make sure that we have no setup nor hold violations.
- WNS stands for Worst Negative Slack
- TNS stands for Total Negative Slack.
- If we do we need to run optimize timing, to solve this issue.

optDesign Final	Summary

+]   Setup mode	all	reg2reg	in2reg	reg2out	in2out	clkgate
WNS (ns):	5.242	5.242	15.707	N/A	N/A	N/A
TNS (ns):	0.000	0.000	0.000	N/A	N/A	N/A
Violating Paths:	0	0	0	N/A	N/A	N/A
All Paths:	83	75	8	N/A	N/A	N/A
Hold mode	all	reg2reg	in2reg	reg2out	in2out	clkgate
WNS (ns):	-0.019	-0.019	0.074	N/A	N/A	N/A
TNS (ns):	-0.041	-0.041	0.000	N/A	N/A	N/A
Violating Paths:	4	4	0	N/A	N/A	N/A
All Paths:	83	75	8	N/A	N/A	N/A



# **Fix Timing Violations**

- Timing -> Optimize Timing
- Select your design stage, Post-Route.
- Select which violation you which to fix, such as Hold.
- Make sure to fix Max Cap, Max Tran and Max Fanout as well.

	Optimization		/// = = ×
Design Stage			
🔷 Pre-CTS	♦ Post-CTS	🔶 Post-Route	
Optimization Type			
📕 👅 Setup	⊒ He	old	
🔷 Incremental			
Design Rules Violations	;		
📕 📕 Max Cap			
📕 Max Tran			
🔲 🔲 Max Fanout			
Include SI SI Options			
OK 📐 Apply	Mode De	efault <u>C</u> lose	<u>H</u> elp

• Do not run all things at once.



#### **Fix Timing Violations cont'd**

- Make sure that all violations are fixed.
- If not re-run optimize timing, and select the method to fix.
- If running only setup time make sure to run analyze timing for hold violations afterwards.

	optDesign Final S	ummary					
+	Setup mode	 all		 in2reσ	+	 in2out	+
+	WNS (ns):	5.049	5.049	15.699	+	   N/A   N/A	N/A
	Violating Paths:  All Paths:	0.000 0 83	0.000	0.000	N/A N/A N/A	N/A N/A N/A	N/A   N/A
++ +	+		-+	·	+	+	+
	Hold mode	all	reg2reg	in2reg	reg2out	in2out	clkgate
	WNS (ns):  TNS (ns):	0.008	0.008	0.077	N/A   N/A	N/A N/A	N/A   N/A
	All Paths:	83	75	8	N/A   N/A	N/A N/A	N/A   N/A



#### **Fix Timing Violations cont'd**

- If no reg2out, in2reg paths are found, input delay and/ or output delay are missing.
- See synthesis slides.

1						
optDesign Final S	ummary					
+		+	+	.+	+	+
Setup mode	all	reg2reg	in2reg	reg2out	in2out	clkgate
UNS (ns):  WNS (ns):  TNS (ns):  Violating Paths:  All Paths:	5.049 0.000 0 83	5.049   0.000   0   75	15.699   0.000   0   8	N/A N/A N/A N/A	N/A N/A N/A N/A	N/A   N/A   N/A   N/A
Hold mode	all	+	   in2reg	+	in2out	+   clkgate
WNS (ns):   :TNS (ns):  Violating Paths:  All Paths:	0.008 0.000 0 83	0.008 0.000 0 75	0.077 0.000 0 8	N/A   N/A   N/A   N/A	N/A N/A N/A N/A	N/A   N/A   N/A   N/A



## Add Filler cells

- Place -> Physical Cells -> Add Filler.
- Be sure to select the largest fillers first to use them when possible





### Add Filler cells

 Final design should look as in picture if Metal 1 is set to not visible in the drawer in the right hand side of SoC Encounter.





#### **Export Netlist and SDF**

- To simulate your design in Modelsim with correct timing annotation, you need to export a netlist (your design) and SDF (Synopsys Delay Format, timing annotation).
- Timing -> Extract RC
- Timing -> Delay Cal
- Design -> Save -> Netlist



✓ ////////	Calculate	Delay	// = = ×					
<b>Delay Calcu</b> Ideal Cloc	<b>lation Option</b> – k							
SDF Output File: MEDIANFILTER_N8.sdf								
<u>0</u> K	<u>A</u> pply	<u>C</u> ancel	<u>H</u> elp					



### **Save Design and Restore Design**

- To save and restore your design use:
- Save
  - Design -> Save Design As -> SoCE
- Restore
  - Design -> Restore Design -> SoCE



#### **Re-run entire placement**

- When developing a chip, placement might be run many times and each indiviual step may take a long time a few hours is not uncommon.
- To avoid having to wait for each step to finish running a script is easier.
- Enounter saves all commands entered in a file called encounter.cmd with an added digit for every run, i.e. encounter.cmd23 if you you are running for the 23<sup>rd</sup> time in the same directory.
- **IMPORTANT!** Don't re-run this file directly as it contains every single change performed, including zooming in and out.
- Edit the file and remove unnecessary commands, e.g. zoom, fit.
- Type source filename.cmd to execute an encounter script.



