Report for the Assignment of IC project and verification

Deadline March 8th. **No more than 20 pages**

For the report we expect that you write about your implementation (FSM, datapath), synthesis results, verification, and physical routing. Only ONE pdf file will be accepted.

First page is your name and student-ID

Implementation: Include the architecture and ASM and explain what is happening in words. It is not enough to provide the ASM figure without explaining it. If you are unsure about the ASM have a look at chap 11.

Synthesis: Present your synthesis results in table(s). Discuss area cost, critical path. It is expected that you provide results for a "low area" and a "high-speed" synthesis. No screen dumps from the synthesis tool.

Which constraints were set?

How many adders and multipliers and DFF were inferred by the synthesis tool? Does this number match with what you expect?

Verification: Provide an excerpt of the (post synthesis or post layout) Modelsim wave-window, where you show functionality. Change to decimal representation of the numbers. Explain what can be seen on the curves. How many clock cycles were required?

If you do post-synthesis simulation you need to do it without pads, since the clock pad will not be able to drive the registers without a synthesized clock tree.

Routing: Provide a screen dump of the layout.

Compare the final area with the estimated area from the synthesis tool. Only compare the core area.

Timing and Power Analysis: Demonstrate and discuss the performance of a fully routed design.

Discuss the performance difference between different synthesis and routing strategies and constraints. Present power figures with a coverage rate over 90%.

Appendix:

VHDL code: Use landscape format, and "2 pages" on one page!!

Clean synthesis script.

Clean routing (cmd) script.

Finally, do spell checking.