

# **Backend Tools**

Place and Route for Faraday 130nm

**Joachim Rodrigues** 

# **Import Design**

- This step will take a while. Be patient and pick exactly the files specified in the guide.
- It is possible to save/load settings using the Save button.
   Do this to avoid browsing for all files multiple times.
   This applies both to Design Import and Create Analysis Configuration.
- It is important that all files are included and in the correct order. Look for possible errors in the command prompt.
- If you need to re-import your design the tool needs to be restarted.



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# Import Design

#### • File -> Import Design

- You should enter:
  - Netlist + Top Cell
  - LEF files
  - IO file
  - Power
  - MMMC definition file (Use Create Analysis Configuration).
- · More information on next slides.





# Import Design – LEF files

- Folder for backend files:
  - /usr/local-eit/cad2/far130/syn2012/
- LEFs Physical information (Pins and Metal Layers):
  - header8m2t\_V55.lef Header LEF (Design rules)
  - $\ fsc0l\_d\_generic\_core.lef {\tt Physical dimensions for Standard Cells}$
  - FSC0L\_D\_GENERIC\_ANT\_V55.8m2t.lef Antenna information for Standard Cells
  - foc0l\_a33\_t33\_generic\_io.8m2t.lef Physical dimension for I/O Cells
  - FOC0L\_A33\_T33\_GENERIC\_IO\_ANT\_V55.8m2t.let
    - Antenna information for I/O Cells





# Import Design – Timing Files

- Folder for backend files:
  - /usr/local-eit/cad2/far130/syn2012/
- · Libs:
  - fsc0l d generic core xx.lib Low Power Standard Cell Library
  - focOl a33 t33 generic io xx.lib Low Power I/O Library
- Performance variations depending on environment: Manufacturing Process, Voltage, Temperature.
- MAX-timing = worst timing => Worst Case
  - ss1p08v125c (slow NMOS slow PMOS) (1.08V) (125°C)
- Min-Timing = best timing => Best Case
  - ff1p32vm40c (fast NMOS fast PMOS) (1.32V) (- 40°C)

Netlist

O OA

O OA

Floorpl

Verilog



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# **Import Design**

- After you have entered:
  - Netlist + Top Cell
  - LEF files
  - IO file
  - Power
- It should look something like this.
- First: Click Save.
- Afterwards: Click on Create Analysis Configuration



Design Import (on khalid.fransg)

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# **Import Design - Memories**

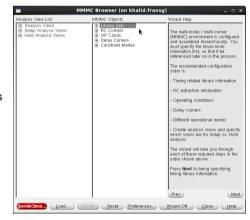
- · Memories are found in memory directory.
- LEFs:
  - SPLD130 512X14BM1A.lef
  - SHLD130 128X32X1BM1.lef
- Libs:
  - Best Case :
    - SPLD130 512X14BM1A BC.lib
    - SHLD130 128X32X1BM1 BC.lib
  - Worst Case:
    - SPLD130 512X14BM1A WC.lib
    - SHLD130 128X32X1BM1 WC.lib



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# Import Design -**Create Analysis** Configuration

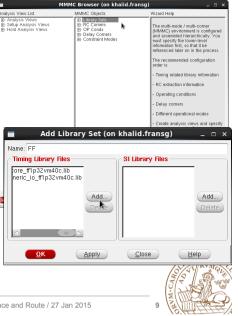
- The empty configuration looks like this.
- Feel free to read the wizard about Multi-mode-multicorner.
- · The idea is to analyze the designed chip in multiple environments at different manufacturing process variations. To make sure the fabricated chip works in all cases.
- We will now pupulate elements in the MMMC viewer.





# **Import Design -Create Analysis** Configuration

- · Start by right clicking on Library set and select New.
- · Create one set FF for best case timing
  - Add the best case timing libraries.
  - Shown on Previous slide. don't forget the memory files (not shown in figure).
- · Create a similar set SS for worst case timing.



1C Browser (on khalid.fransg

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# Import Design -**Create Analysis** Configuration

- · Create two OpConds.
- Name them: WCCOM - (SS) Worst Case BCCOM - (FF) Best Case
- · These are operating conditions defined in the lib files, and therefore, named different.
- Use the Voltage and Temperature for the specific library.

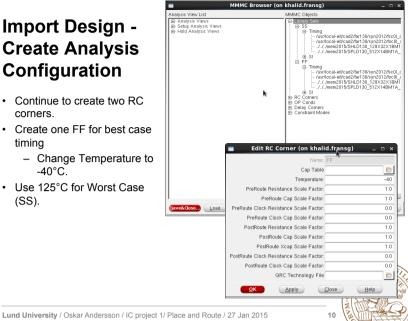
/ LISI	MMINIC Objects
Viens lysis Viens lysis Viens	Charge Set         B         SS           B         SS         B           B         SS         B           B         SS         B           B         Androcal-Wickad/Mr 300/yr021/frc01_c/         C           -         J/J Amed 215/SC1101_C/         C           B         F         F         SS           B         F         F         SS           B         F         F         F           B         F         F         F           B         F         F         F           F         F         F         F           B         F         F         F           B         F         F         F           B         F         F         F           B         F         F         F           B         F         F         F         F           B         F         F         F         F           B         F         F         F         F           B         F         F         F         F         F           B         F         F         F
Add OP Cond (o	on khalid.fransg _ 🗆 🗙
Name	e: WCCOM
Library Fil	e ic_core_ss1p08v125c.lib 🖻
Process	s: 1.0
Voltage	e: 1.08
Temperature	e: 125.0
OK Apply	<u>C</u> lose <u>H</u> elp
the ( 07 Jan 2015	SILLE AND

11

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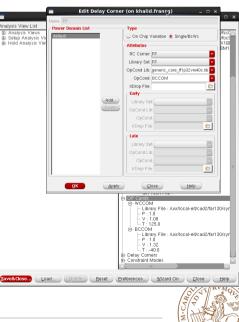
# Import Design -**Create Analysis** Configuration

- Continue to create two RC corners.
- Create one FF for best case timing
  - Change Temperature to -40°C.
- Use 125°C for Worst Case (SS).



Import Design -**Create Analysis** Configuration

- · Add two delay corners. FF, and SS.
- Choose the existing RC corner and corresponding Library Set.
- Enter the OpCond and copy the Opcond Lib from the previous OpCond dialog.



# Import Design -**Create Analysis** Configuration

· Now add the clock constraints from the SDC file (created during synthesis).

MMMC Browser (on	khalid.transg) _ 🗆 ×
	MMMC Objects
B. Analysis Views     South Analysis Views     Hold Analysis Views     Edit Constraint Mode (	- PostRoute Cap: 1.0           - PostRoute Cap: 1.0           - PostRoute Care: 0.0           - Out The Care Care Care Care Care Care Care Car
Name: Clock_constraints	
SDC Constraint Files	ILM Constraint Files
n_filter/netlists/medfilt.sdc Add Delete	Add Delete
<u>OK</u> <u>Apply</u>	<u>Close</u> <u>H</u> elp
lace and Route / 27 Jan 2015	13

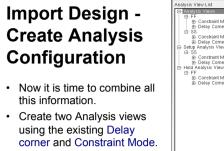
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**Import Design** 

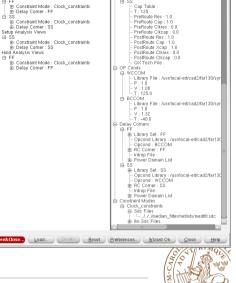
- It should now look something like this.
- · First: Click Save.
- Afterwards: Click on OK
- Next time you can use Load instead, and skip browsing for all files.

Files:	.J.J./median_filter/netlists/medfilt.v
	Top Cell: 🔾 Auto Assign 💿 By User: MEDIANFILTER_N8
D OA	
Library:	
Cell:	•
View:	
Technology/Physical Libr	raries:
⊖ OA	
- Reference Libraries:	
Abstract View Names:	
Lavout View Names:	
	SHLD130_128X32X1BM1.lef ./././mem2015/SPLD130_512X14BM1A.lef
LEF Files	
LEF Files     Floorplan	SHLD130_128X32X1BM1.lef ./././mem2015/SPLD130_512X14BM1A.lef
LEF Files     Floorplan     IO Assignment File:	
LEF Files     Floorplan	SHLD130_128X32X1BM1.lef ./././mem2015/SPLD130_512X14BM1A.lef
LEF Files     Floorplan     IO Assignment File:	SHLD130_128X32X1BM1 lef J J./mem2015/SPLD130_512X14BM1A lef
LEF Files     Hoorplan     IO Assignment File:     Power	SHLD130_128X32X18MI lef J J./mem2015/SPLD130_512X148MIA.lef
LEF Files     Floorplan     IO Assignment File:     Power     Power Nets:	SHLD130_128X32X18MI lef J J./mem2015/SPLD130_512X148MIA.lef
LEF Files     Hoorplan     IO Assignment File:     Power     Power      Cround Nets:     CPF File:	SHLD130_128X32X18MI lef J J./mem2015/SPLD130_512X148MIA.lef
LEF Files     Floorplan     IO Assignment File:     Power     Power Nets:     Ground Nets:     CPF File:     Analysis Configuration	SHLD130_128X32X18MI lef J J./mem2015/SPLD130_512X148MIA.lef

Design Import (on khalid.f<u>ransg)</u>



- · Select to SS Analysis View as Setup Analysis View
- · Select to FF Analysis View as Hold Analysis View
- · The design should look like the screenshot.
- · Do not forget to save the MMMC file.



Power Ground

Connect

> Pin

+ Tie High

- Tie Low

Instance Ba Pin Name(s): Net Basename Single Instance: Under Module

Under Power Domain

× 0.0

Under Region: 1

Override prior cor

Verbose Output Add to List

Reset

Apply All

To Global Net VC

CC PIN\* VCC AI

VCC:TIEHI:".:All

ND:PIN:<sup>\*</sup>.GND:AI ND:TIELO:\*.:AII

Apply

on khalid.fransg

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# **Global Net Connect**

- To connect the power networks: Power -> Connect Global Nets...
- Two types: Pin & TieHi/Low
- Power network, e.g., VCC connect to TIEHI, Pin VCC.
- · Ground network, e.g., GND connects to TIELO, Pin GND.
- Scope: Apply All



Delete

Help

ly: 0.0 uns 0.0 ury: 0.0

Close

#### Floorplan



Basic Advanced

Snacify Ru- 🔶 Size .

A. Com Size In

Die Size

Die Size Calculation Use Floorolan Origin at

Routing Hal

ок |

/ + Com to 10 B

Apply

Cancel

Core to Die B Core to Left

- · Resize floorplan to fit memories
- Floorplan -> Specify Floorplan
- The size of memories can be measured with the ruler tool.
- To zoom use the zoom buttons:  $\bigcirc \bigcirc \bigcirc$
- Zoom in (z), Zoom out (shift+z), Fit to screen (f)
- · Also right-click and drag a square to zoom in a to a desired area.



Help

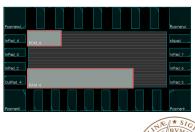
0.59036

0.028826

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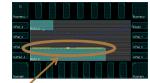
#### Add Halo

- Floorplan -> Edit Floorplan -> Edit Halo
- To create a ring around the memory macro, where no standard cells can be placed.
- · Routing is still possible
- · Be sure to specify a distance, e.g. 10 µm.



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# Place and rotate memories



- · Move memories by selecting movement tool <br/>
  tool Topress "Shift+R".
- Need to rotate memories to have pin<sup>2</sup> connections inside the core.
- Rotate memories by edit proporties for selected object by pressing "q".
- Orientation set to R180 for 180 degree rotation.
- · Afterwards change to normal pointer by selecting the arrow next to 🚸 or press "a".

ame	Va	lue	ту	pe
RAM_0				String
75				Integer
SHUD130_1	0X32X18	41		String
750.0				Double
124.0				Double
× 1574.4	Y	0.0	2	Location
Lower Left	-			Origin
				Orientati
UNPLACED	-			Enumera
None				String
None				String
	RAM_D 75 SHUD130_12 750.0 124.0 X: 1574.4 Lower Let UNPLACED None	RAM_D 75 SHUD130_128X32X18F 750.0 1784.0 Kore		РАМ_D  75  5460/30_120432/18441  7503  7403  7404 × 55744 × 5744  910  1049×ACED]  0000

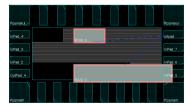


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## **Cut Rows**

- Floorplan -> Row -> Cut Core Row
- Deletes core rows beneath memories.
- NOTE: Be sure to select memories before cutting.
- · Now is a good time to save the design: File -> Save Design -Data Type: Encounter
- To restore: File -> Restore Design
- By moving memories, the cut rows are shown.
- Use undo to move back.







## **Power rings**

· To add Power rings around core

metal4 for Vertical wires.

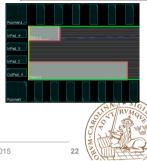
specify Width: 2, Spacing: 2, Offset 2. Use metal3 for Horizontal wires and

\$250 Advanced We Generated NHID: GND V Ang Type Core ring(s) Power -> Power Planning -> Add Rings Apply Defaults Cancel

# **Power rings**

- · Make sure that an entire ring is visible under the advanced tab.
- · If applied correctly your design should look like this.





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## **Power rings**

- Select the memory macros and select as in the figure.
- · This will create a block ring around the memory block.
- · Used to connect VDD and GND for memory.
- · If memories are placed along the border of the die, some powerrouting can be re-used.



# **Power rings**

• For the upper memory no extra power routes are necessary for the top and left sides.

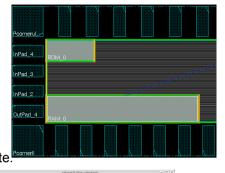






## **Power rings**

- If successfull the design should look like the picture.
- If not, type the command: "deleteAllPowerPreroutes", use Tab key to autocomplete.
- This command clears all power routing.



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File Edit View



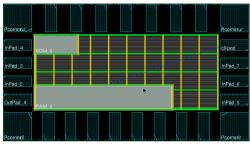
- Place -> Physical Cell -> Add well Tap
- Adds contacts for well and substrate.
- Use cell FILLER4ELD

**Place well taps** 

- Use a spacing of 25µm.
- Prefix WELLTAP

# **Power stripes**

- Power -> Power Planning -> Add Stripes
- Select metal4 for vertical and metal3 for horizontal



Add Stripes	-
C Advanced Via Generation	
Let Configuration	
H4(S): GND VCC	
ayar: nettild	
inction:   Vertical   Horizontal	
11ath: 2	
pacing 2 Update	
iet Pattern	
Sel-to-set distance: 100	
- Number of sets: 1	
Bumps 🗢 Over 🧇 Bebreen	_
- Over P/G pins Pin layer. Top pin layer 🛶 📋 Max pin width: 🛛	
Master serve: Selected blocks - All blocks	
Plant ing i inter the Outer - Declip boundary IF Consta pros Such switch to bocktronia/Mence - Al domine - Specify rectangular area - Specify rectangular area	
instituast Stripe	
Start from: 🔶 latt. 🤝 right	
Peladive from core or selected area	
X from left: 0 X from right 0	
- Absolute locations	
ption Set	
Use option set	



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# **Place standard cells**

Place -> Specify -> Placement Blockage



- Place -> Place Standard cells
- Change from "Floorplan view" to "Physical view" to see placed cells:





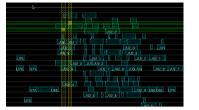




#### Place standard cells

- Zoom in close to a crossing of two metal stripes in the middle of the die.
- Hide signal wires by expanding "Net" in the right hand control "Layer Control" and untick "Net".
- · You should see that no cells are placed underneath metal stripes.
- · Like in the lower figure.
- Now show the nets again.

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# **Design Clock**

- Clock -> Synthesize Clock
- · Click on Gen Spec and add all cells
- Second time use the (...) button to open your .CTSTCH file.

-	Synthesize Clock Tree	- C X
Bas	Advanced	
Clo	ck Specification Files: Gen Spec	
Res	uits Directory: clock_report	
Q	K Apply Mode Loag Spec Clear Spec Cancel	<u>t</u> eip
	Cells List Selected Cells	_
	INVLLD Add	T.
	INVMLD INVNLD	<u> </u>
	INVQLD Delete	1
	Output Specification File: Clock.ctstch	
	QK Apply Clear Spec Cancel Help	

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#### **Design Clock**

- Now the synthesized clock with clock buffers and including a trial route of the remaining signals nets is shown.
- Type "deleteTrialRoute" to delete the trial route and only show the clock net.



# **Design Clock**

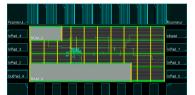
- It is possible to highlight the clock tree: Clock -> Display -> Display Clock Tree...
- Choose all clocks and All Level
- Clear it with Clock -> Display -> Clear Clock Tree Display.
- To see which buffers and inverters are used in the clock tree, use the clock tree Browser: Clock -> Browse Clock Tree





# **IO Filler cells**

- Before placeing IO-fillers the pads need to be aligned on a 0.4µm x 0.4µm grid. As the width of minimum filler is 0.4µm.
- Select all pads in the top row except the right corner pad.
- Floorplan -> Edit Floorplan -> Space
- Enter a spacing value similar to the current spacing (Use ruler "k" to measure).
- Choose "Horizontal Spacing" and "Fix Left". For Right and Left side use "Vertical spacing".
- Verify with ruler that distance is a multiple of 0.4µm.



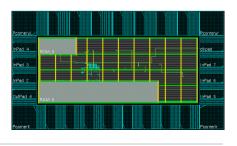


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## **IO Filler cells**

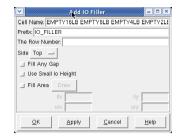
• If successfull design should look as in picture.

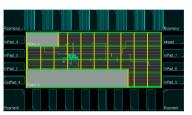


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# **IO Filler cells**

- Place -> Physical Cells -> Add I/O Filler
- Cells are named: EMPTY16LB EMPTY8LB EMPTY4LB EMPTY2LB EMPTY1LB
- Prefix: IO\_FILLER
- Select which side to add to: Top/Bottom/Right/Left.
- The screen does not auto-refresh (press "f").
- · Add to all sides.





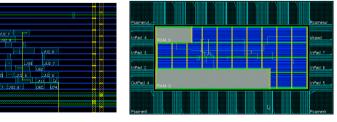


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## **Special Route**

- Route -> Spceial Route
- Routes GND and VCC net for powering of standard cells.









#### Route normal nets

Route -> Nanoroute -> Route

#### Run with default

Run with default options	Routing Phase
· · · · · · · · · · · · · · · ·	F Global Route
	Detail Route     Start Iteration     D     End Iteration     default
	Post Route Optimization _ Optimize Via _ Optimize Wire
	Concurrent Routing Features
	Fix Antenna 🔄 Insert Diodes Diode Cell Name
	Timing Driven Congestion Timing S.M.A.R.T.
	Enori S
	SI Driven
	Post Route SI SI Victim File
	🔟 Litho Driven
	Post Route Litho Repair
	- Routing Control
	Selected Nets Only Bottom Layer default Top Layer default
	ECO Route     ECO Route
	Area Route Area Elect Area and Route
	Job Control
	Auto Stop
	Number of Thread(s) For Multiple Threaded: 1
	Number of Thread(s) For Superthreaded 1
	Number of Hinsts For Superthreaded: 0
	Set Multiple CPU
	QK Apply Apribute Mode Save Load Cancel Help
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## **Analyze Timing**

- · Before adding fillers we need to make sure that we meet timing, both setup and hold.
- Timing -> Report Timing
- · Choose which design stage we are in, at this point Post-Route.
- · Select both Setup and Hold, one after each other.

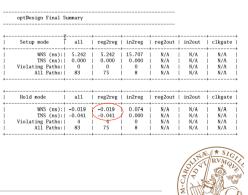
9	Timing Analysis	
	Basic Advanced	
	☐ Use Existing Extraction and Timing Data	
	- Design Stage	
	Analysis Type ◆ Setup ◇ Hold □ Include SI	
	Reporting Options	
	Number of Paths: 50	
	Report file(s) Prefix: MEDIANFILTER_N8_pos	
	Output Directory: timingReports	
ļ		
	QK Apply Cancel Help	

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Analyze Timing cont'd

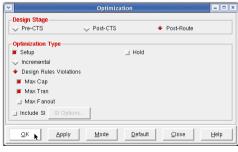
- Make sure that we have no setup nor hold violations.
- WNS stands for Worst **Negative Slack**
- TNS stands for Total Negative Slack.
- If we do we need to run optimize timing, to solve this issue.



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# **Fix Timing Violations**

- Optimize -> Optimize Design
- · Select your design stage, Post-Route.
- · Select which violation you which to fix, such as Hold.
- Make sure to fix Max Cap, Max Tran and Max Fanout as well.
- · TIP: Do not run all things at once.





# Fix Timing Violations cont'd

Make sure that all violations are fixed.
 If pat to run entimize

٠	If not re-run optimize
	timing, and select the
	method to fix.

 If running only setup time make sure to run analyze timing for hold violations afterwards.

Setup mode	all	reg2reg	in2reg	reg2out	in2out	clkgate
WNS (ns):	5.049	5.049	15.699	N/A	N/A	N/A
TNS (ns):	0.000	0.000	0.000	N/A	N/A	N/A
Violating Paths:	0	0	0	N/A	N/A	N/A
All Paths:	83	75	8	N/A	N/A	N/A
 Hold mode	all	reg2reg	in2reg	reg2out	in2out	clkgate
WNS (ns):	0.008	0.008	0.077	N/A	N/A	N/A
TNS (ns):	0.000	0.000	0.000	N/A	N/A	N/A
Violating Paths:	0	0	0	N/A	N/A	N/A
All Paths:	83	75	8	N/A	N/A	N/A



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# **Another note on Timing Violations**

- If timing violations are still seen after multiple runs with a larger design, what to do?
- Run Optimize Timing after each design stage, i.e:
  - After placement (before Clock Tree Synthesis) Pre-CTS
  - After Clock Tree Synthesis Post-CTS
  - After Routing Post-Route
- Try using incremental optimization for hold after the setup optimization.
- · Reduce clock speed.
- Increase die size, i.e., have a lower die utilization.



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# Fix Timing Violations cont'd

- If no reg2out, in2reg paths are found, input delay and/ or output delay are missing.
- See synthesis slides.

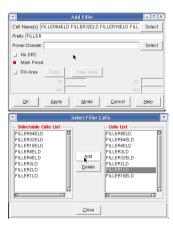
I	Setup mode	all	reg2reg	in2reg	reg2out	in2out	clkg
1	WNS (ns):	5.049	5.049	15.699	N/A	N/A	N/
1	TNS (ns):	0.000	0.000	0.000	N/A	N/A	N/A
1	Violating Paths:	0	0	0	N/A	N/A	N/A
1	All Paths:	83	75	8	N/A	N/A	N/4
			-+	+	+	+	+
+ 	Hold mode	all	-+	in2reg	reg2out	in2out	+
+   +	Hold mode   WNS (ns):	all 0.008	reg2reg	in2reg	reg2out	in2out	+
+   +   	+-		-+	+	+	+	N/
+   +   	WNS (ns):	0.008	0.008	0.077	N/A	N/A	clkga   N//   N//   N//



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## Add Filler cells

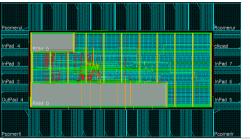
- Place -> Physical Cells -> Add Filler.
- Be sure to select the largest fillers first to use them when possible





## Add Filler cells

• Final design should look as in picture if Metal 1 is set to not visible in the drawer in the right hand side of Encounter.



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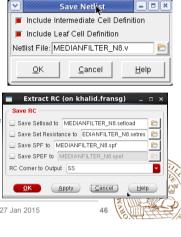


## **Export Netlist and SDF**

- To simulate your design in Modelsim with correct timing annotation, you need to export a netlist (your design) and SDF (Synopsys Delay Format, timing annotation).
- Timing -> Write SDF
- Be sure to untick Ideal Clock
- This dialog runs the "write\_sdf" command in the background. However, to avoid errors in ModelSim, use this "write\_sdf" command in your script: write\_sdf -version 2.1 -interconn nooutport file.sdf
- File -> Save -> Netlist
- It is also possible to save SPF, SPEF for further use in Power and Timing analysis.
- Timing -> Extract RC (Chose which RC corner to output.)

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# Save Design and Restore Design

- · To save and restore your design use:
- · Save
  - File -> Save Design
- Restore
  - Design -> Restore Design



Re-run entire placement

- When developing a chip, placement might be run many times and each indiviual step may take a long time, and a few hours is not uncommon.
- To avoid waiting for each step to finish running a script is easier.
- Enounter saves all commands entered in a file called encounter.cmd with an added digit for every run, i.e. encounter.cmd23 if you you are running for the 23<sup>rd</sup> time in the same directory.
- **IMPORTANT!** Don't re-run this file directly as it contains every single change performed, including zooming in and out.
- Copy the file and remove unnecessary commands, e.g., zoom, fit.
- Type source filename.cmd to execute an encounter script.

