

# IC-Project 1

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# Scope

A project course to give experience in practical design in a modern design environment.

- State-of-the-art EDA tools
- 130/65 nm CMOS

Unique possibility to design an IC!

In groups of 2 students

- VT1 : one assignment to learn the tools and improve/refresh VHDL
  - VT2 : projects
  - HT1/2: verification by measurements
- Applications mainly from signal processing

Can be upgraded to a Master Thesis



# Assignment

During VT1 2016 you need to carry out one compulsory assignment which you will take through an entire digital ASIC design flow

- Matrix multiplier (controller+datapath)
  - RTL implementation
  - Simulation
  - ASIC Synthesis
    - Area/speed constraint
  - Physical placement and routing
  - Power simulation and static timing analysis



# Matrix Multiplier Reports

Feedback will be provided at the end of May

**No update** of the report is required, but we assume that you will consider feedback in the project reports



# Grading

Grade will depend on all parts of the course

- assignments
- project results
- oral presentations
- written report (more than one major revision will lower your grade)

Usually the project/group is given the same grade. However, individual grades might be given depending on the situation, e.g., group dynamics.

All tasks need to be completed **in time** if you are targeting higher than a passing grade.

Project deadline June 4<sup>th</sup>

Report deadline June 11<sup>th</sup>



# Schedule

- This course will be conducted like a small scale project.
- No schedule in the database
- Meetings will be organized by Doodle and announced on the course homepage
- If you can not come to a meeting it is compulsory that you inform us **well ahead** of the meeting time (email)



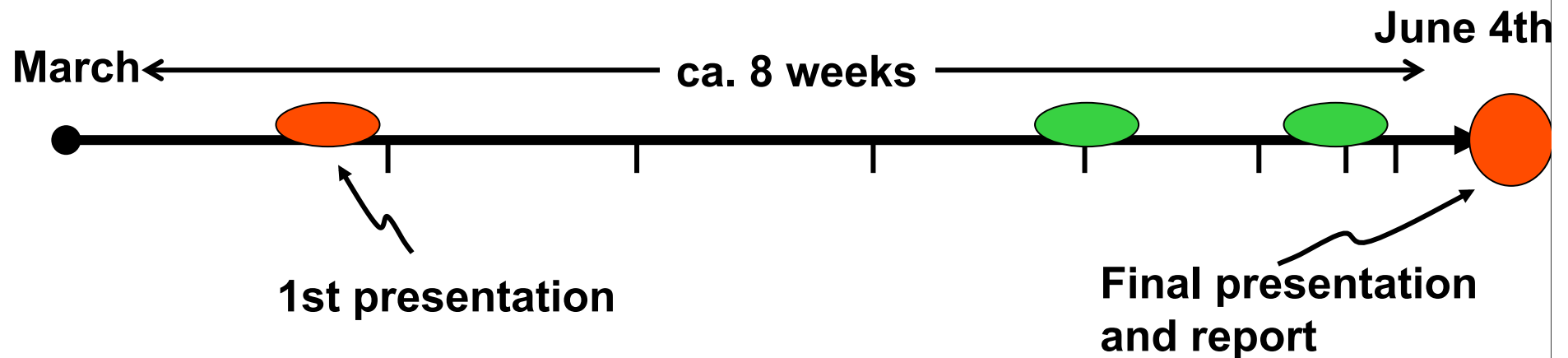
# Plagiasm

Do not copy any material from other students or the internet.

We use an automized system that will check all reports and code.



# Project



Time is “relative”: The closer you get to the deadline the faster the time will progress





# First Task

We will use 65nm from STM

Please update your synthesis and PnR flow to this technology

- Change of libraries
- New memory



# 1st Student Presentation

Goal: you will introduce you project to your course mates, 5 minutes

Feedback on you project schedule and presentation style will be provided.

Who wants “public” feedback?



# Questions??

