

# Integrated Radio Electronics

## Laboratory 3: Down-conversion Mixer

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### 1- Introduction

This lab introduces the simulation methods and software capabilities of Cadence SpectreRF commonly used for designing and verifying RF mixers. It is assumed that the students have already learned how to set up a simulation in Cadence, run it, and report the results, therefore it is strongly suggested that they do the first lab prior to this one.

Mixers are used in RF transceivers to shift the frequency content of signals. They are essentially multipliers and frequency translation is realized based on the fact that multiplication in the time domain equals convolution in the frequency domain. In receivers, RF signal is mixed with LO to get down-converted to an intermediate or zero frequency, depending on the architecture. In transmitters, mixer up-converts an IF signal to RF signal. There are two general categories of mixers: active and passive. Active mixers are biased and supplied with DC power. In this lab, a Gilbert down-conversion mixer is implemented and simulated.

Basically, we can characterize a mixer by measuring the following metrics:

- 1- Power consumption
- 2- Conversion gain
- 3- Compression point and IIP3
- 4- Noise figure
- 5- Port-to-port isolation

To evaluate the mixer performance, in this lab the following simulation are introduced:

- 1- PSS+PAC+PXF simulation for conversion gain and isolation
- 2- Transient simulation for investigating the effect of LO transitions on conversion gain
- 3- PSS+Pnoise simulation for noise evaluation
- 4- QPSS+QPAC simulation for compression point and IIP3

### 2- Schematic View

First a schematic view must be created:

- Create a schematic cellview in the RFIC\_Labs library, call it 'Mixer'.
- Draw the schematic according to Fig. 1. Use minimum length  $n/vt/p$  transistors. Set the widths to variables called 'W\_LO' and 'W\_RF'.

- Place DC voltage and current sources to bias the circuit. (ISS =1 mA, VDD = 1.2V)
- To feed in RF and LO signals we use ports terminated to 50 Ω. Then, they are split into out-of-phase components as illustrated in Fig. 2.

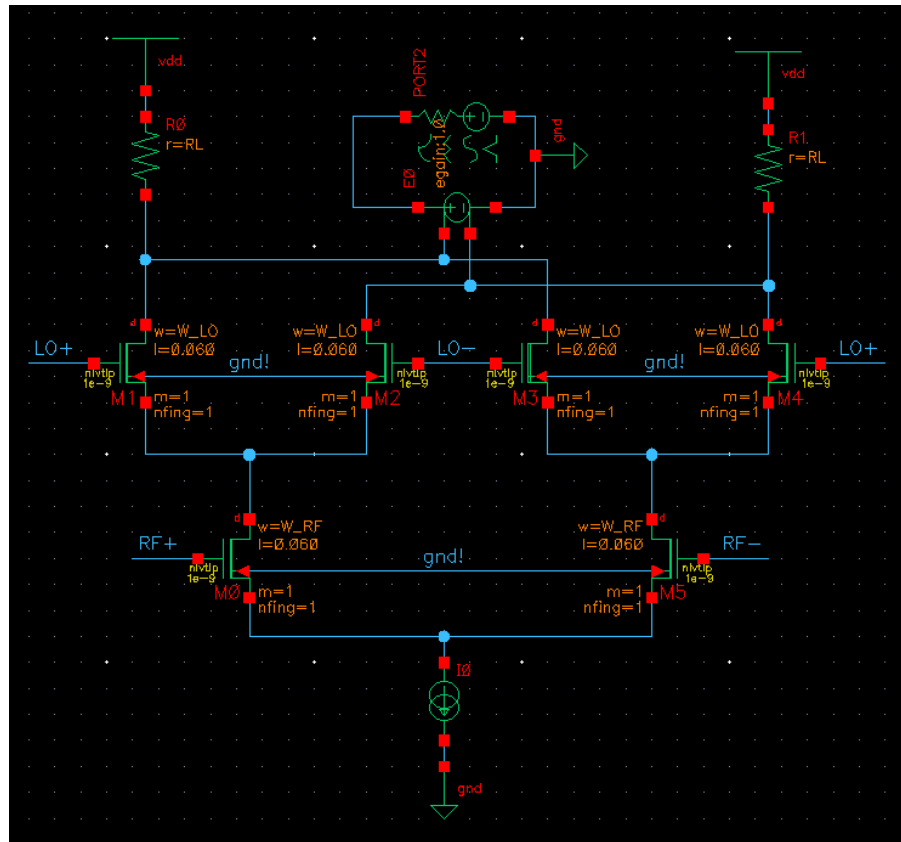


Fig. 1

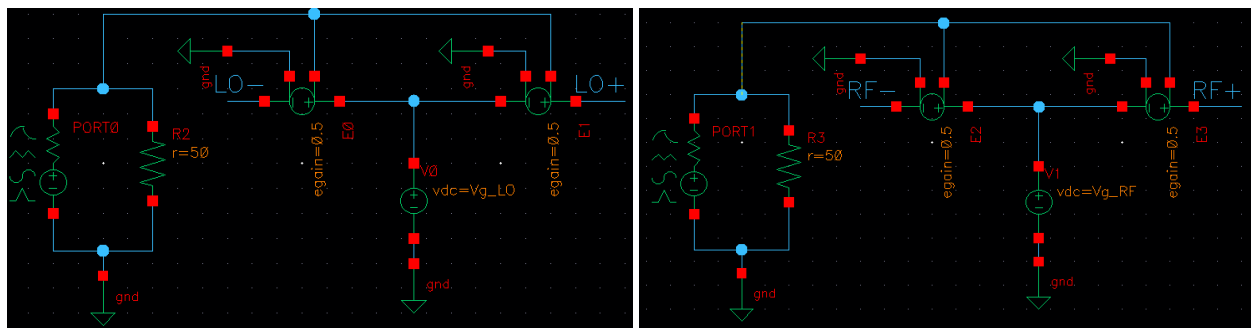


Fig. 2

### 3- Setting Analog Environment Options

To reach satisfactorily reliable and precise results the default parameters of ADE should be changed. In this way the residual errors used by the equation solver to converge to the final result become smaller.

Of course, nothing good comes free, we pay it back by larger memory usage and longer simulation time. Therefore, the values shown in Fig. 3 are chosen for a moderate but satisfactory precision.

- Under Simulation>Options>Analog (Fig. 3), set the values in TOLERANCE OPTIONS according to Fig. 4.

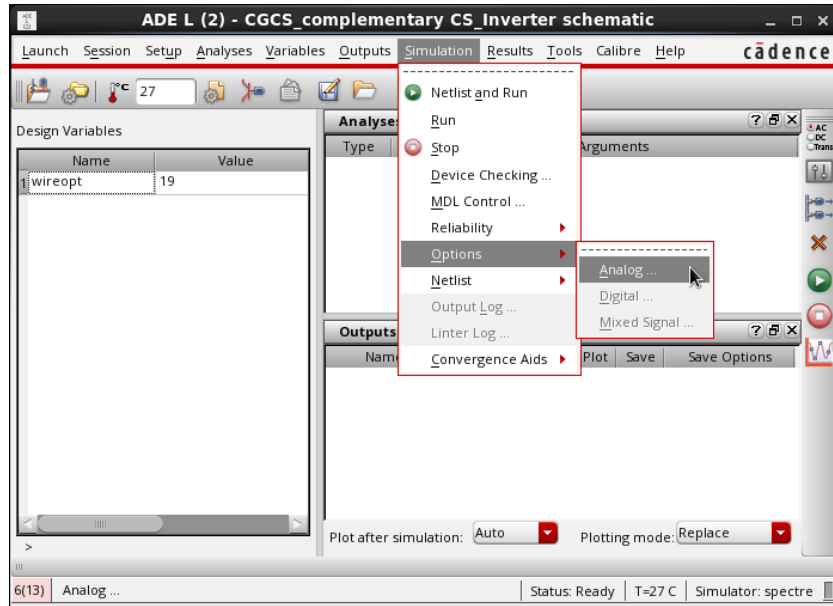


Fig. 3

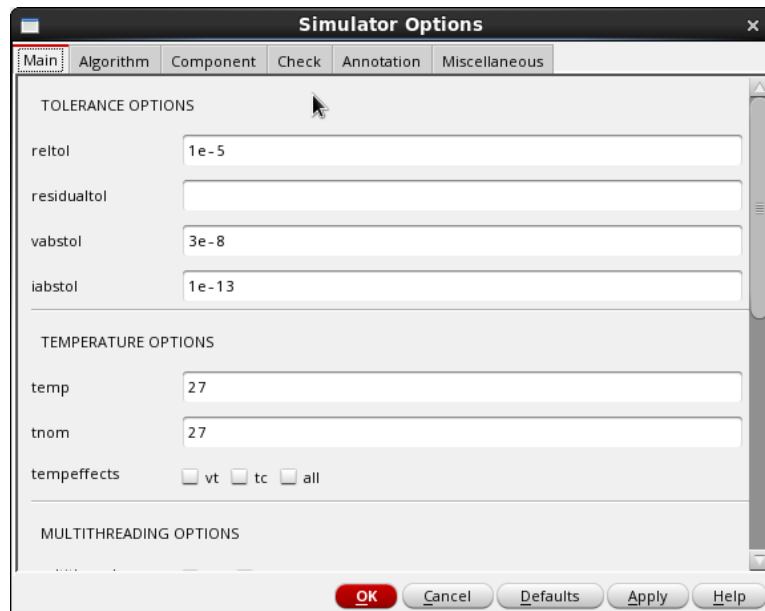


Fig. 4

## 4- Port Setup

Since in this lab a multiport circuit is simulated by different tools, it is important to carefully set the parameters of all ports.

- Configure the RF, LO, and IF ports as shown in Fig. 5 to 7 respectively.

Dialog: Edit Object Properties (on subaida.fransg.eit.lth.se)

Parameter	Value	Display
Display modulation params	<input type="checkbox"/>	off
Phase for Sinusoid 1		off
Display small signal params	<input checked="" type="checkbox"/>	off
AC Magnitude (Vpk)		off
AC phase		off
Display temperature params	<input type="checkbox"/>	off
Port resistance		off
Rport temperature coeff. 1		off
Rport temperature coeff. 2		off
Zport file name		off
Port number		off
Port capacitor		off
Port inductor		off
Suppress noise	<input type="checkbox"/>	off
Mode	<input type="checkbox"/>	off
Noise temperature		off
Temperature Source	<input type="checkbox"/>	off
Other Eido parameters		off
Frequency name 1		off
Display second sinusoid	<input type="checkbox"/>	off
Display noise parameters	<input type="checkbox"/>	off
Resistance	50 Ohms	off
Port number	1	off
Frequency 1	fr f Hz	off
Amplitude 1 (Vpk)		off
Amplitude 1 (dBm)	pr f	off
Sine DC level		off
PAC Magnitude (Vpk)	RF_pacnag V	off
PAC Magnitude (dBm)		off
PAC phase		off
XF Magnitude (Vpk)		off
Multiplier		off
Port mode	<input checked="" type="radio"/> Normal <input type="radio"/> HarmonicPort	off

Fig. 5. RF port setup

Dialog: Edit Object Properties (on subaida.fransg.eit.lth.se)

Parameter	Value	Display
Ignore	TRUE	off
CDF Parameter		
DC voltage		off
Source type	pulse	off
Voltage 1		off
Voltage 2		off
Delay time		off
Rise time	Tr s	off
Fall time	Tr s	off
Pulse width	1/2/f1o s	off
Period of waveform	1/f1o s	off
Zero value	-VP_LO V	off
One value	VP_LO V	off
Display small signal params	<input type="checkbox"/>	off
Display temperature params	<input type="checkbox"/>	off
Port resistance		off
Rport temperature coeff. 1		off
Rport temperature coeff. 2		off
Zport file name		off
Port number		off
Port capacitor		off
Port inductor		off
Suppress noise	<input type="checkbox"/>	off
Mode	<input type="checkbox"/>	off
Noise temperature		off
Temperature Source	<input type="checkbox"/>	off
Other Eido parameters		off
Frequency name 1		off
Display noise parameters	<input type="checkbox"/>	off
Resistance	50 Ohms	off
Port number	2	off
Multiplier		off
Port mode	<input checked="" type="radio"/> Normal <input type="radio"/> HarmonicPort	off

Fig.6. LO port setup

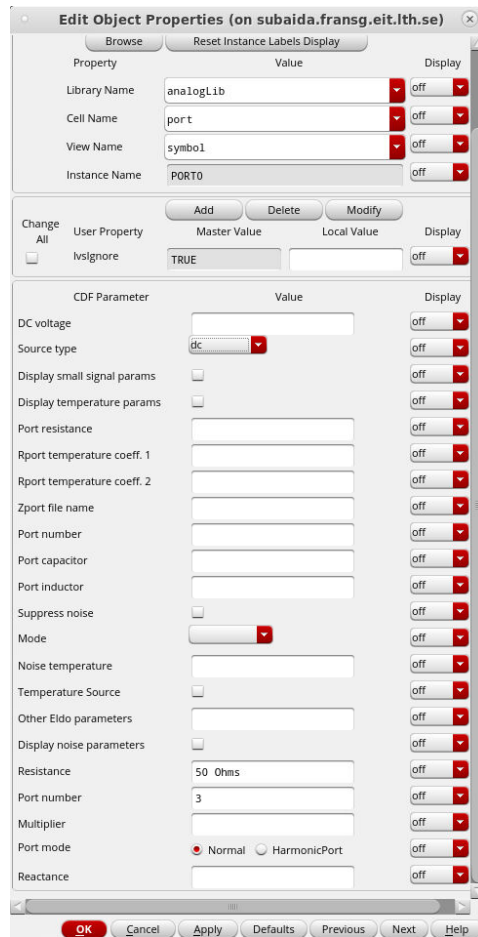


Fig. 7. IF port setup

## 5- DC Simulation

DC simulation helps to make sure that all transistors are biased properly in the active region.

- Set up the Design Variables according to Fig. 8.
- Carry out DC simulation and report the overdrive voltage of the transistors. What is the voltage across the current source? What portion of mixer's headroom is dropped on  $R_L$ ? What trade-offs do you see in this mixer?

Design Variables		
	Name	Value
1	Tr	10p
2	VP_LO	100m
3	f <sub>rf</sub>	2.4G
4	prf	-50
5	RF_pacmag	1
6	f <sub>lo</sub>	2.4G
7	RL	1K
8	Vg_LO	1
9	Vg_RF	700m
10	W_LO	40
11	W_RF	20

Fig. 8

## 6- Transient Simulation

Next step is to monitor the signals before moving on to frequency domain simulations. It provides important insights into the switching mechanism.

- In ADE, select Outputs → To Be Saved → Select On Design and select the four drain pins of the LO transistors.
- Run transient simulation with “moderate” accuracy and “stop time” = 50/VAR(“f<sub>lo</sub>”).
- Plot the drain currents of the LO transistors. Is the current completely steered to one side by the LO?
- Do a parametric sweep of VP\_LO from 50 mV to 500 mV in 10 steps and plot the currents again. What is the lowest LO amplitude that gives complete steering of the current?

## 7- Conversion Gain

The conversion gain is defined as the ratio of the RMS value of the IF voltage to the RF input. In this section we trace the conversion gain variations versus RF and LO power. If the input and output of the mixer are matched to the same resistance, the voltage conversion gain equals the power conversion gain in dB.

To calculate the conversion gain, in this lab we use PSS+PAC simulation as follows.

### 7-1- LO Power Sweep

- In the RF port, set the source type to DC.
- In ADE, choose PSS simulation and set its parameters according to Fig. 9.

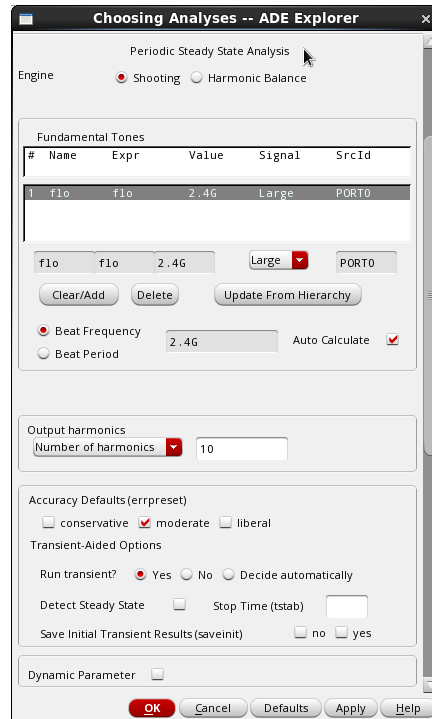


Fig.9

- Check “sweep” option in PSS form and set it up as shown in Fig. 10.

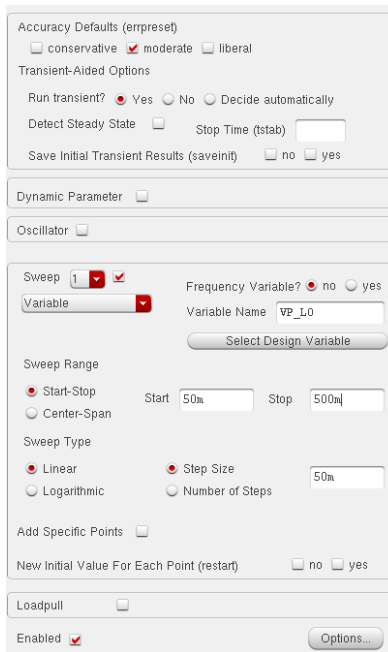


Fig. 10

- Choose PAC analysis and set its parameters as illustrated in Fig. 11.

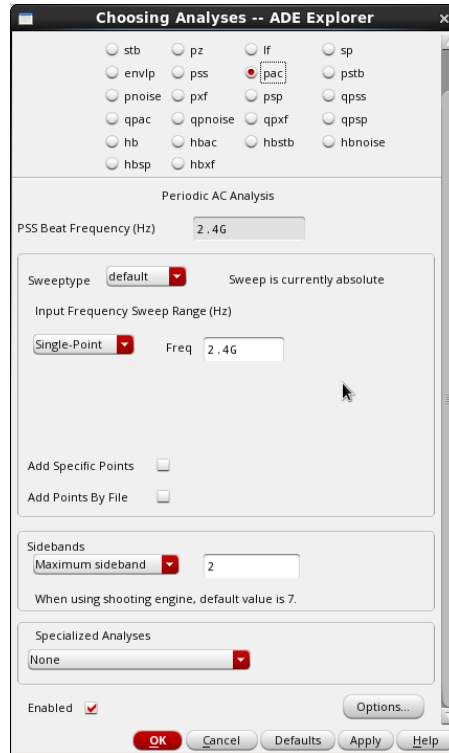


Fig. 11

To plot the conversion gain, open Results/Direct Plot/Main form and select PAC and set the parameters as shown in Fig. 12. Then, click on the output net (positive terminal of the IF port).



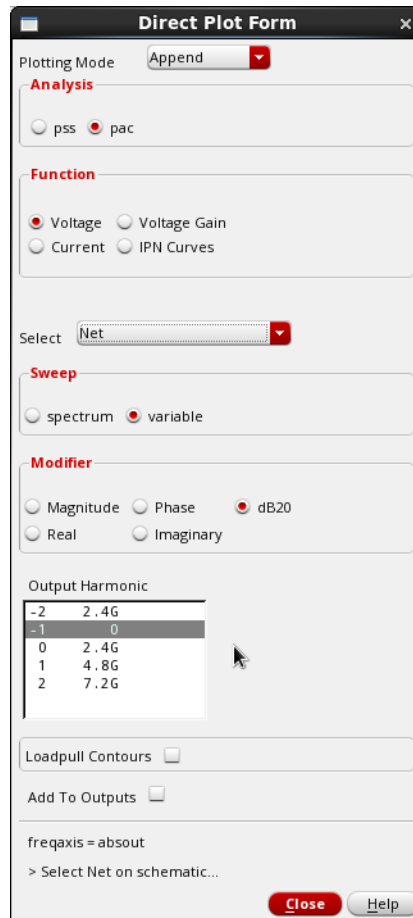


Fig. 12

Note that the Voltage in dB is equal to the voltage conversion gain because we set the input RF voltage to 1.

- Measure the LO voltage at which the conversion gain reaches its maximum. We call this value VP\_LO\_max from this point of the manual.
- Is the conversion gain in agreement with the theory? What do you expect to happen to it if we double the bias current and transistor's width and halve the load resistance? What happens if we keep the load resistance constant?

## 7-2- RF Frequency Sweep

- Set VP\_LO to VP\_LO\_max and uncheck the sweep box in PSS setup form.
- Change PAC setup according to Fig. 13. This way the simulation tool sweeps RF frequency from 2.3 to 2.5 GHz.
- Plot the conversion gain from Results/Direct Plot/Main form/PAC/Voltage as illustrated in Fig. 14.

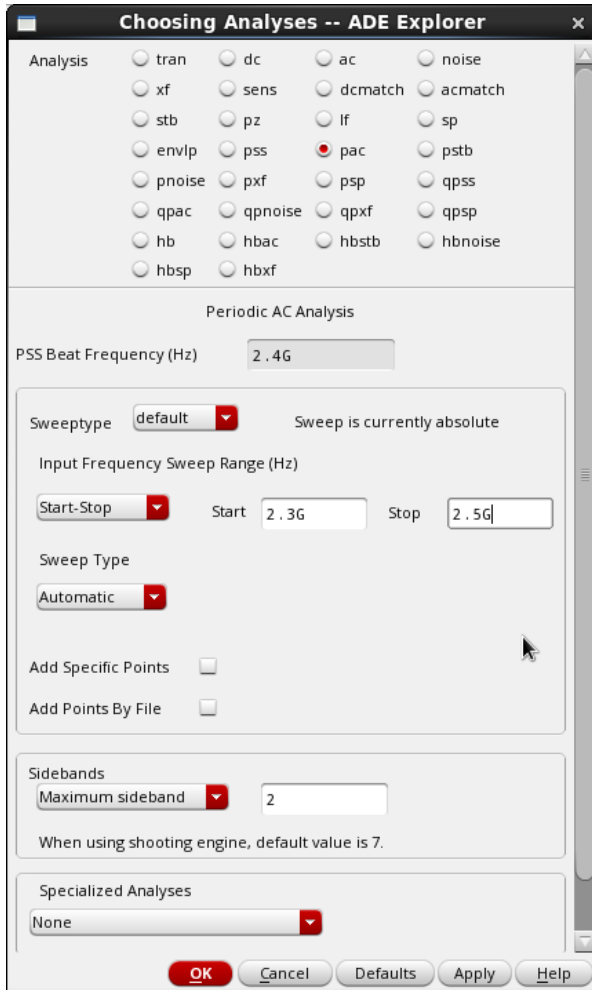


Fig. 13

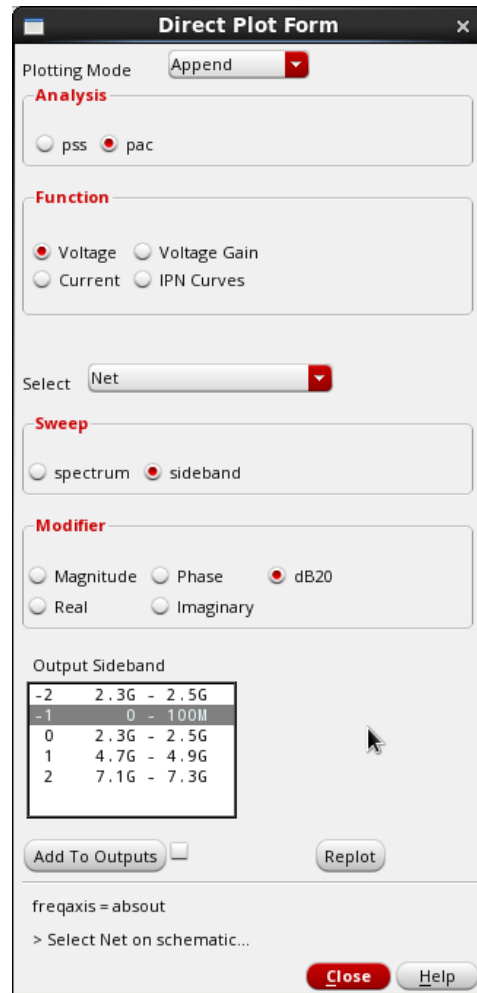


Fig. 14

- Can you justify the result?
- Add 3 pF in parallel with each RL and repeat the simulation. Give the reason why the conversion gain behavior has changed.

## 8- Gain Compression and Intermodulation Intercept Point

The non-linear elements of the mixer lead to conversion gain degradation for large input signals. Also, the intermodulation signals get more pronounced as the input power increases because the high order components of the polynomial expansion of the gain conversion grows much faster than the fundamental tone.

To evaluate the non-linearity effects, we should run QPSS and QPAC simulations instead of PSS and PAC. It can handle multi-tonal inputs.

- Change the RF port to Sine and move the PAC small signal parameter “RF\_pacmag” from “magnitude (Vpk)” to “magnitude (dBm)”.
- Assign these values to the variables: flo = 2.4 GHz, frf = 2.401 GHz, prf = -10 dBm, RF\_pacmag = prf
- Choose QPSS simulation and enter the simulation parameters as shown in Fig. 15.
- Activate QPAC simulation and set it up like Fig. 16.

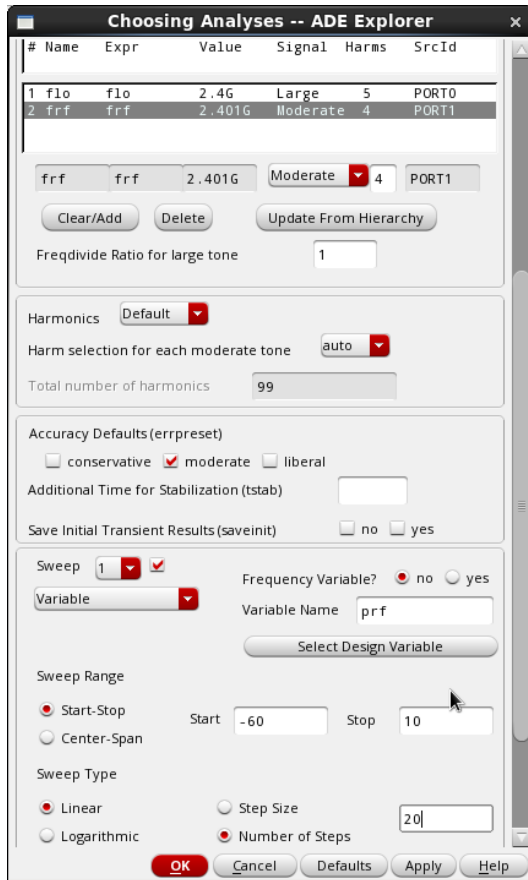


Fig. 15



Fig.16

- Run the simulation. This simulation will take quite a bit of time.
- Plot 1dB compression point from Results/Direct Plot/Main Form/QPSS, select the options as shown in Fig. 17 and click on the output port.
- Plot IIP3 from Results/Direct Plot/Main Form/QPAC, select the options as shown in Fig. 18 and click on the output port.
- Can you explain what QPAC is doing and why its frequency is set to 2.4011 GHz?

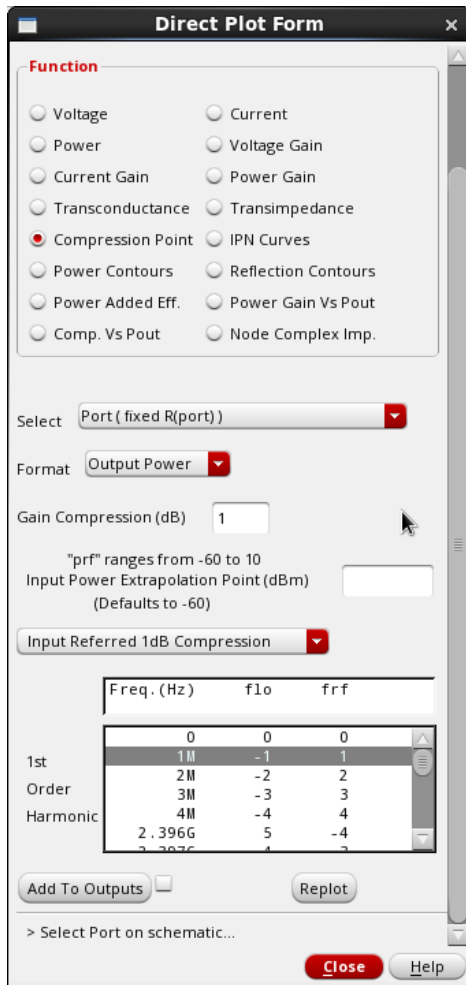


Fig. 17

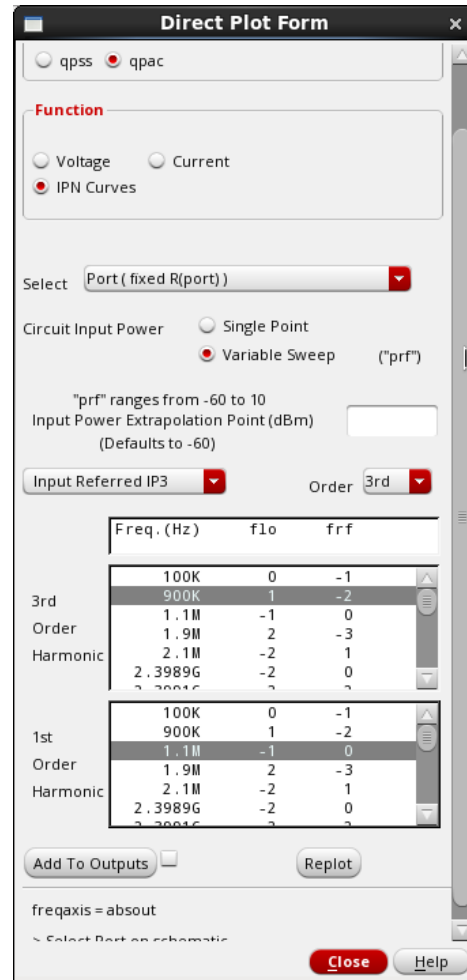


Fig.18

## 9- Port-to-Port Leakage

Capacitive couplings between RF, LO, and IF ports of a mixer make feedthrough between these three terminals possible.

LO-RF leakage causes a phenomenon called LO self-mixing which deteriorates the quality of signal capturing, particularly in direct conversion receivers. In the presence of a strong blocker, RF-LO leakage is likely to adversely affect LO and generate unwanted IF signal after getting mixed with the desired RF signal.

In this section, we will use both PAC and PXF (periodic transfer function) to simulate these feedthroughs. Both are small-signal simulations that use the results from a PSS simulation.

### 9-1- Port and Simulation Setup

- Set RF port to DC and remove RF\_pacmag.
- In the LO port, set the "PAC Magnitude" to LO\_pacmag.

- In Design Variable box assign the following values to the variables.  
frf = flo = 2.4 GHz, prf = -60 dBm, VP\_LO = VP\_LO\_max dBm, LO\_pacmag = 1
- Deactivate QPSS and QPAC.
- Enable PSS analysis and configure it as shown in Fig. 19.
- Enable PAC analysis and configure it as shown in Fig. 20.
- Activate PXF analysis and set its parameters according to Fig. 21. Select the IF port as your output probe. Note that this is the output frequency we specify, while in the PAC simulation we specify the input frequency.

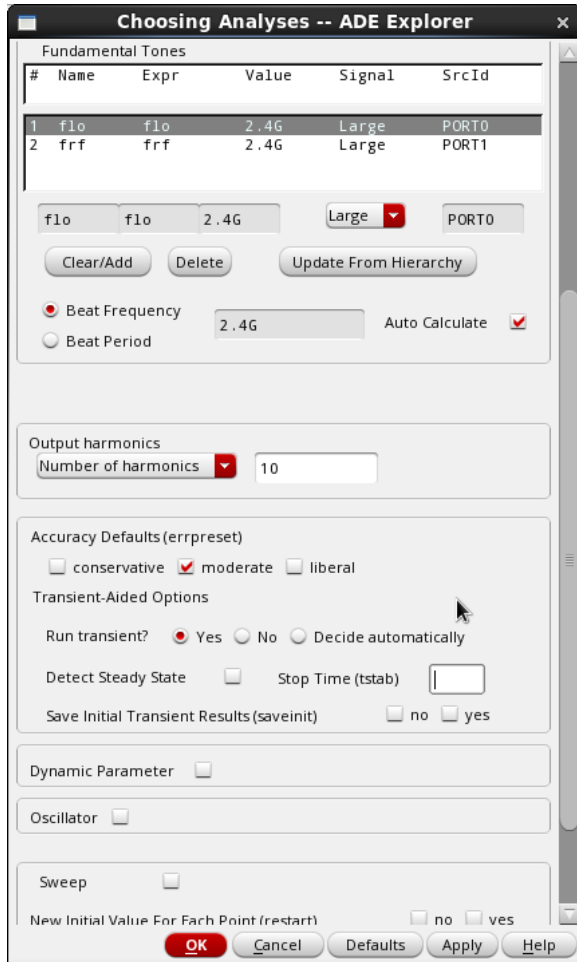


Fig. 19

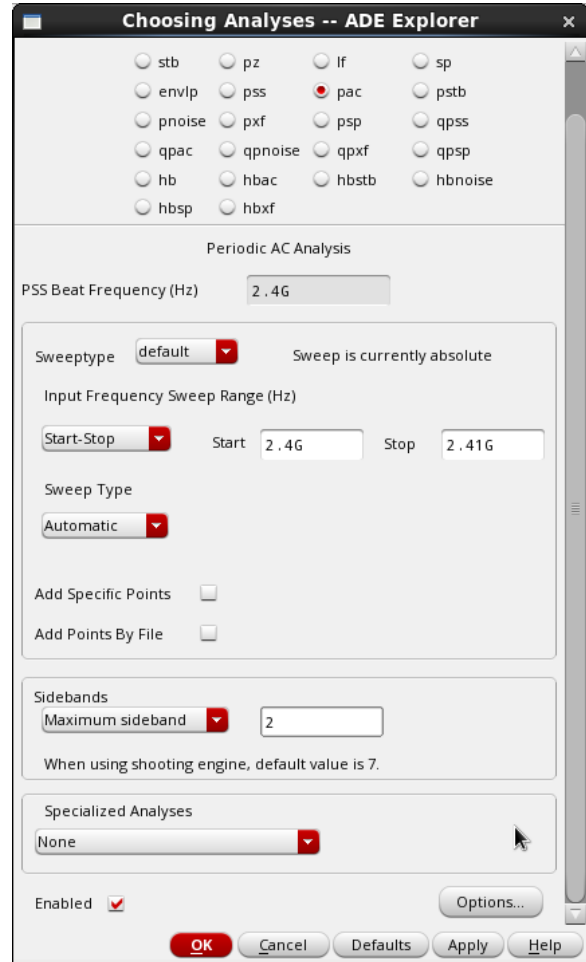


Fig.20

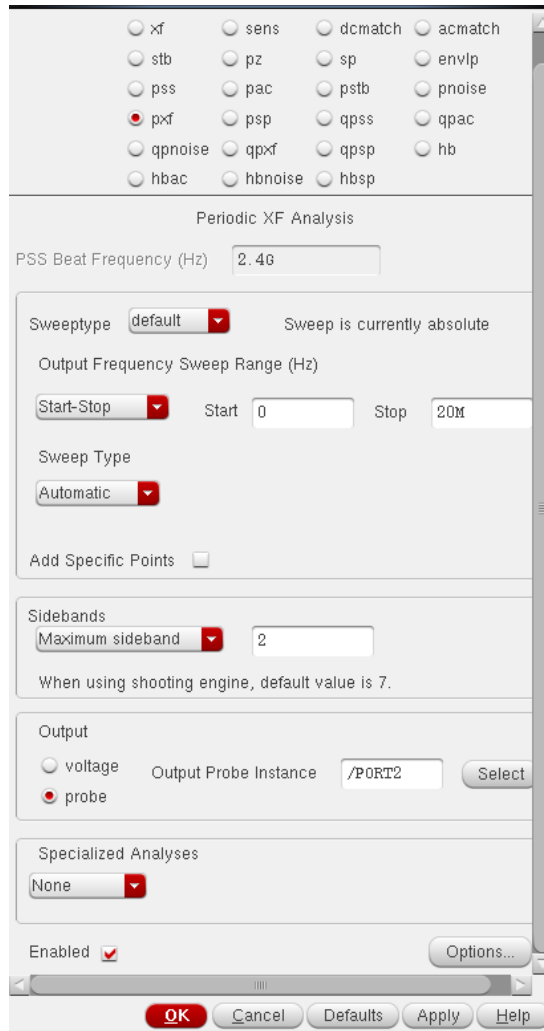


Fig. 21

- Run the simulation and follow the steps below for plotting feedthrough characteristics.

### 9-2- LO-to-IF Feedthrough

- From Results/Direct Plot/Main Form select PXF and configure the form as shown in Fig. 22.
- Click on the LO port.

### 9-3- LO-to-RF Feedthrough

- Note that this analysis will not give you any usable results, since in a small-signal analysis the RF+ and RF- nets are effectively shorted to ground through the vcvs components. For this analysis to make sense you would need to know the output resistance of the previous stage (typically the LNA) and create a better model of it. Alternatively, you could simulate the whole chain, i.e. simulate the LNA and mixer simultaneously, for the highest accuracy.

- From Results/Direct Plot/Main Form select PSS and configure the form as shown in Fig. 23 (note “Differential Nets”).
- Click on “RF+” and then “RF-”.

#### 9-4- RF-to-IF Feedthrough

- From Results/Direct Plot/Main Form select PXF and configure the form as shown in Fig. 22.
- Click on the RF port (this should give you the same result as when using PAC in section 7).

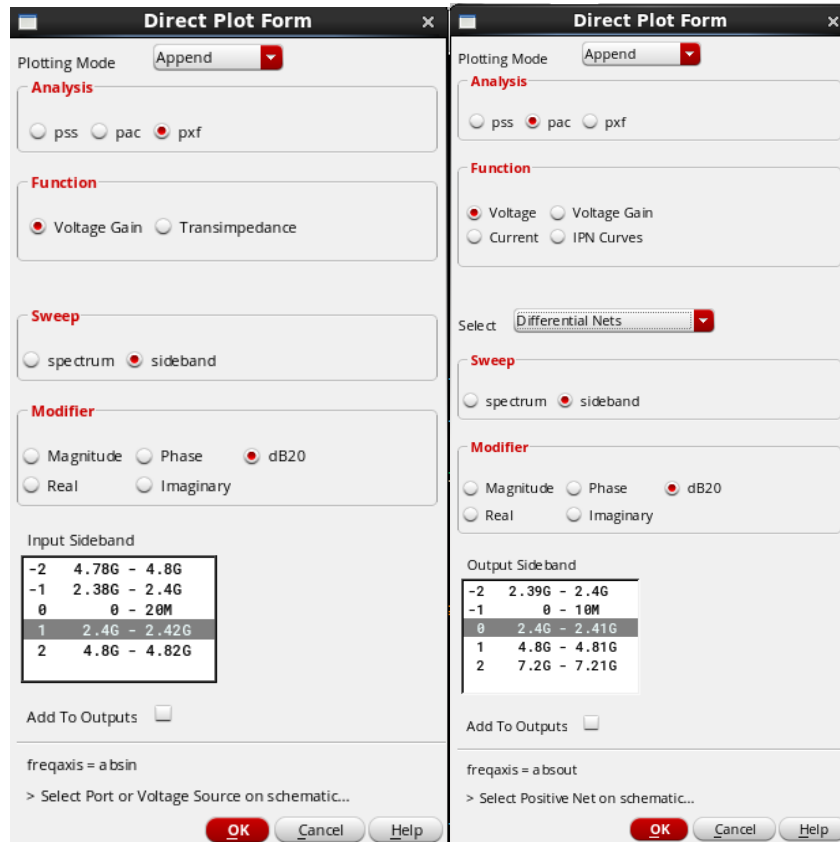


Fig. 22

Fig. 23

- The simulation results in this section are much less than the typical measured values. What do you think is the reason? If you were to manufacture this circuit, would the leakage be this low?

#### 10- Noise Figure

The noise performance of a mixer is measured by the degradation of the signal to noise power ratio (SNR) after mixing. The input SNR is measured at RF frequency while the output SNR is calculated at IF frequency. Mixing translates down both signal and noise at both the desired channel and its image channel. In the cases where the image frequency does not contain a useful signal, the noise power is doubled after mixing while the signal power remains constant (both referred to the input). Therefore, even a noiseless mixer

has 3 dB NF. Direct conversion mixer, where IF is zero, is an exception because the image of the desired signal is itself. Therefore, in this special case the signal power and the noise power go through the same process and SNR remain unchanged, i.e.  $NF=0$ . In practice, transistors and resistors of the mixer add noise and increase NF, however we can still say that double side-band NF ( $NF_{DSB}$ ) is 3 dB lower than single side-band NF ( $NF_{SSB}$ ).

To simulate the noise performance of a mixer, PSS and Pnoise analysis are used together.

- Configure the PSS simulation form as depicted in Fig. 24.
- Configure the Pnoise setup form as Fig. 25 illustrates. Select IF port as “output port” and RF port as “input port”.
- Run the simulation.
- From Results/Direct Plot/Main Form choose Pnoise and plot NF,  $NF_{DSB}$ , and  $NF_{SSB}$ . Check the box to calculate “integrated noise over bandwidth” (Fig. 26) .

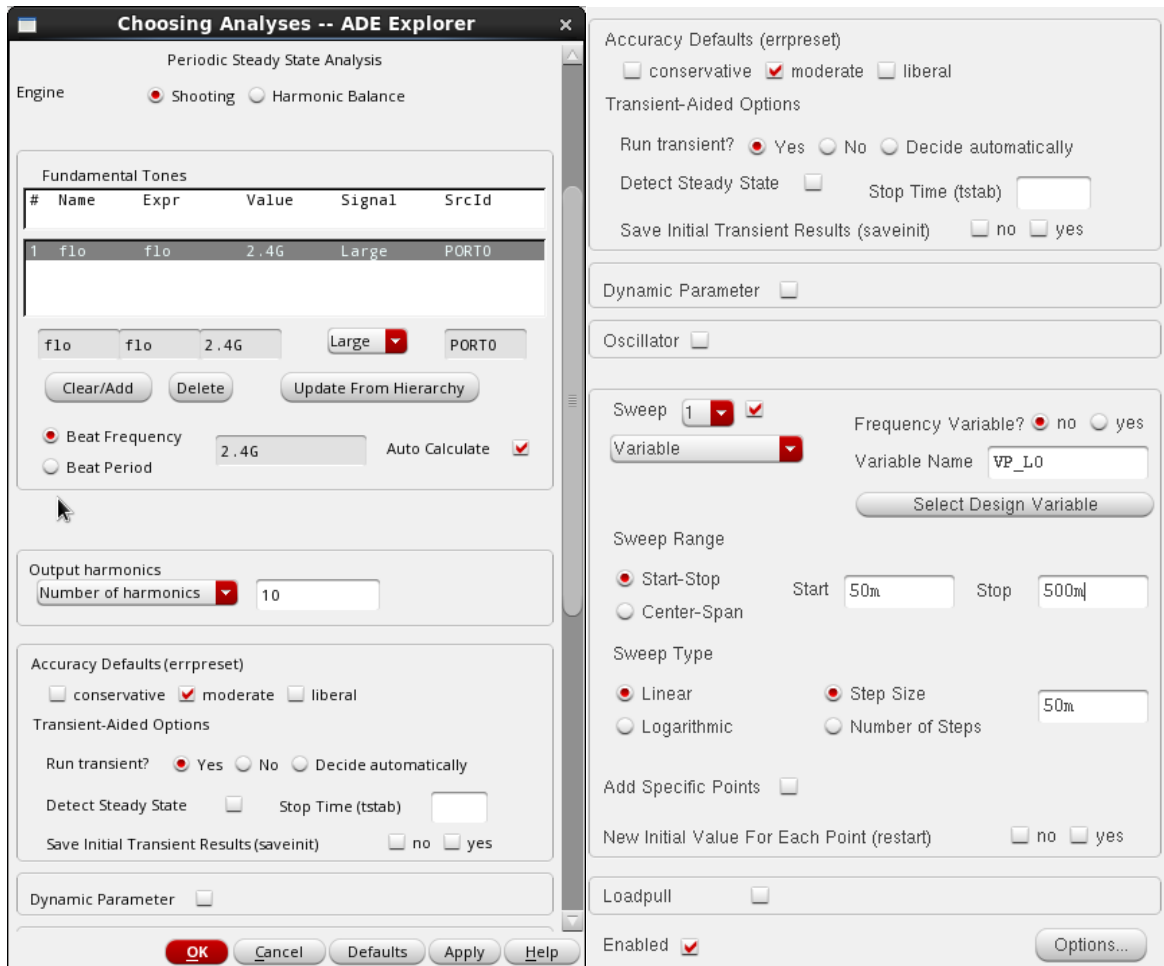


Fig. 24



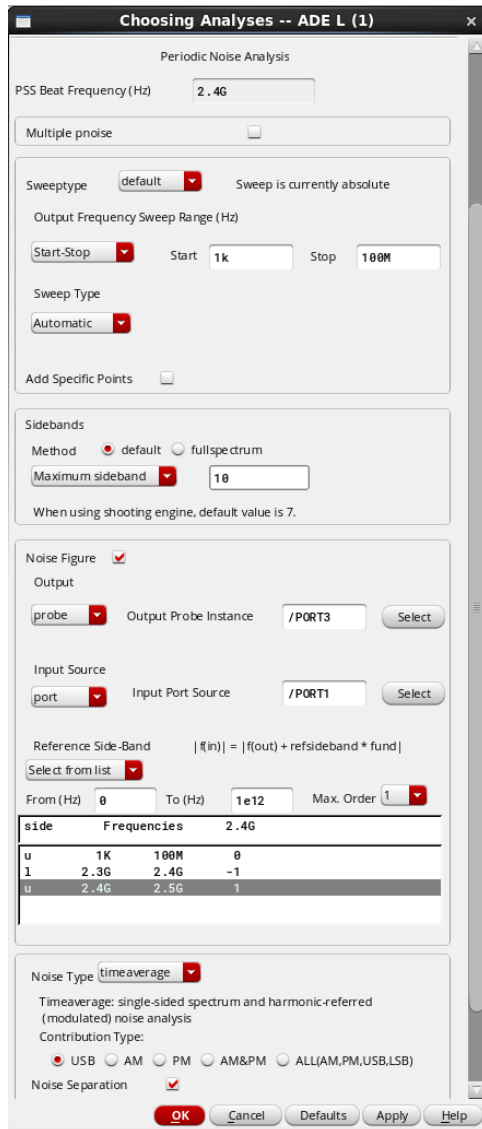


Fig. 25

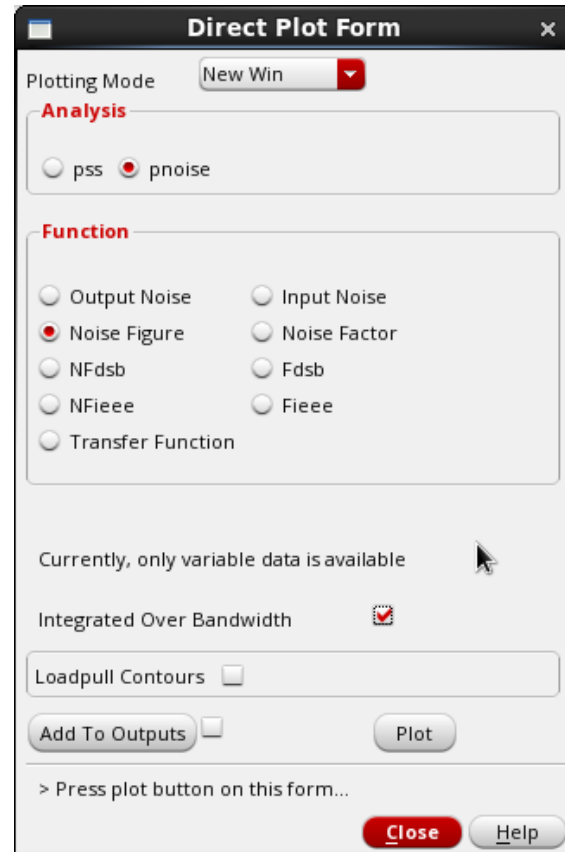


Fig. 26

- Compare the result when using NFdsb.
- You can investigate the dominant noise sources by turning on the “noise separation” option in Pnoise analysis.