Advanced Digital IC Design

A/D Conversion and Filtering for Ultra Low Power Radios

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Why is this important?

A/D Conversion

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A/D converters introduction

- White noise approximation accuracy
  - Accurate for rapidly changing and random input signals
  - Increases with the number of bits in the quantizer
  - Least accurate for 1-bit quantizers but used anyway

- Maximum theoretical SNR for an N-bit ideal ADC
  \[ SQNR_{\text{dB}} = 6.02N + 1.76 \]

Oversampling A/D Converters

Basic principle of oversampling
Oversampling A/D Converters

**ΔΣ modulation for A/D conversion**

General ΔΣ-modulator

Linear model

\[ Y(z) = STF(z)X(z) + NTF(z)E(z) \]

Signal Transfer Function: \( STF(z) \)

Noise Transfer Function: \( NTF(z) \)

Oversampling A/D Converters

- SQNR controlled by
  - Order of the loop filter
  - Number of bits in the quantizer
  - Oversampling ratio

\( \Delta \Sigma \) ADCs vs. Nyquist ADCs
- High resolution obtained with few bits in the quantizer
- Mismatch in the quantizer suppressed by the loop
- Additional analog blocks in the loop filter
- Feedback loop → stability issues

Oversampling A/D Converters

Continuous Time ΔΣ-modulators

Sampling operation moved after the loop filter
Implicit anti alias filtering inherited

Ultra Low Power Receiver

- RF front end
- ΔΣ modulator
- Decimation filters
- Matching filters
- Analog decoder

Specifications
- Supply voltage: 900 mV
- Maximum input signal: 200 mV diff
- Power consumption: 300 μW
- Bandwidth: 125 kHz
- SNDR target: 70 dB
- Sampling frequency: 4 MHz

Low Power Circuits, Dejan and Yasser, 2012-02-14
A third order, 3-bit CT ΔΣ modulator has been implemented in CMOS

DAC mismatch

In multi-bit DACs, mismatch between DAC cells causes nonlinearities
- Digital correction techniques are used to correct for mismatch
- One successful correction technique is called Data Weighted Averaging (DWA)

DWA algorithm

Implementation of the DWA algorithm

Layout

Decoupling capacitors
Loop filter
Flash ADC
DWA
Output buffers
Measurement Results

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Technology</td>
<td>65nm CMOS</td>
</tr>
<tr>
<td>Supply voltage</td>
<td>900 mV</td>
</tr>
<tr>
<td>Active area</td>
<td>0.17 mm²</td>
</tr>
<tr>
<td>Signal bandwidth</td>
<td>125 kHz</td>
</tr>
<tr>
<td>Maximum input amplitude (-3dBFS)</td>
<td>200 mV (differential)</td>
</tr>
<tr>
<td>Clock frequency</td>
<td>4 MHz</td>
</tr>
<tr>
<td>Power consumption</td>
<td>380 pW</td>
</tr>
</tbody>
</table>

Results summary

Chip photo

SNR/SNDR vs. amplitude

- Peak SNDR = 70 dB @ -2.5 dBFS
- Peak SNR = 74 dB @ -1.7 dBFS

Conclusions

- ΔΣ modulators achieve high resolution using a few bits in the quantizer
- Multi-bit CT ΔΣ are sensitive to errors in the feedback DAC – Digital correction needed
- ΔΣ modulation Usually employed for moderate resolution but pushing towards higher resolutions and higher frequencies
Motivation and Sub-VT Basics

- Energy minimum operating voltage in sub-VT.
- Circuit operates at critical path speed, idle time is minimized.
- Delay increases exponentially.

Main Sources of Leakage

- Gate leakage
  - Tunneling of electrons from bulk and the overlapped p-n diffusion region into the gate through the thin oxide.

- P-N junction leakage
  - Flow of the minority carriers drifting from the reverse p-n junction between both source and drain to bulk (BTBT).

- Sub-threshold leakage
  - Caused by diffusion of carriers in weak inversion region.

Normalized average leakage in Inverter Circuitry using RBB

- At $V_{DD} = 0.1V$, we get 6% leakage reduction.
- At $V_{DD} = 0.3V$, we get 16% leakage reduction.
- At $V_{DD} = 1.2V$, we get 20% leakage reduction.
High-level Modeling in the Sub-\( V_T \) Domain [1]

- No standard/commercial flow available which simply characterizes designs with \( V_{DD} \leq 400 \) mV.
- High-level Energy Model
  - Conventional EDA tools.
  - SPICE-accurate in a fraction of SPICE simulation time.
  - Any RTL design.
  - Standard- and full-custom based designs.

Energy Model Application

- SVT cells have least energy dissipation.

Effect of Switching Activity on EMV [3]

- High switch activity shifts EMV to lower voltages.
- Sub optimal operational frequency leads to high energy dissipation.

Energy-Throughput Analysis w.r.t. different \( V_T \)'s

- Energy vs \( V_{DD} \)
  - HVT cells have least energy dissipation.
- Energy vs Throughput
  - SVT cells have least energy dissipation for moderate throughput requirements.
Dual-\(V_T\) Implementations [5]

- Energy vs Voltage
  - No advantage is observed for \(H+S\) combination.

Standard-Cell-Based Memory [6]

- SRAM macro-cells become significantly larger due to the need for 8T or 10T [7] bit-cells
- Additional assist circuits required for reliable sub-\(V_T\) operation (sense-amplifier).

Standard Cell Based Memories (SCM) [7]

- Energy vs Voltage
  - Flip-Flop based implementation are a bit faster.

Energy Analysis of SCMs

- Energy vs Voltage
  - Latch based multiplexer clock-gate architecture for \(R = 256\), \(C = 128\) and for \(R = 128\), \(C = 256\). The \(\Delta\) corresponds to [8], a hard macro SRAM memory.


Reliability Analysis

- Eye diagram of the latch used in the SCM architecture for $V_{DD}=0.4V$ and $V_{DD}=0.25V$.
- 1000-point Monte Carlo circuit simulation assuming within die process parameter variations.
- Operation is still possible below $V_{T}$, but the SNMs are small and reliability starts to become critical at 250mV.

Conclusions

- A high-level energy flow for sub-$V_{T}$ domain characterization was presented.
  - Enables architectural design space exploration.
- Dual-$V_{T}$ implementations may not be beneficial.
- SCM are promising option for sub-$V_{T}$ memories.
- Proper knowledge of input stimuli is crucial for system specification.