EITF35: Introduction to Structured VLSI Design

Introduction to FPGA design

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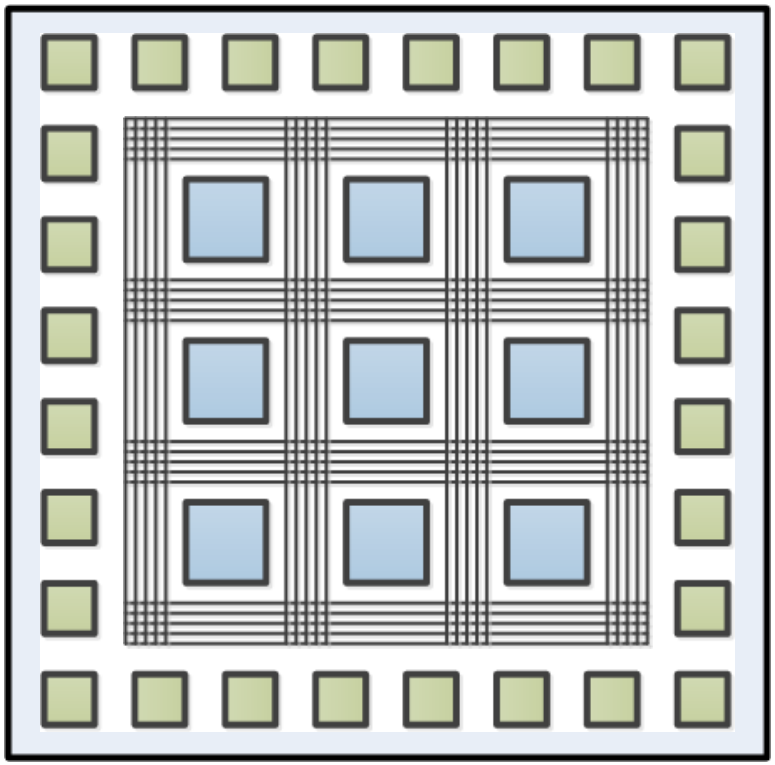
Slides from Chenxin Zhang and Steffan Malkowsky

WWW.FPGA

- What is FPGA?
  - Field Programmable Gate Array

Configurable logic blocks



Interconnects

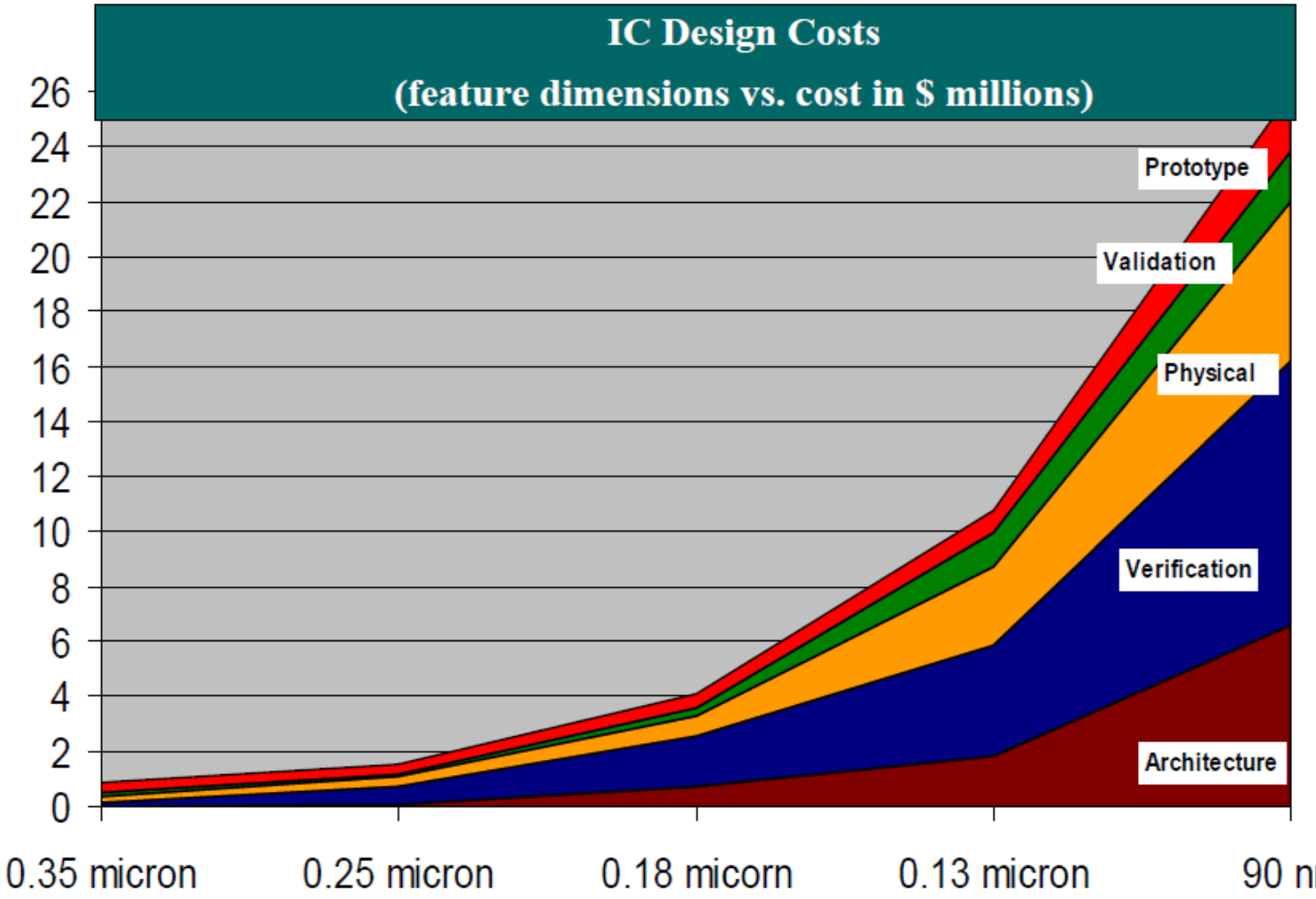
Configuration memory

IO blocks

WWW.FPGA

- What is FPGA?
  - Field Programmable Gate Array
  - Configurable logic blocks + interconnects + IOs + memory
- Why do we use it?
  - High performance & Flexible
  - Shorter time to market

WWW.FPGA


IC Design Costs
(feature dimensions vs. cost in $ millions)
26
24
22
20
18
16
14
12
10
8
6
4
2
0
Prototype
Validation
Physical
Verification
Architecture
0.35 micron
0.25 micron
0.18 micorn
0.13 micron
90 nm

WWW.FPGA

- What is FPGA?
  - Field Programmable Gate Array
  - Configurable logic blocks + interconnects + IOs + memory
- Why do we use it?
  - High performance & Flexible
  - Shorter time to market
- Where do we use it?
  - Prototyping
  - Computer vision
  - Medical imaging
  - Software-defined radio
  - …

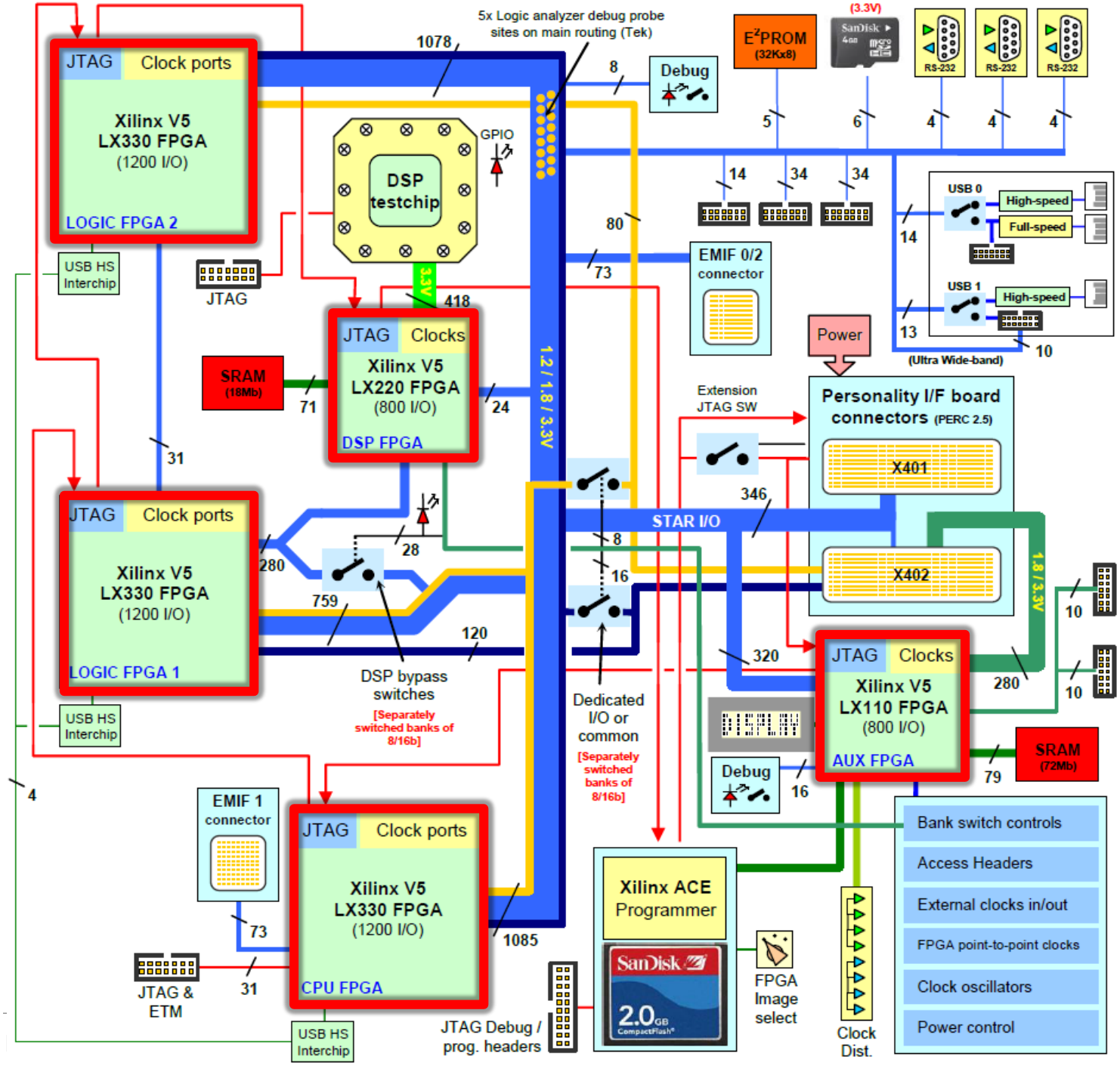
FPGA vs. Microprocessor

	Intel Itanium 2	Xilinx Virtex-II Pro (XC2VP100)
Technology	0.13 µm	0.13 µm
Clock speed	1.6 GHz	180 MHz
Internal memory bandwidth	102 GBytes/S	7.5 TBytes/S
# Processing units	5 FPU (2 MACs+1 FPU) 6 MMU 6 Integer units	212 FPU or 300+Integer units or …
Power consumption	130 W	15 W
Peak performance	8 GFLOPs	38 GFLOPs
Sustained performance	~2GFLOPs	~19 GFLOPs
IO/External memory bandwidth	6.4 GBytes/S	67 GBytes/S

(Courtesy: Nallatech)

FPGA devices

- Manufactures:
  - **Xilinx**: Virtex, Kintex, Artix, Spartan
  - **Altera**: Cyclone, Arria, Stratix
  - Lattice Semiconductor: flash, low power
  - Microsemi (Actel): antifuse, mix-signal
  - Achronix: high speed
  - QuickLogic: application-specific (handheld)


5x Logic analyzer debug probe sites on main routing (Tek)
1078
JTAG
Clock ports
Xilinx V5
LX330 FPGA
(1200 I/O)
LOGIC FPGA 2
USB HS Interchip
JTAG
DSP testchip
GPIO
3.3V
418
JTAG
Clocks
Xilinx V5
LX220 FPGA
(800 I/O)
DSP FPGA
SRAM
(18Mb)
71
24
1.2 / 1.8 / 3.3V
31
JTAG
Clock ports
Xilinx V5
LX330 FPGA
(1200 I/O)
LOGIC FPGA 1
USB HS Interchip
280
28
759
120
DSP bypass switches
[Separately switched banks of 8/16b]
4
EMIF 1 connector
73
JTAG & ETM
31
JTAG
Clock ports
Xilinx V5
LX330 FPGA
(1200 I/O)
CPU FPGA
USB HS Interchip
1085
JTAG Debug / prog. headers
8
Debug
80
73
EMIF 0/2 connector
E²PROM
(32Kx8)
(3.3V)
SanDisk
4GB
RS-232
RS-232
RS-232
5
6
4
4
4
14
34
34
USB 0
High-speed
Full-speed
USB 1
High-speed
14
13
10
(Ultra Wide-band)
Power
Extension JTAG SW
Personality I/F board connectors (PERC 2.5)
X401
X402
346
STAR I/O
8
16
1.8 / 3.3V
10
10
280
320
JTAG
Clocks
Xilinx V5
LX110 FPGA
(800 I/O)
AUX FPGA
SRAM
(72Mb)
79
DISPLAY
Debug
16
Dedicated I/O or common
[Separately switched banks of 8/16b]
Xilinx ACE Programmer
SanDisk
2.0GB
CompactFlash
FPGA Image select
Clock Dist.
Bank switch controls
Access Headers
External clocks in/out
FPGA point-to-point clocks
Clock oscillators
Power control

Some FPGA b

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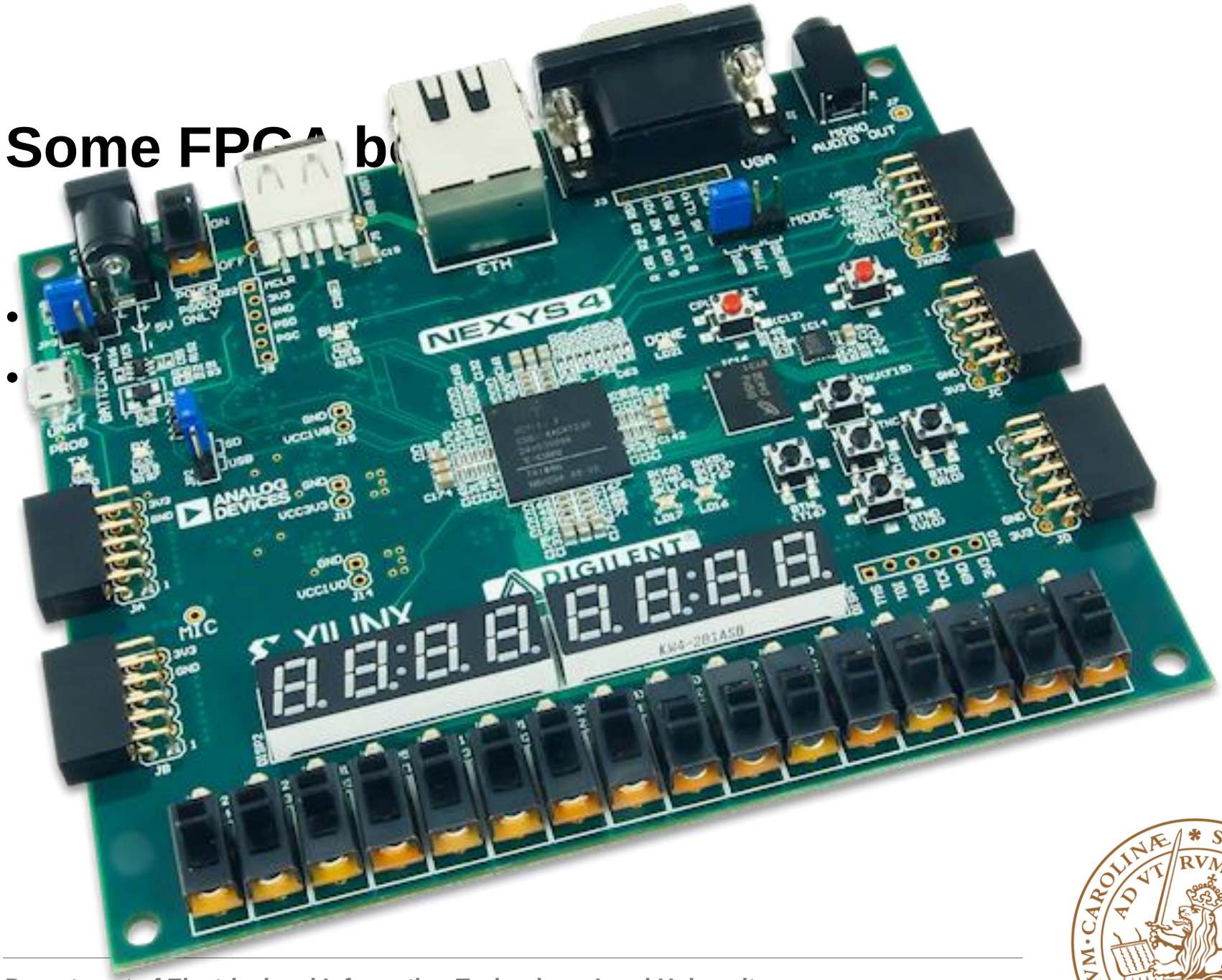
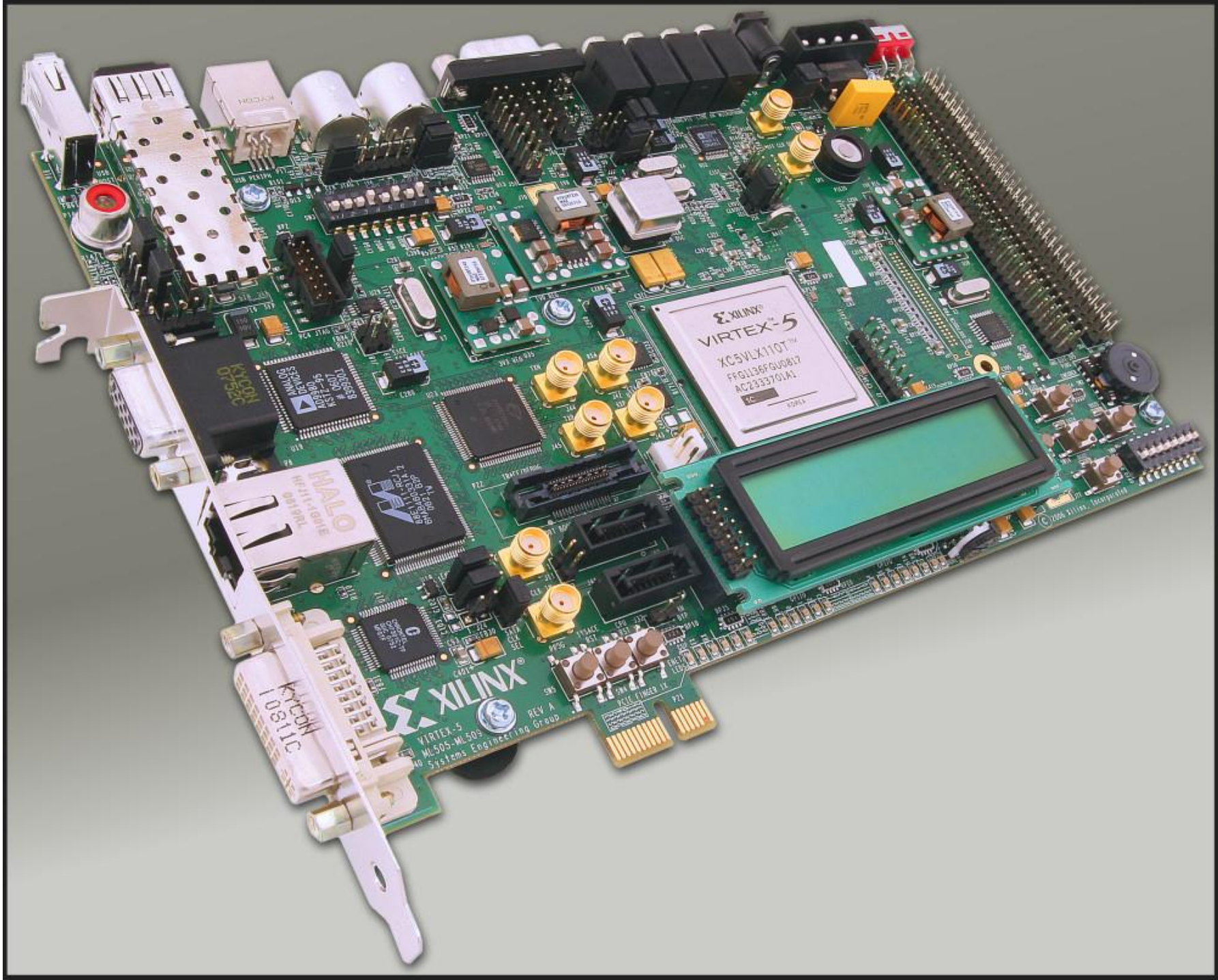
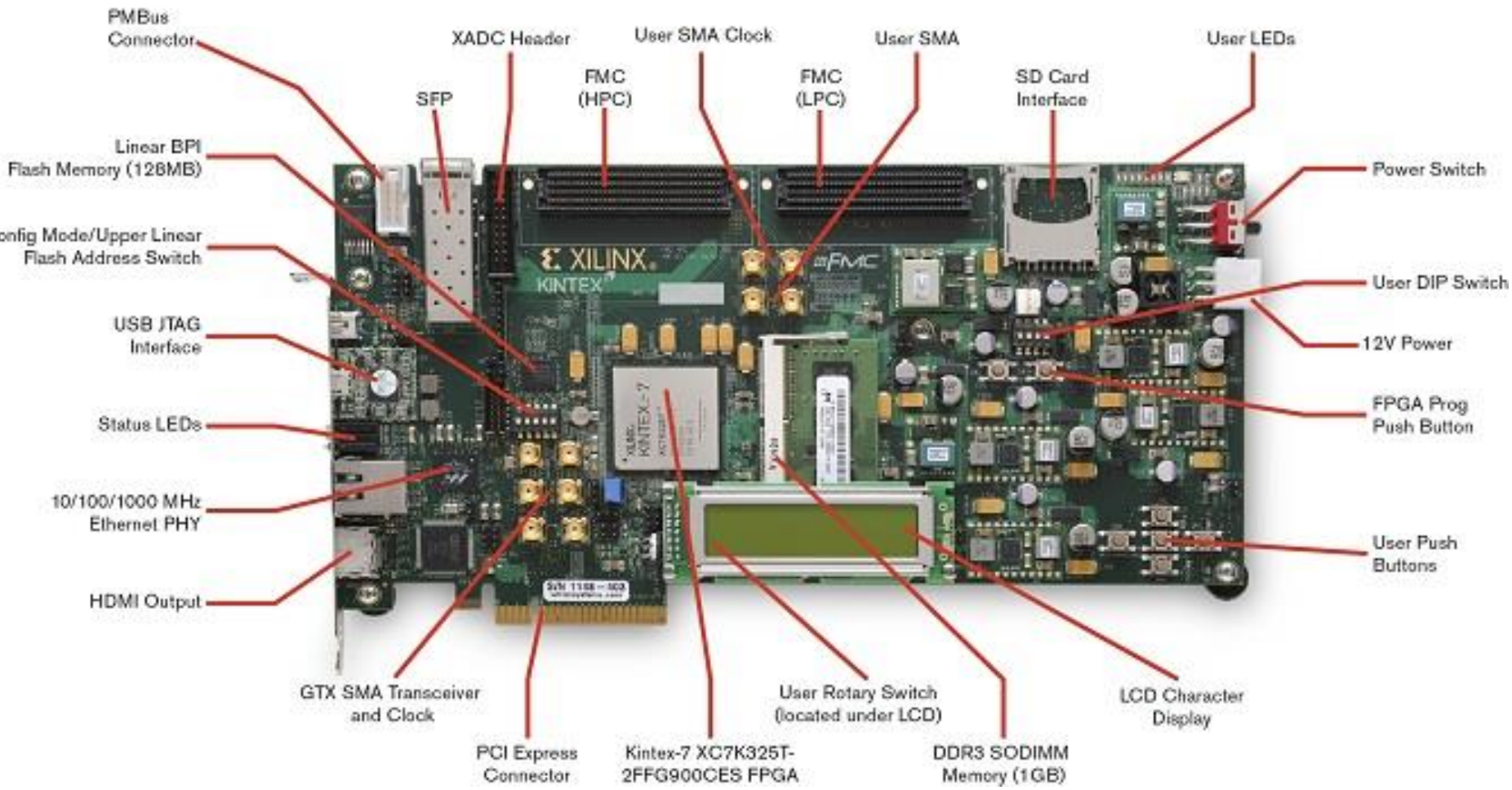
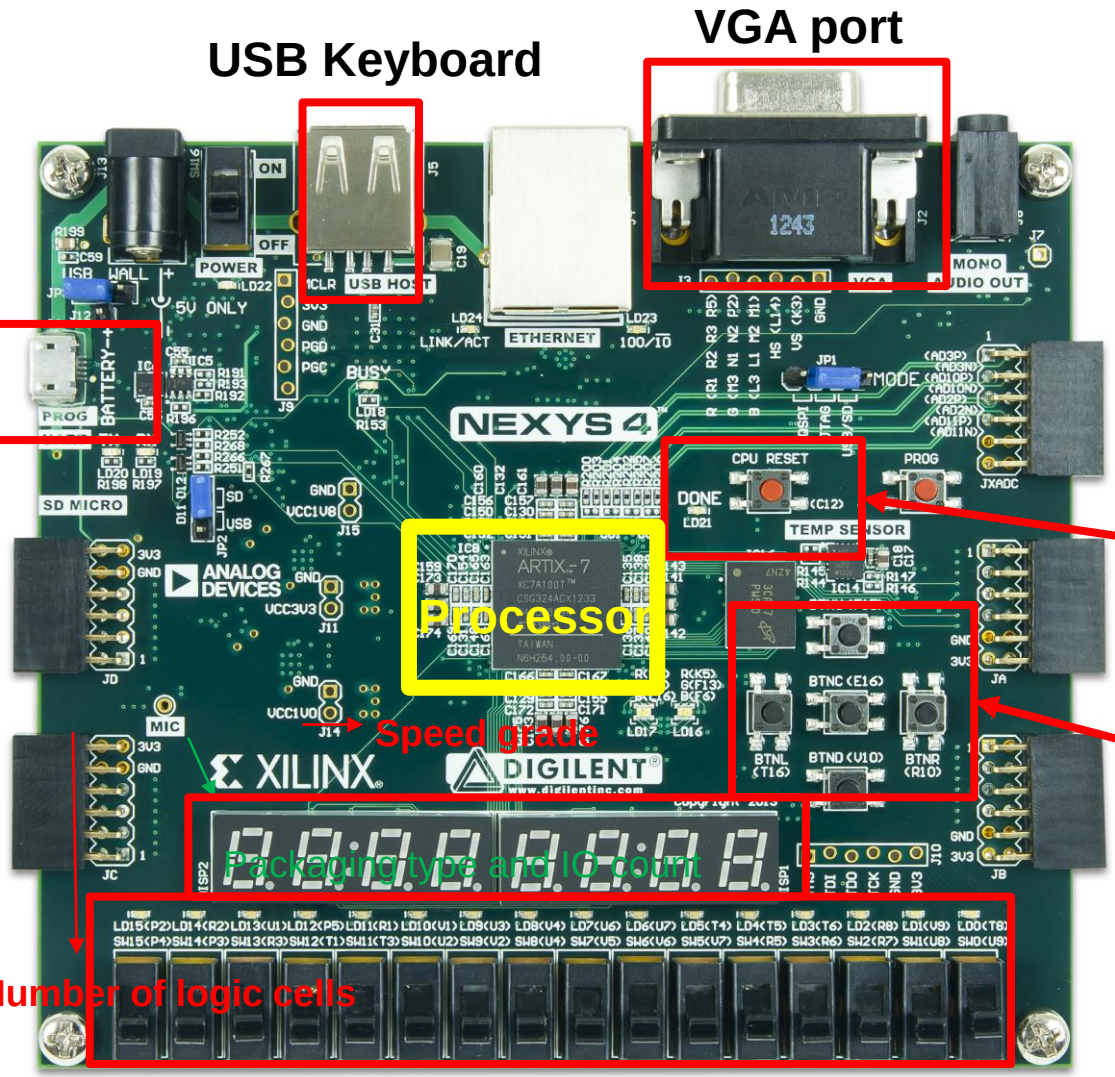



XILINX
VIRTEX-5
XC5VLX110T
FFG1136FGU0617
AC2333701A1
XILINX
VIRTEX-5
ML505-ML509
Systems Engineering Group
REV A


PMBus Connector
XADC Header
User SMA Clock
User SMA
User LEDs
SFP
FMC (HPC)
FMC (LPC)
SD Card Interface
Linear BPI Flash Memory (128MB)
Power Switch
onfig Mode/Upper Linear Flash Address Switch
User DIP Switch
USB JTAG Interface
12V Power
FPGA Prog Push Button
Status LEDs
10/100/1000 MHz Ethernet PHY
User Push Buttons
HDMI Output
GTX SMA Transceiver and Clock
User Rotary Switch (located under LCD)
LCD Character Display
PCI Express Connector
Kintex-7 XC7K325T-2FFG900CES FPGA
DDR3 SODIMM Memory (1GB)

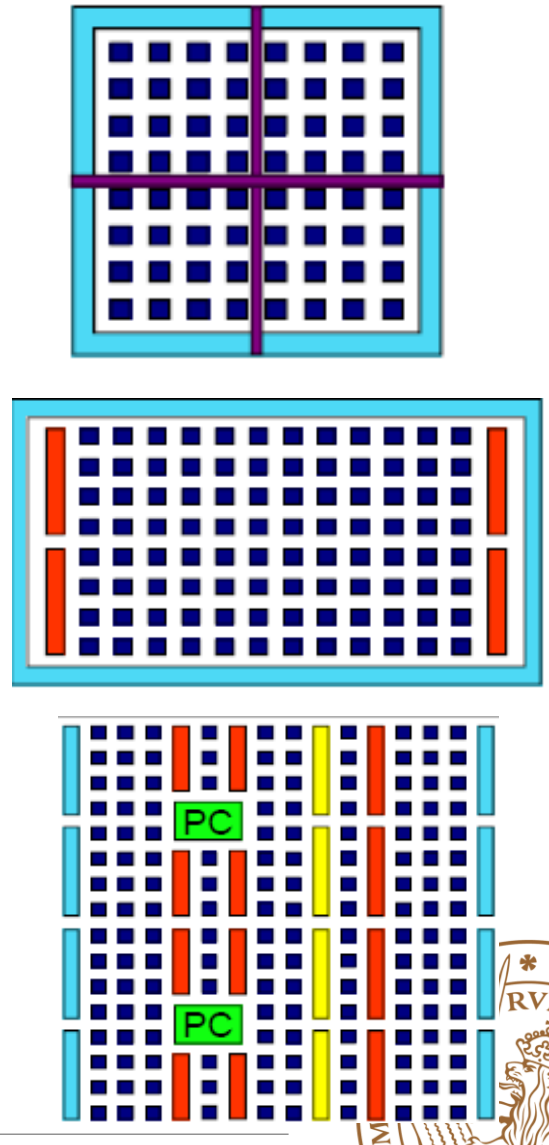
Some FPGA boards

- ERICSSC
- Xilinx Virt
  - http://ww
- Xilinx Kin
  - http://ww
- Nexys™ 4
  - http://ww
  - FPGA P
    - XC7
      - Artix-7 serie



FPGA architectures

- Early FPGAs
  - N x N array of unit cells (CLB + routing)
  - Configurable Logic Blocks
  - Special routing along center axis
- Next Generation FPGAs
  - M x N unit cells
  - Small block RAMs around edges
- More recent FPGAs
  - Added block RAM arrays
  - Added multiplier cores
  - Added processor cores



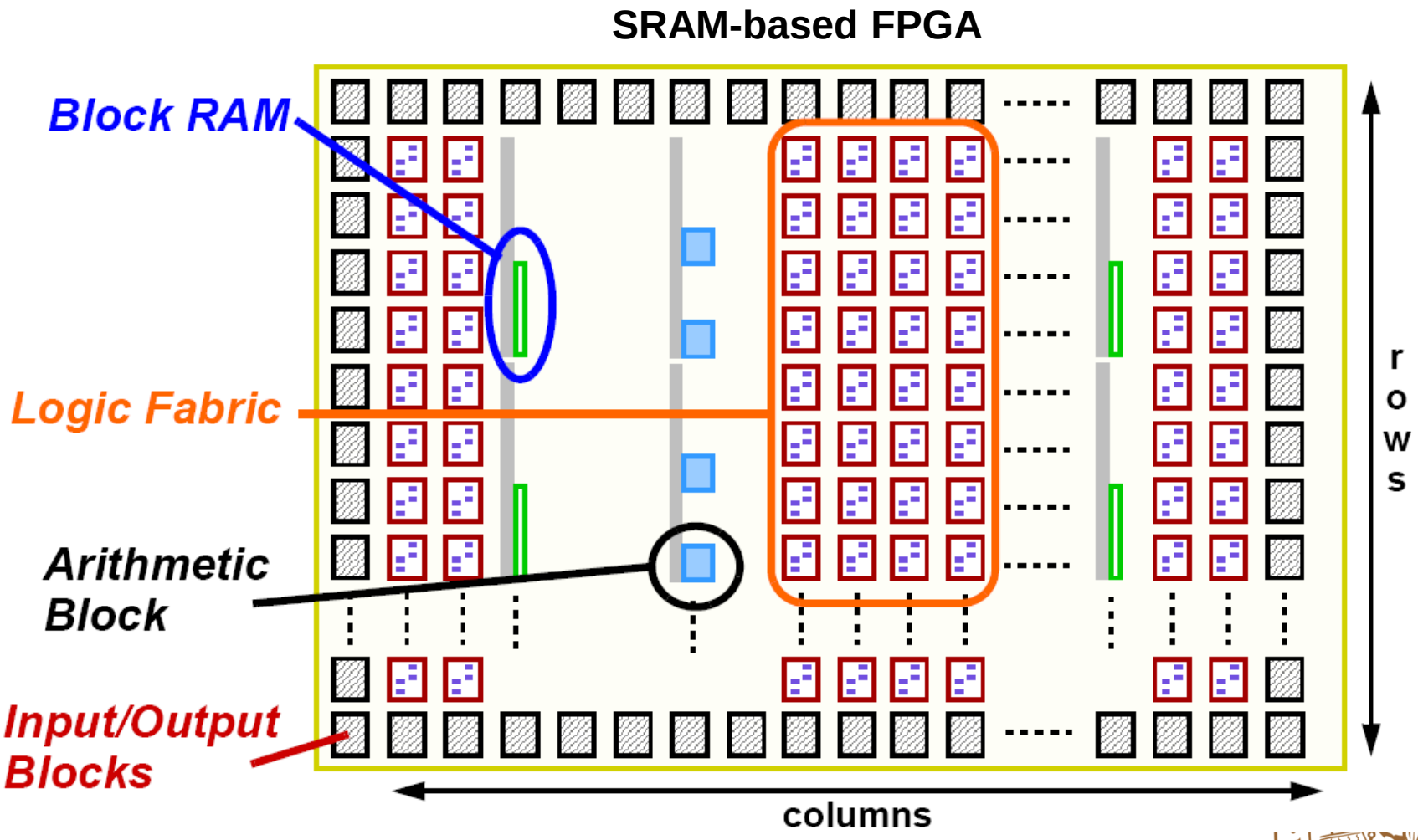
FPGA architecture trends

- Memories
  - Single & Dual-port RAMs
- Digital Signal Processor Engines
- Embedded Processors
  - Hardcore (dedicated processors)
  - Soft core (synthesized from a HDL)
- High speed/performance I/O connectivity
  - PCIe interface block
  - I/O transceiver
  - Gigabit Ethernet
  - HPC and LPC interfaces
- Clock management blocks

Programming technology

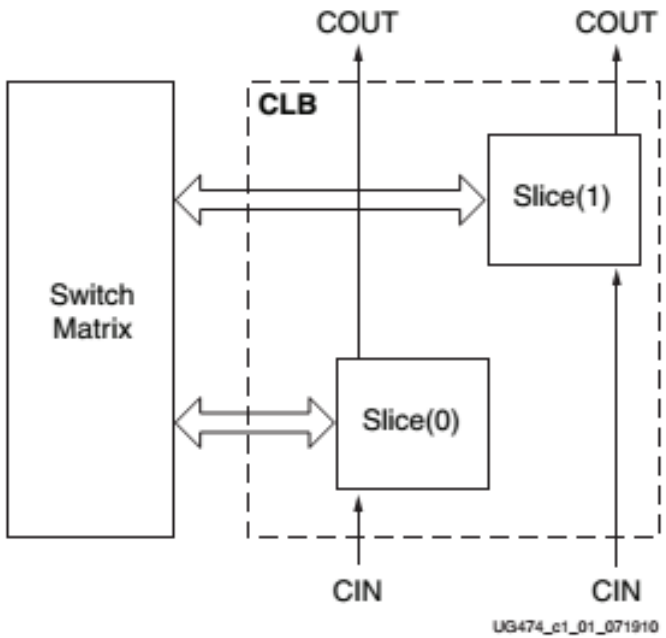
Feature	SRAM	Antifuse	Flash/E2PROM
Technology	State-of-the-art	One or more generations behind	One or more generations behind
Reprogrammable	Yes (in system)	No	Yes (in system or offline)
Reprogramming speed	Fast	---	3x slower than SRAM
Volatile	Yes	No	No
Instant-on	No	Yes	Yes
Security	Acceptable	Very Good	Very Good
Size of Config. Cell	Large (Six transistors)	Very small	Medium-small (Two transistors)
Power consumption	Medium	Low	Medium

Xilinx FPGA architecture



Configurable logic block (CLB) (I)

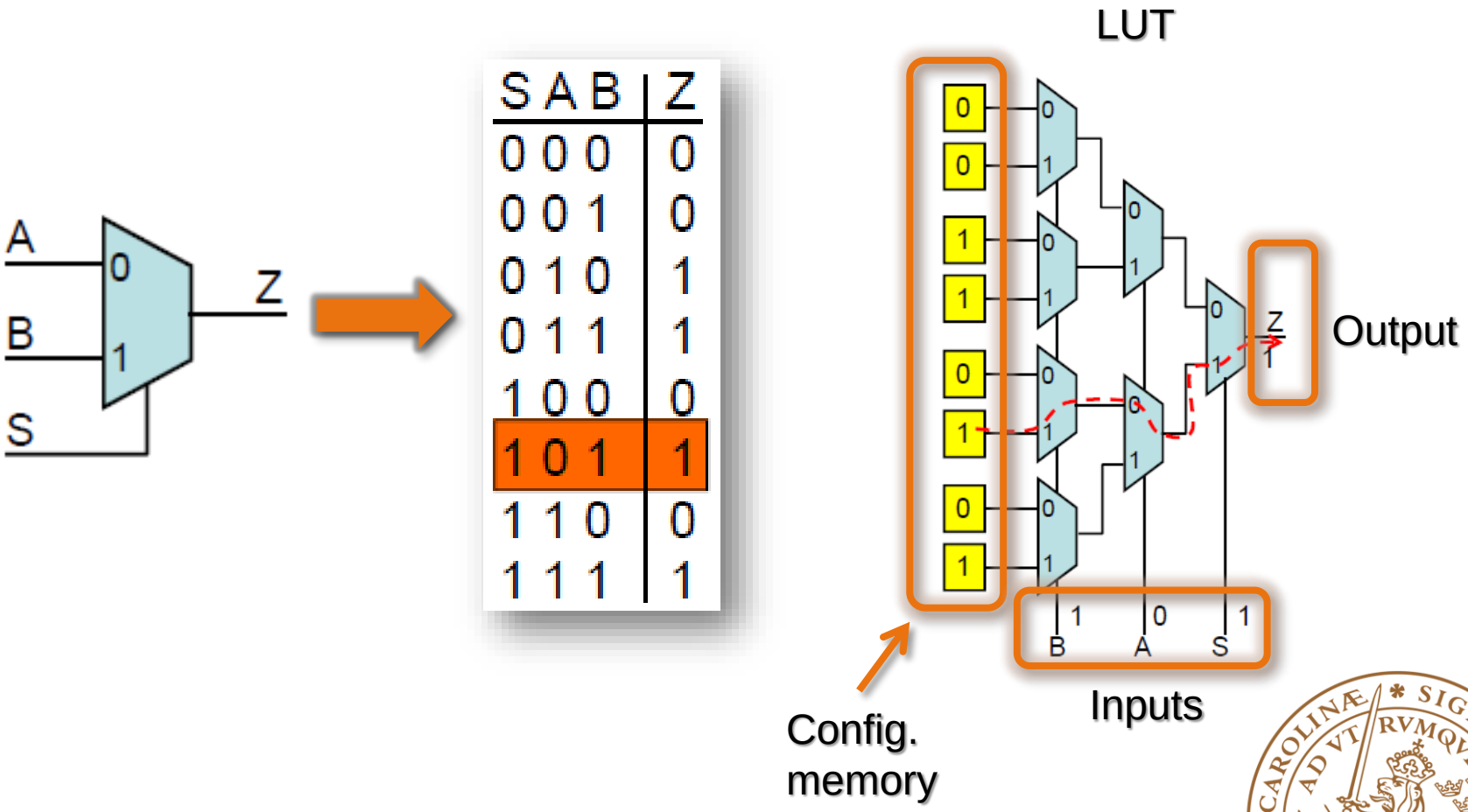
- One CLB contains two slices (7 series Xilinx FPGA)



Configurable logic block (CLB) (II)

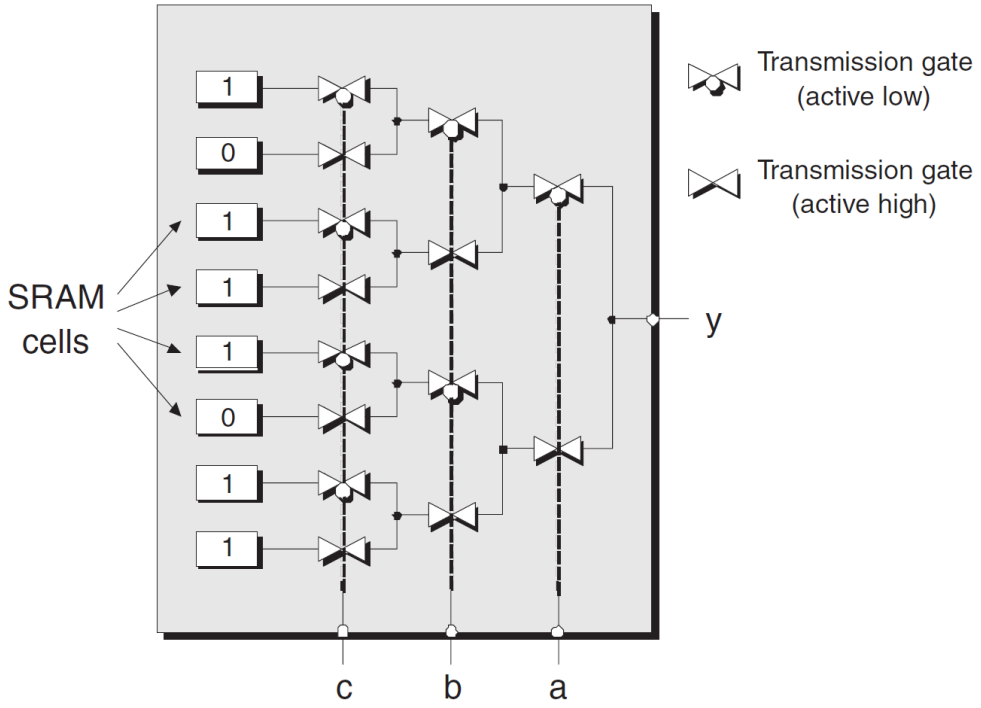
- One CLB contains two slices
- Each slice:
  - Four Look-up tables (LUTs)
  - Eight D Flip-Flops (DFFs)
  - Multiplexers and arithmetic gates
  - Carry logic
- 2/3 of all slices are SLICEL and 1/3 SLICEM
  - Distributed RAM and Shift registers in SLICEM
  - Higher Interconnect density in 7 series

Look-up table (LUT) (I)



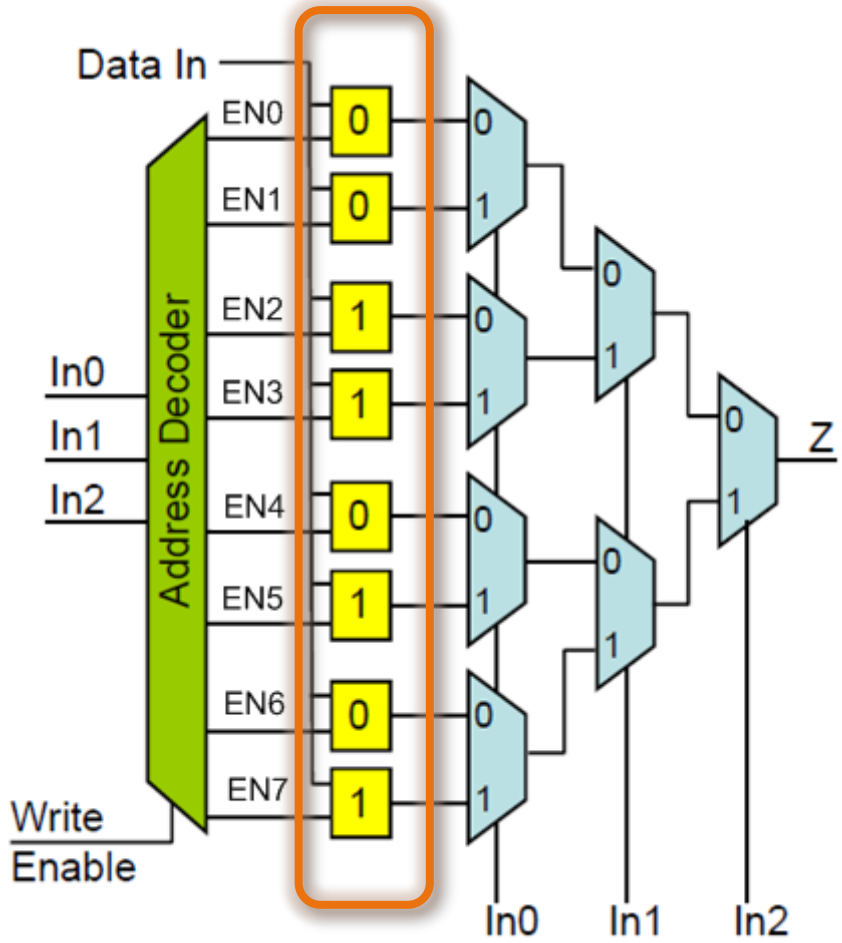
Look-up table (LUT) (II)

- Inputs are used as a pointer into a LUT.
- Decoded using a hierarchy of transmission-gate MUXs.
- Transmission-gate: “pass” or “high-impedance”.

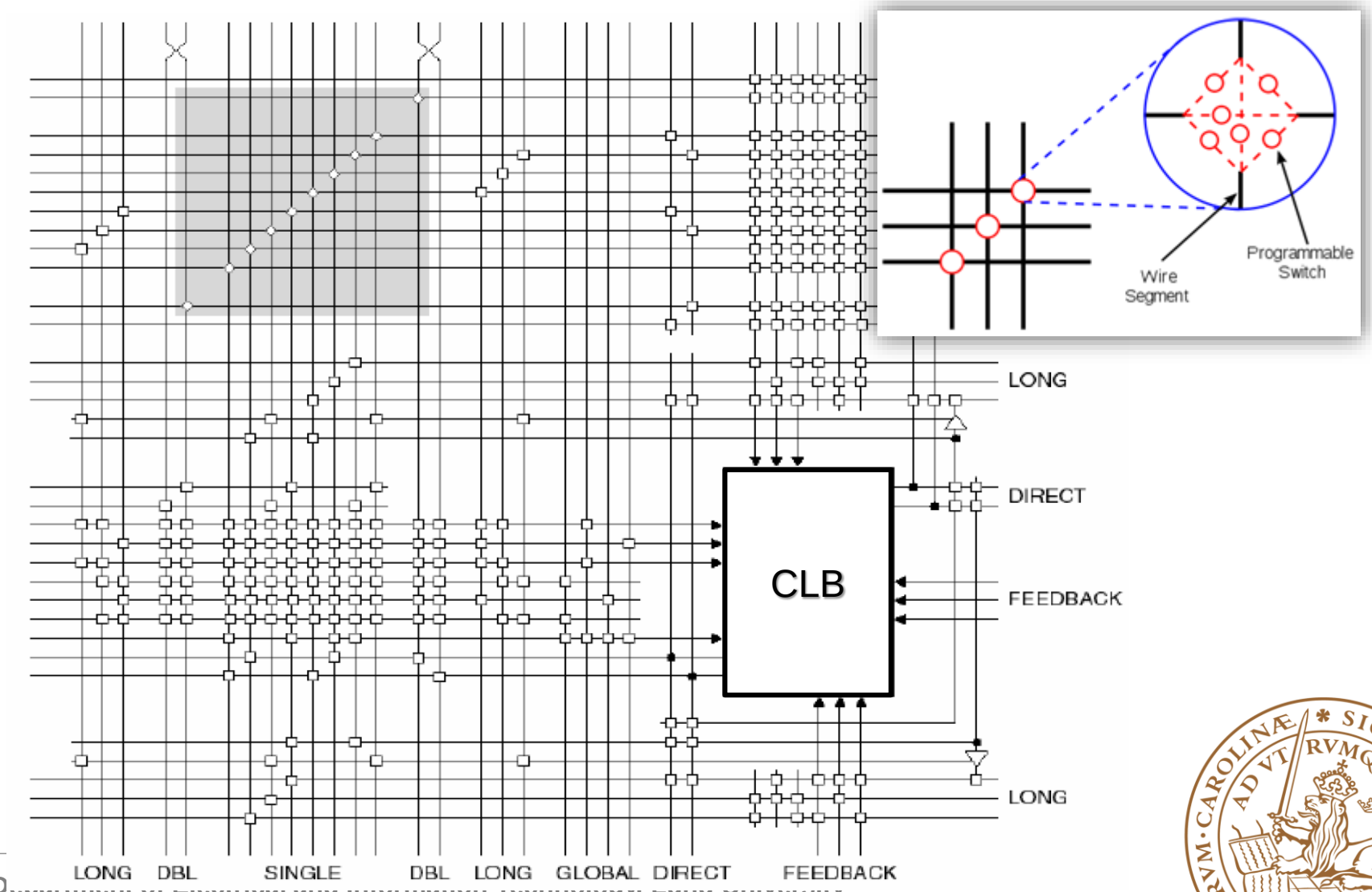


LUT based RAM (Distributed RAM)

- Normal LUT performs “read” operation.
- For “write” operation, address decoders + write enable.
- Can be concatenated to created larger RAMs.
- Can also be used as shift registers (some of the LUTs).

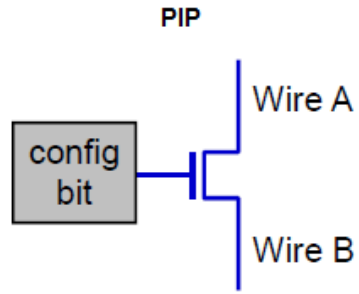


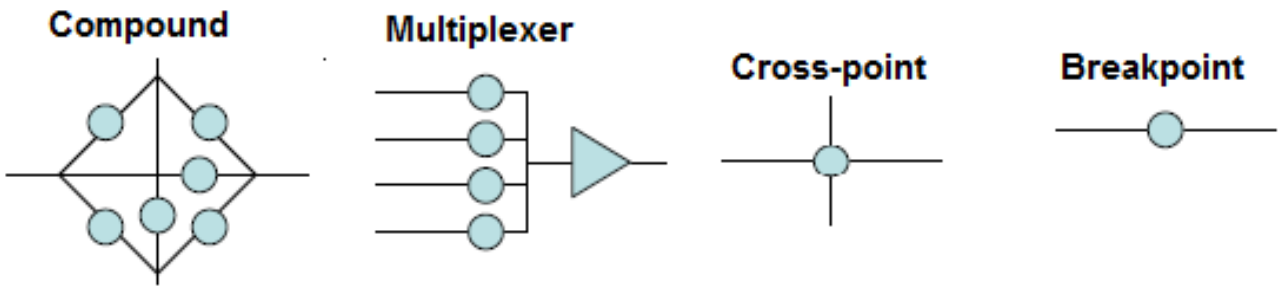
Programmable Interconnects (I)



Programmable Interconnects (II)

- Programmable swich, also called programmable interconnect points (PIP).
- Implemented using transmission gates.
- Several types of PIPs:





Xilinx Artix-7 FPGA

- XC7A100T:
  - ~8000 CLBs
  - ~5000 kb of BRAMs
  - ~1200 Kb Distributed RAM
  - 240 DSP units

Table 1-1: **Artix-7 FPGA CLB Resources *(Cont'd)***

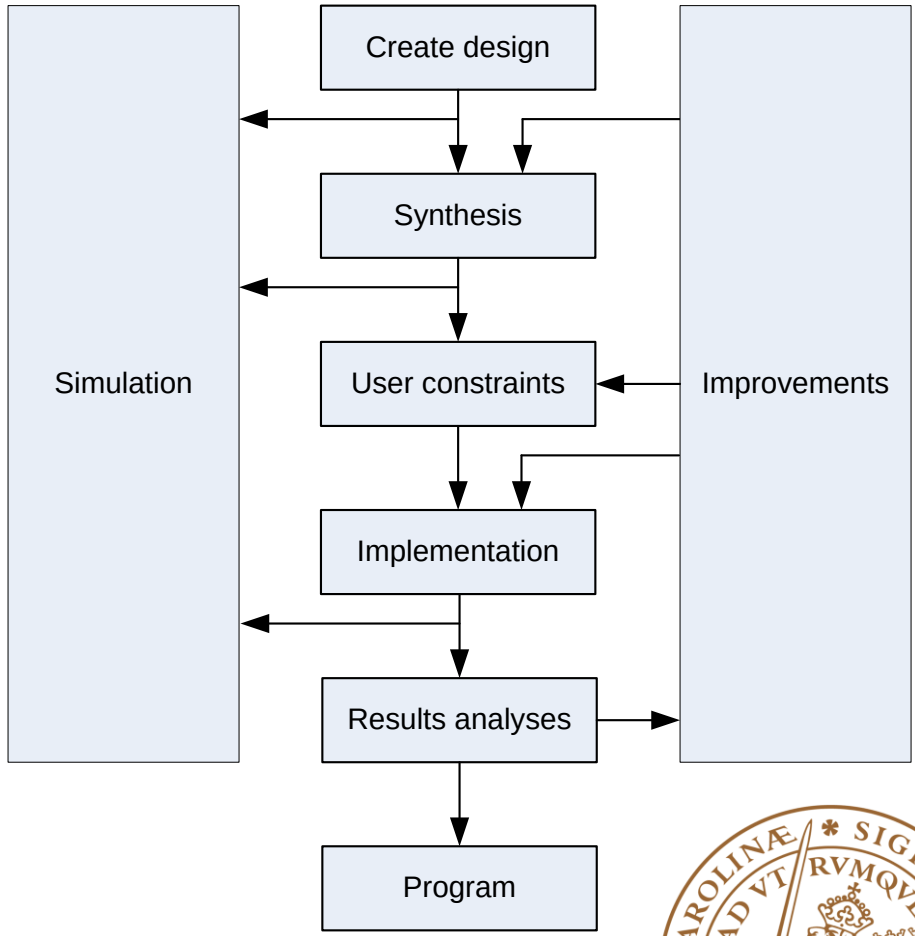
Device	Slices(1)	SLICEL	SLICEM	6-input LUTs	Distributed RAM (Kb)	Shift Register (Kb)	Flip-Flops
7A50T	8,150	5,750	2,400	32,600	600	300	65,200
7A75T	11,800(2)	8,232	3,568	47,200	892	446	94,400
7A100T	15,850	11,100	4,750	63,400	1,188	594	126,800
7A200T	33,650	22,100	11,550	134,600	2,888	1,444	269,200

Notes:

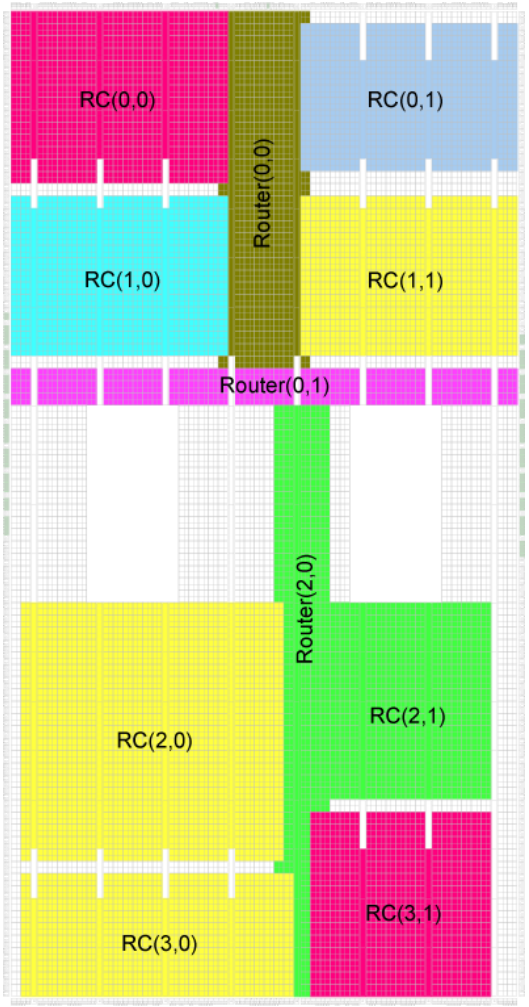
1. Each 7 series FPGA slice contains four LUTs and eight flip-flops; only SLICEMs can use their LUTs as distributed RAM or SRLs.
2. Number of slices corresponding to the number of LUTs and flip-flops supported in the device.

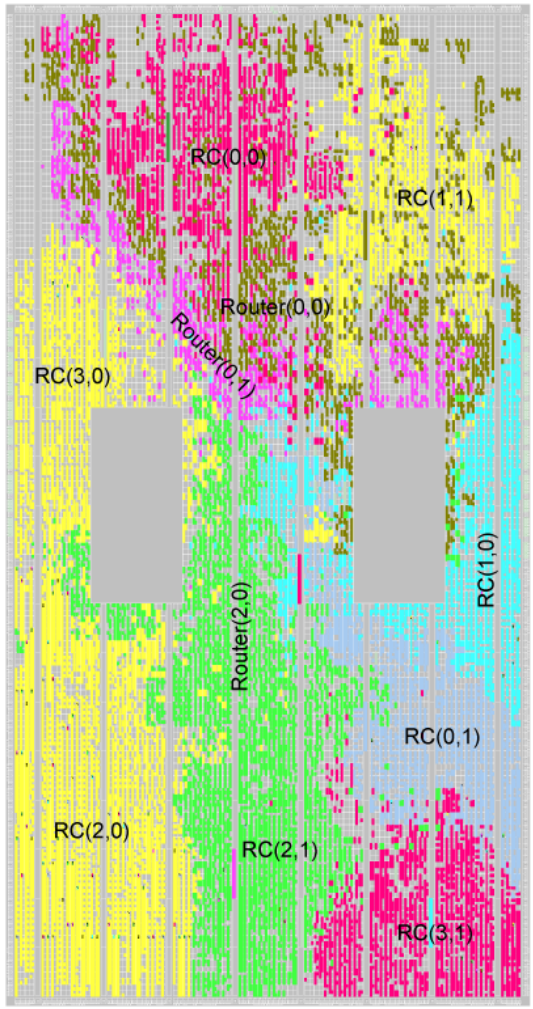
FPGA Design flow

- Synthesis
  - Parses HDL design
  - Infers Xilinx primitives
  - Generates design netlist
- Translate
  - Merges incoming netlists and constraints into a design file
- Map
  - Maps (places) design into the available resources on the target device
- Place and Route
  - Places and routes design

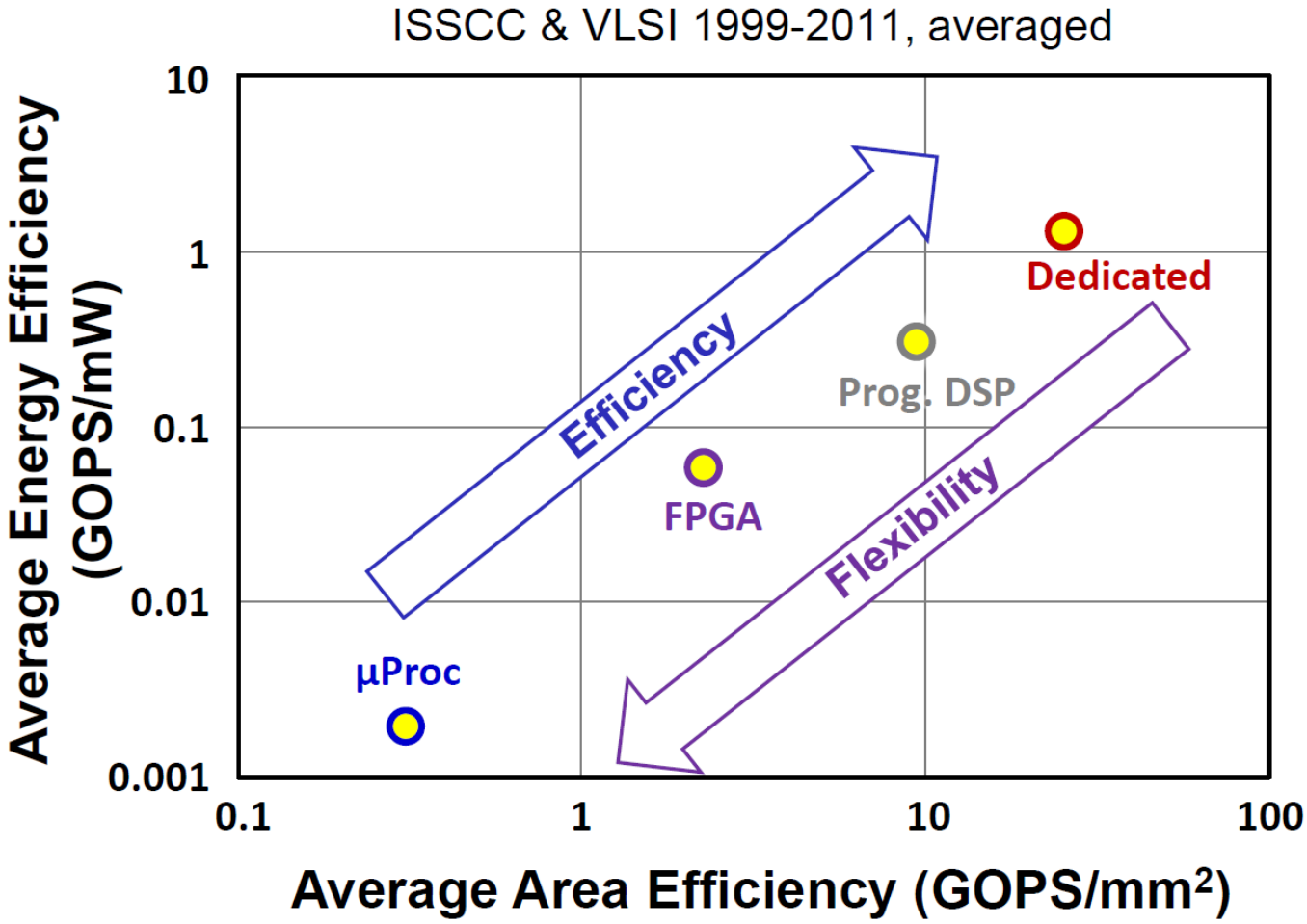


Design constraints



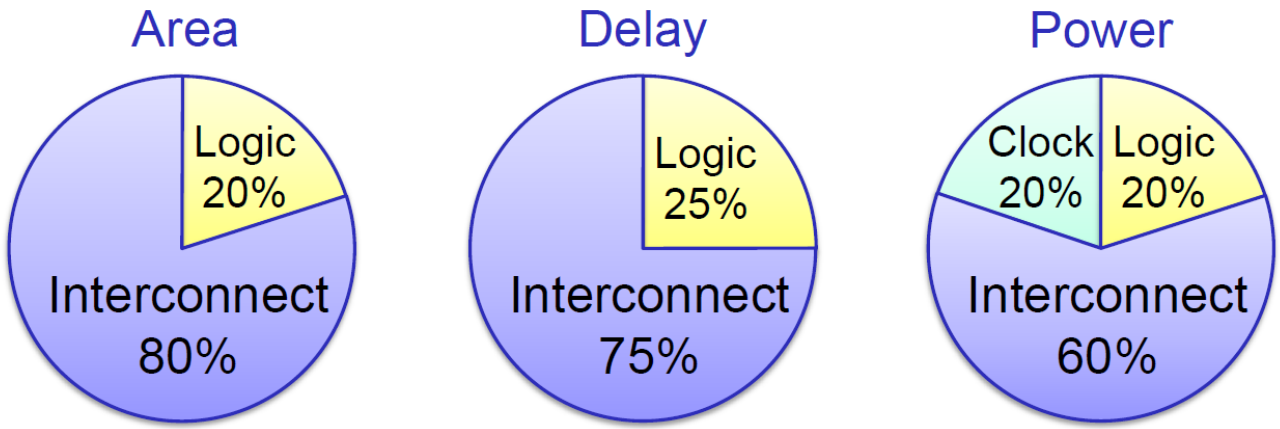


Are FPGAs perfect?



FPGAs are inefficient

- Compared to ASICs, penalties in FPGAs:
  - Area: 17 – 54x
  - Speed: 3 – 7x
  - Power: 6 – 62x
- Main culprit: **INTERCONNECT!**

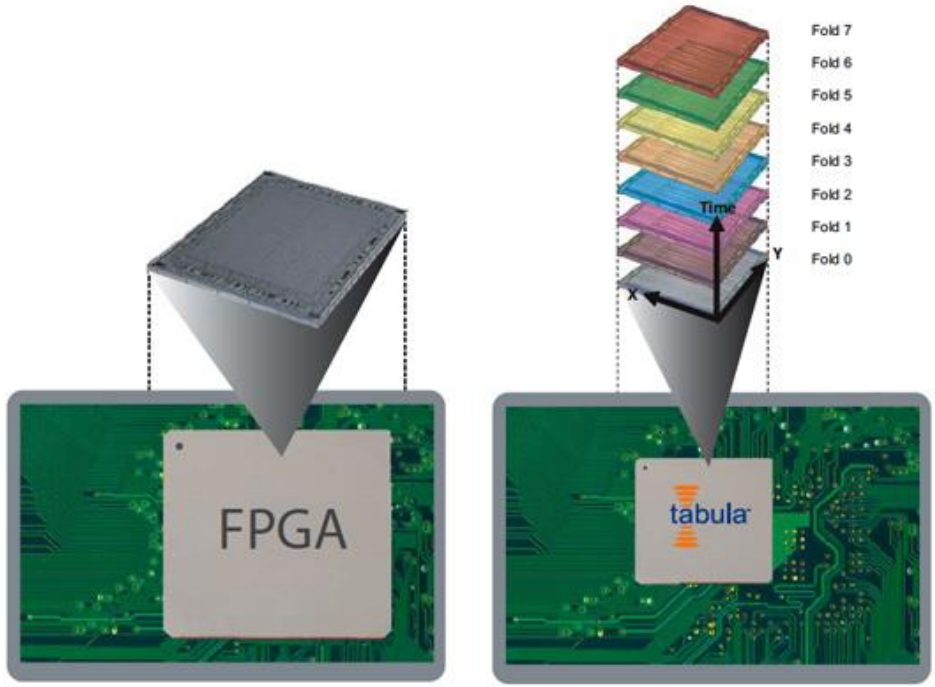


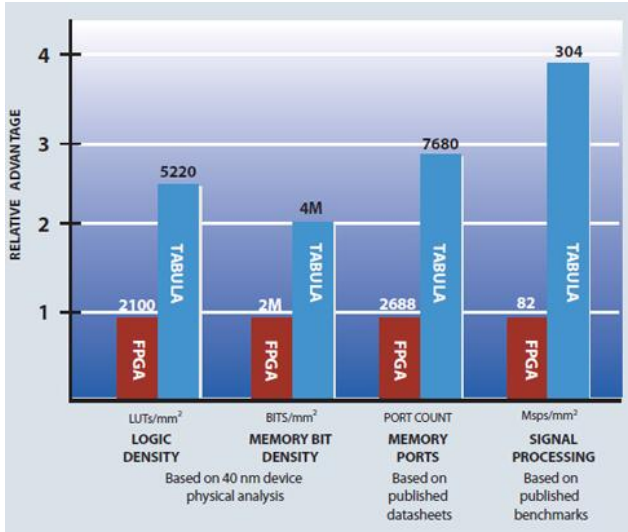
Tabula Spacetime

- Ultra-rapid full/partial reconfiguration with makes it possible to fold more functions onto the same hardware:

  multi-GHz rates
- Their claim:
  - 2.5x logic density
  - 3.7x DSP performance

www.tabula.com





Coarse-grained reconfigurable architecture

- Currently in FPGA
  - Dedicated building blocks: multiplier, DSP core, processor
  - Partial configuration
- Moving torwards coarse-grained architecture:
  - Block-level instead of bit manipulations
  - Lower area and power consumption
  - High-level programming: e.g. xilinx vivado
  - Run-time configuration

Introduction to Xilinx Software

- Xilinx Vivado
  - Integrated tool for design, simulation, synthesis, implementation and FPGA debug
- IP generator
  - Tool used to instantiate Xilinx and third-party IPs into your design
  - Clock generator, Dividers, BRAM etc.
- Integrated Logic Analyzer
  - Used for real time debugging

Introduction to Xilinx Software

- Xilinx Vivado

References

- Clive “Max” Maxfield, “The Design Warrior’s Guide to FPGAs – Devices, Tools and Flows”, ELSEVIER, 2004.

- Bill Jason P. Tomas, “Introduction to Field Programmable Gate Arrays (FPGAs)”.

- Xilinx, “Nexys-4 FPGA Family Data Sheet”.