Lab Assignment 2

Interfacing Keyboard with FPGA Board

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Keyboad Clk and Data

- **Interface the USB keyboard.**
- **It uses two signals (keyboard data and clock)**
- **Interface protocol (LSB first)**

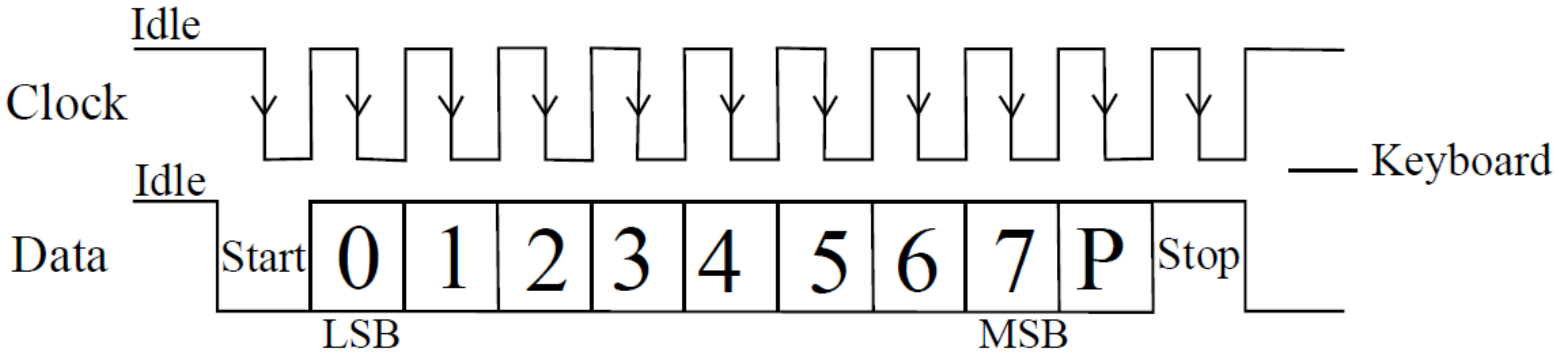


Figure 1: Key Board interface waveform

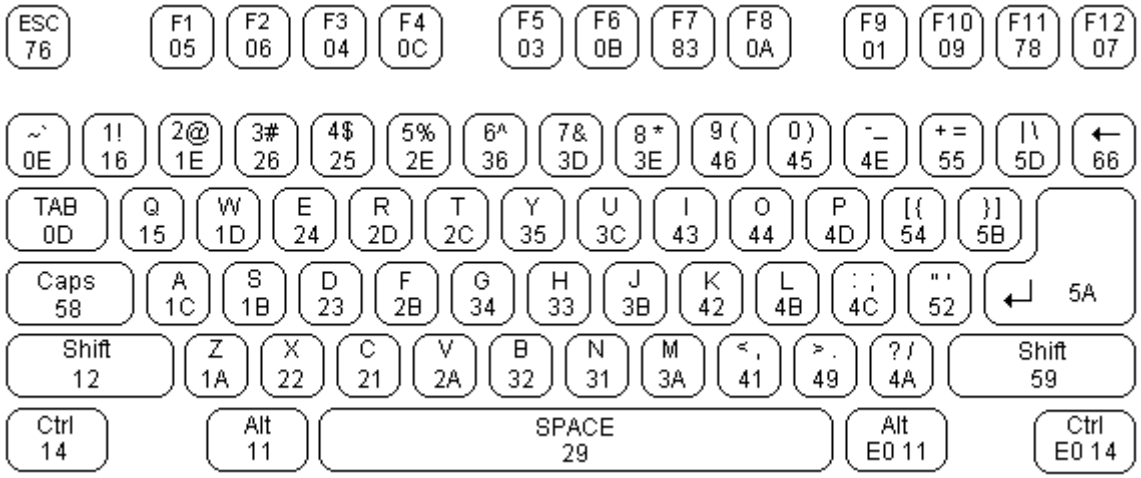
Make code & Break code

- **When key pressed, a make code is generated.**
- **When key is released a break code is generated.**

key	make	break
A	‘1C’h	‘F0’h ‘1C’h
B	‘32’h	‘F0’h ‘32’h
C	‘21’h	‘F0’h ‘21’h

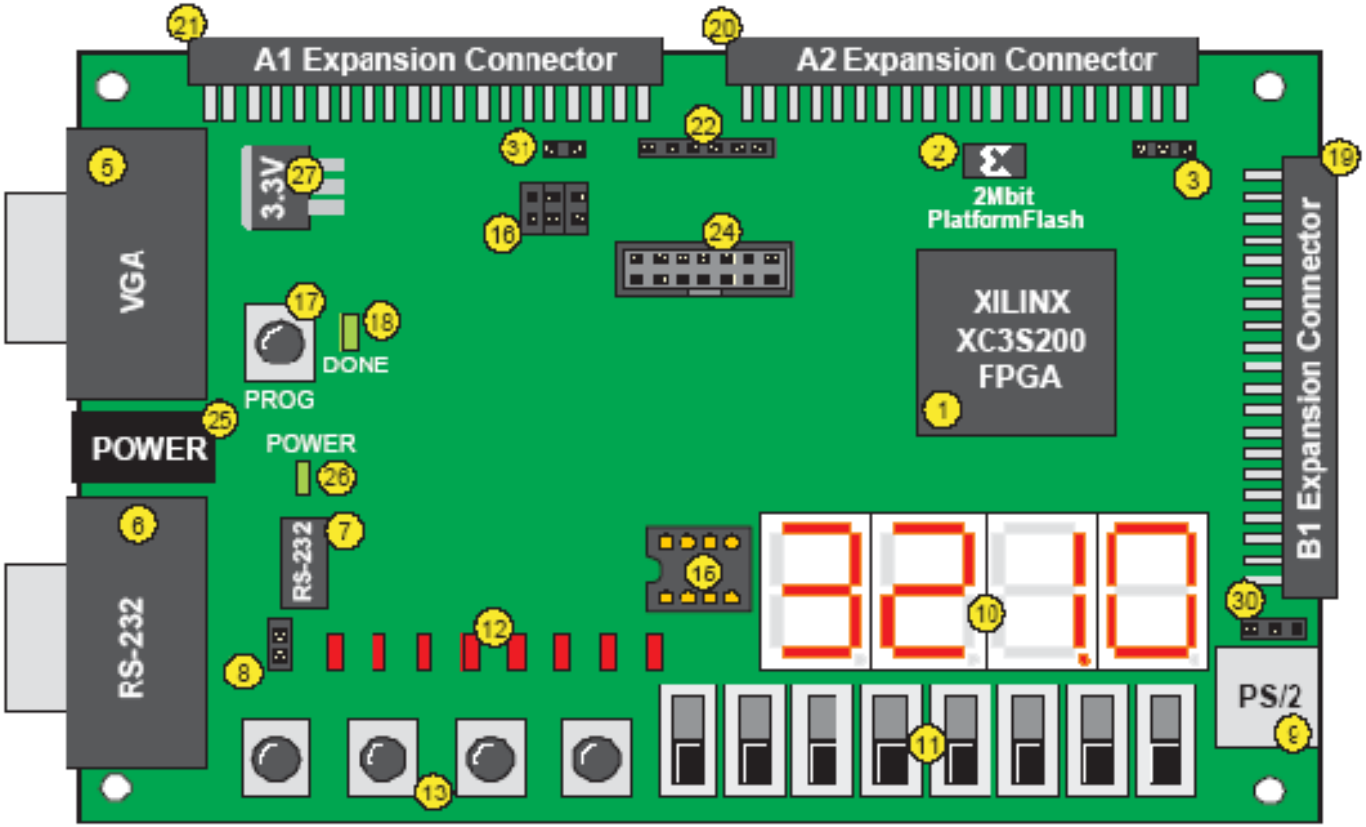
Scan codes

- **Each key is assigned a unique scan code.**



FPGA

- **Pressed key shows on FPGA -- 7 SEGEMENT DISPLAY**



Demostration

- Check the reset condition, all display should be switched off at reset.
- Pressing "123456" one by one, the display should look the following:

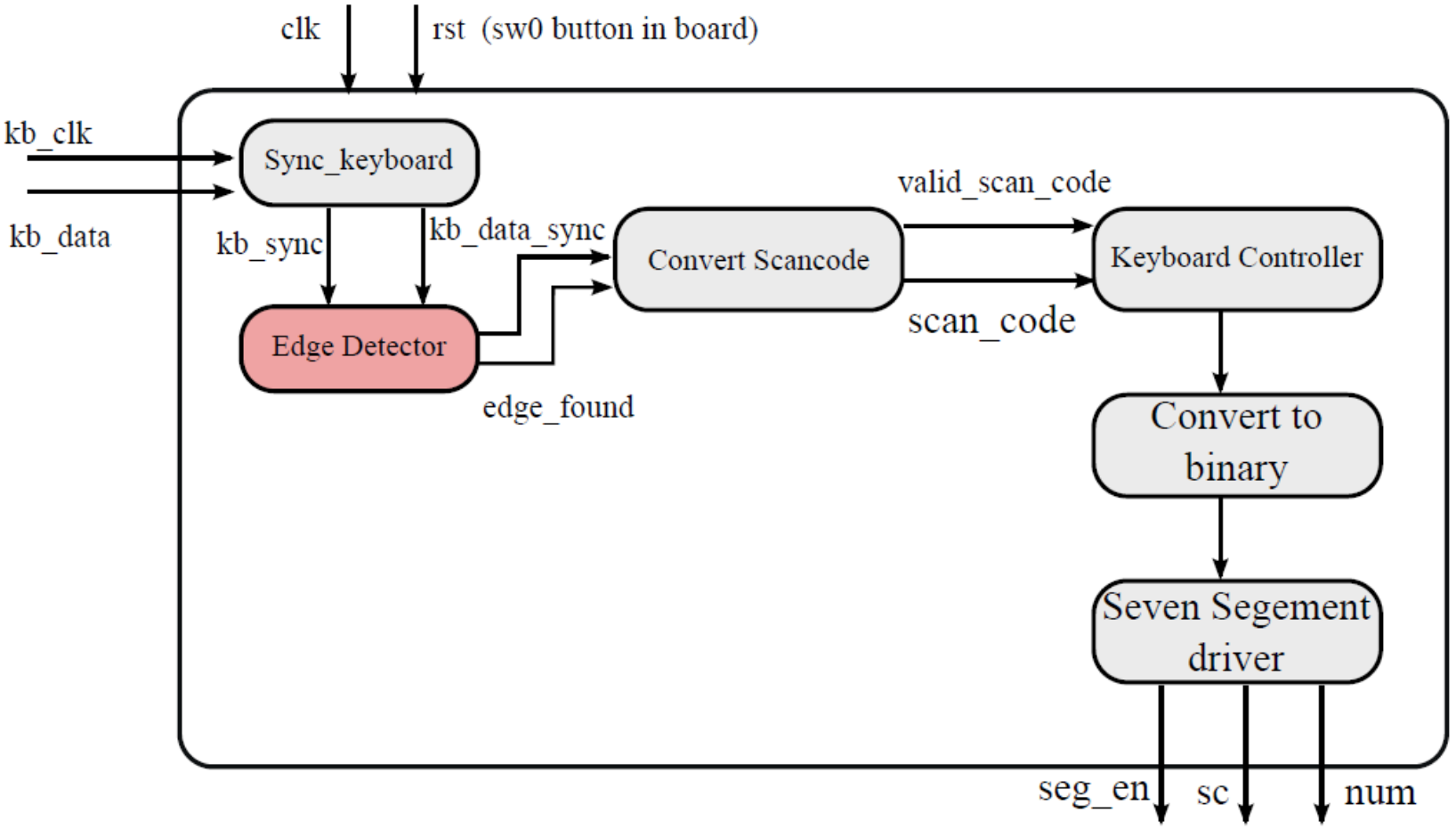
Seven Segement Display

DISPLAY OFF				press (sw0) reset
			1	press 1
		1	2	press 2
	1	2	3	press 3
1	2	3	4	press 4
2	3	4	5	press 5
3	4	5	6	press 6

Main Processes

- **Synchronizing Keyboard with FPGA.**
- **Detection of falling edge of keyboard Clock.**
- **Storing of relevant Data (Scan Code).**
- **Display of ’numbers’ keys on Seven Segment.**
- **Shift the previous key left and display the current number when the next number key is pressed.**

Tasks


clk
rst (sw0 button in board)
kb_clk
kb_data
Sync_keyboard
kb_sync
kb_data_sync
Edge Detector
edge_found
Convert Scancode
valid_scan_code
scan_code
Keyboard Controller
Convert to binary
Seven Segement driver
seg_en
sc
num

VHDL File Lists

File Name	Function
keyboard_top.vhd	Top level integration file
sync_keyboard.vhd	Synchronize keyboard data
edge_detector.vhd	Edge detection circuit
convert_scancode.vhd	Convert serial data to parallel
keybaord_ctrl.vhd	Keyboard controller
convert_to_binary.vhd	Convert scan code to binary
binary_to_sg.vhd	Seven segment driver
keyboard_top.xdc	Pin mapping to FPGA board.
tb_pkg.vhd	Required for some functions in testbench
tb_keyboard.vhd	test bench to drive stimulus
input.txt	Keys to be sent to design via testbench.