EITF35: Introduction to Structured VLSI Design

Part 1.1.2: Introduction (Digital VLSI Systems)

Liang Liu
liang.liu@eit.lth.se
Outline

- Why Digital?
- History & Roadmap
- Device Technology & Platforms
- System Representation
- Design Flow
- RTL (register transfer level) Basics
Digital is an abstraction
- Discrete in time: Sampling
- Discrete in value: Quantization

Digital vs. Analog
- Flexibility & functionality: easier to store and manipulate information
- Reliability: tolerant to noise, mismatch, variations, etc.
- Economic: “easy” to design, and friendly to technology evolvement
Applications 4C: CCCC

Computation

Communication

Consumer

Control

£17,000 (1832)
Coming soon

- **5G 2020+**: 10,000x more traffic, 10 millisecond latency, 10-100x more devices
- **Benefits**:
  - Peak data rates: 10 Gbit/s
  - Battery life: 10 years
  - M2M: ultra low cost
  - Ultra reliability
  - Low energy
  - Coverage

- **26 Billion installed units by 2020**

- **Computing Everywhere**

*Gartner*
Outline

- Why Digital?
  - Advantages
  - Some applications

- History & Roadmap

- Device Technology & Platforms

- System Representation

- Design Flow

- RTL Basics
Brief History

- Transistor Evolution
  - First Transistor
    - Bell Labs (1947)
    - Bardeen, Brattain, Shockley
    - Nobel Prize (1956)

- Integration Evolution
  - First Integrated circuit
    - Jack Kilby
    - TI (1960)
    - Nobel Prize (2000)
Technology Evolution

**Bipolar**
- Transistor
  - 1947, Bardeen/Bell Lab
- Bipolar junction transistor
  - 1949, William Shockley
- Logic gate
  - 1956, Harris
- Integrated circuit
  - 1958, Kilby/Noyes
- Transistor–transistor logic (TTL)
  - 1962, James L. Buie
- High-speed Emitter-coupled logic (ECL)
  - 1974, Masaki

**MOSFET (metal-oxide-semiconductor field-effect transistor)**
- Bipolar faces **power** and **size** limitation
- CMOS logic gate
  - 1963, Wanlass
- PMOSFET
- NMOSFET
  - 1970, *high-density storage* (4K)
  - 1972, *first microprocessor* (4004)
  - 1974, 8080 *microprocessor*
Technology Evolution (cont.)

Ultra-low power graphene-based transistor could enable 100 GHz clock speeds

Scientists at MIPT have developed a new type of power-efficient transistor using bilayered graphene.

Hybrid III-V/silicon SOA for photonic integrated circuits

Conferences Papers (PDF Available) in Proceedings of SPIE - The International Society for Optical Engineering
9277:9277-6 - October 2014 with 236 Reads
DOI: 10.1117/12.2074047

Abstract
Silicon photonics has reached a considerable level of maturity, and the complexity of photonic integrated circuits (PIC) is steadily increasing. As the number of components in a PIC grows, loss management becomes more and more important. Integrated semiconductor optical amplifiers (SOA) will be crucial components in future photonic systems for loss compensation. In addition, there are

Nanowire Transistors Could Let You Talk, Text, and Tweet Longer

Transistors with compound-semiconductor nanowires could consume less power than today's silicon FinFETs

By Richard Stevenson
Posted 26 Jan 2016 | 20:34 GMT

Image: Purdue University
Moore’s Law

Electronics, Apr. 19, 1965

Gordon Moore (co-founder of Intel) made a prediction that semiconductor technology will double its effectiveness every 18 months.
Intel 4004: 1972

- First micro-processor on a single chip
- 2,300 transistors
- 0.3 mm x 0.4 mm
- 4 bit words
- Clock: 0.108 MHz

You will have the possibility to design a more powerful processor in one of our courses

- 42 000 000 transistors
- 0.18 micron CMOS
- Clock: 1.5 GHz
- Die: 20 mm²

Baseband ASIC of a modern mobile phone has easily 10 times more transistors.
SandyBridge (2009)

- 32 nm-64 bit
- 995 000 000 Transistors (23 × P4)
- ~3.5 GHz
- 216 mm²

IvyBridge (2011)

- 22 nm-64 bit
- 1.4b Transistors
- ~3.5 GHz
- 160 mm²
Haswell (2013)

- 22 nm
- Tri-gate 3D transistor
- 1.4b Transistors
- ~3.5 GHz
- 177 mm²
FinFET

Source
Gate
Drain

Gate
Source
Drain
PMOS
substrate

Lund University / EITF35/ Liang Liu 2016
Braswell (2014)

- 14 nm
- Tri-gate 3D transistor (FinFET)
- 1.4b Transistors
- ~4 GHz
- 8MB Cache

Skylake (2015)

- Industry Leading 14nm
- Fanless 2 in 1s to Enthusiast Desktops
- Amazing Form Factors
- New User Experiences

Source: Intel
On-Time 2 Year Cycles

Source: Intel
Moore’s Law: number of transistors
Moore’s Law: frequency

Source: CPU DB: Recording Microprocessor History
Architecture change due to physical limitation
Moore’s Law: power density

Source: Borkar, De Intel®
Architecture change due to new applications
Outline

- Why Digital?
  - Advantages
  - Some applications
- History & Roadmap
- Device Technology & Platforms
- System Representation
- Design Flow
- RTL Basics
Devices

- General-purpose integrated circuits
  - Microprocessors, digital signal processors, FPGA and memories

- Application-specific integrated circuits (ASIC)
  - Designed for a narrow range of applications
  - Full-custom ASIC
  - Standard-cell ASIC
Devices (heterogeneous)

All Programmable SoC
Devices

Intel® Xeon® Processor + Field Programmable Gate Array Software Development Platform (SDP) Shipping Today

Software Development for Accelerating Workloads using Intel® Xeon® processors and coherently attached FPGA in-socket

<table>
<thead>
<tr>
<th>Processor</th>
<th>Intel® Xeon® Processor E5</th>
</tr>
</thead>
<tbody>
<tr>
<td>FPGA Module</td>
<td>Altera® Stratix® V</td>
</tr>
<tr>
<td>QPI Speed</td>
<td>6.4 GT/s full width</td>
</tr>
<tr>
<td></td>
<td>(target 8.0 GT/s at full width)</td>
</tr>
<tr>
<td>Memory to FPGA Module</td>
<td>2 channels of DDR3</td>
</tr>
<tr>
<td></td>
<td>(up to 64 GB)</td>
</tr>
<tr>
<td>Expansion connector</td>
<td>PCI Express® (PCIe) 3.0 x8</td>
</tr>
<tr>
<td>to FPGA Module</td>
<td>lanes - maybe used for direct</td>
</tr>
<tr>
<td></td>
<td>I/O e.g. Ethernet</td>
</tr>
<tr>
<td>Features</td>
<td>Configuration Agent, Caching</td>
</tr>
<tr>
<td></td>
<td>Agent, (optional) Memory</td>
</tr>
<tr>
<td></td>
<td>Controller</td>
</tr>
<tr>
<td>Software</td>
<td>Accelerator Abstraction Layer</td>
</tr>
<tr>
<td></td>
<td>(AAL) runtime, drivers, sample</td>
</tr>
</tbody>
</table>

Available as part of Intel & Altera co-sponsored Hardware Accelerator Research Program
Outline

- Why Digital?
  - Advantages
  - Some applications
- History & Roadmap
- Device Technology & Platforms
- System Representation
- Design Flow
- RTL Basics
System Representation

- **System**
  - SoC: a CPU chip …

- **Module**
  - Macro cell in a chip: ALU…

- **Gate**
  - Basic logic block: xor, nor…

- **Circuit**
  - Transistors

- **Device**
  - Gate, source, drain

This course Digital IC Design
View a Design in a Proper Way

Intel 4004 (2.3K transistors)  Intel Haswell (1.4B transistors)
Full-custom  

- Abstraction: simplified model of a system
  - Show the selected features accurate enough
  - Ignore the others
VLSI Design Flow

- Evolution of circuit design (Design Hierarchy)
  - Full-custom ⇒ Design-automation
    - Based on library cells and IPs
    - Top-down methodology
  - Design abstraction ⇒ “Black box” or “Model”
    - Parameter simplification
    - Accurate enough to meet the requirement

module HS65_GH_NAND2AX14 (Z, A, B);
  output Z;
  input A,B;
  not  U1 (INTERNAL1, B) ;
  or   #1 U2 (Z, A, INTERNAL1) ;
  specify
    (A +=> Z) = (0.1,0.1);
    (B -=> Z) = (0.1,0.1);
  endspecify
endmodule // HS65_GH_NAND2AX14
Outline

- Why Digital?
  - Advantages
  - Some applications
- History & Roadmap
- Device Technology & Platforms
- System Representation
- Design Flow
- RTL Basics
VLSI Design

- **Set of specification:**
  - What does the chip **do**?
  - How **fast** does it run?
  - How **reliable** will it be?
  - How is the silicon **area**?
  - How much **power** will it consume?
  - ......
VLSI Design Flow

- An iterative process that transfers the specification to a manufacturable chip through at least five levels of design abstraction.

1. **Specification**
   - Function, performance, definition: English
2. **Behavior Design**
   - Behavior, algorithm: C/C++, SystemC, Matlab...
3. **Behavior simulation**
Register Transfer Level Design

RTL simulation

VHDL
Verilog

Synthesis

Logic Design

Gate-level simulation
Timing analysis
Power analysis
Circuit Design

Custom Design

Layout

Physical Design

Design rule checking
Post layout simulation
Verification

- **Verification**
  - Check whether a design meets the **specification** and **performance goals**

- **Two aspects**
  - **Functionality**
  - **Performance (timing/power/area)**

- **Method of Verification**
  - **Simulation**
    - **Spot check**: cannot verify the absence of errors
    - **Can be computation intensive**
  - **Timing analysis**
    - **Just check delay**
  - Formal verification
    - **Apply formal math techniques determine its property**
    - **E.g, equivalence checking**
  - **Hardware emulation**
Fabrication

22nm Fab Upgrades

D1D/C
Fab 32/12
Fab 28
Israel

14nm

D1X
Oregon

22nm 3rd generation
Intel® Core™ processor
Testing

- Testing is the process of detecting physical defects of a die or a package occurred at the time of manufacturing.
- Testing and verification are different tasks.
- Difficult for large circuit
  - Need to add auxiliary testing circuit in design
  - E.g., built-in self test (BIST), scan chain etc.
VLSI Design Flow: Tools

- **Algorithm**
  - Matlab

- **RTL Simulation**
  - **Modelsim, Mentor**
  - VCS, Synopsys
  - VerilogXL, Cadence

- **Logic Synthesis**
  - **Design Compiler, Synopsys**
  - Blast Create, Magma

- **Transistor Simulation**
  - **Hspice/Starsim, Synopsys**
  - Spectra, Cadence
  - Eldo, Mentor

- **Mixed-Signal Simulation**
  - **AMS Designer, Cadence**
  - ADMS, Mentor
  - Saber, Synopsys

- **Place & Route**
  - Astro, Synopsys
  - **Silicon Encounter, Cadence**
  - Blast Fusion, Magma

- **Layout**
  - lcfb/Dracula, Cadence
  - ICstation/Calibre, Mentor

- **FPGA**
  - **Vivado, Xilinx**
  - Quatus, Altera
VLSI Design Flow: Summary

1. **English**
   - specification

2. **Executable program**
   - behavior

3. **HDL**
   - register-transfer

4. **Logic gates**
   - logic

5. **Transistors**
   - circuit

6. **Rectangles**
   - layout

**Tools:**
- PDF
- Matlab/C/Pen&Paper
- Emacs/UltraEdit/Modelsim
- Xilinx
- Vivado
Following slides should fresh up your memory
Overall VLSI Structure

- **Scheduling / ordering / sequencing of operations**
- **Mapping / allocation:**
  - Variables -> \{Reg1, ... ,RegN\}
  - Operations -> \{MUL, ADD, ALU, ... ,\}

We will implement something similar in this course
Two Basic Digital Components (What)

**Combinational Logic**

Always:
\[ z \leq F(a, b, c); \]

i.e. a function that is always evaluated when an input changes. Can be expressed by a truth table.

**Register**

if clk’ event and clk= ‘1’ then
\[ Q \leq D; \]

i.e. a stored variable,
Edge triggered D Flip-Flop with enable.
Timing (When)

Only if we guarantee to meet the **timing requirements**

... do the components guarantee to behave as intended.
Combinational Logic Timing

- **Propagation delay:**
  After presenting new inputs
  Worst case delay before producing correct output
**Register timing**

**Setup time:**
Minimum time input must be stable before clk↑.

**Hold time:**
Minimum time input must be stable after clk↑.

**Propagation delay (clk_to_Q):**
Worst case (maximum) delay after clk↑ before new output data is valid on Q.
Clock Frequency (RTL)

What is the maximum clock frequency?

**Register**
- Propagation delay: \( T_{ckl-Q} \) 250ps
- Setup time: \( T_{su} \) 200ps
- Hold time: \( T_{h} \) 100ps

**AND-gate**
- Propagation delay: \( T_{prop} \) 250ps

\[
250 + 250 \times 3 + 200 = 1.2\text{ns}
\]

\[
f = 833\text{MHz}
\]
Critical path

- begin to explore the construction of digital systems with complex behavior
  - Example: \( K = (A +_1 B) *_1 (C +_2 D *_2 E) \)

- Combinational circuit:

```
\[ \text{Critical Path} \]
```
Thanks