EITF35: Introduction to Structured VLSI Design

Part 1.1.2: Introduction (Digital VLSI Systems)

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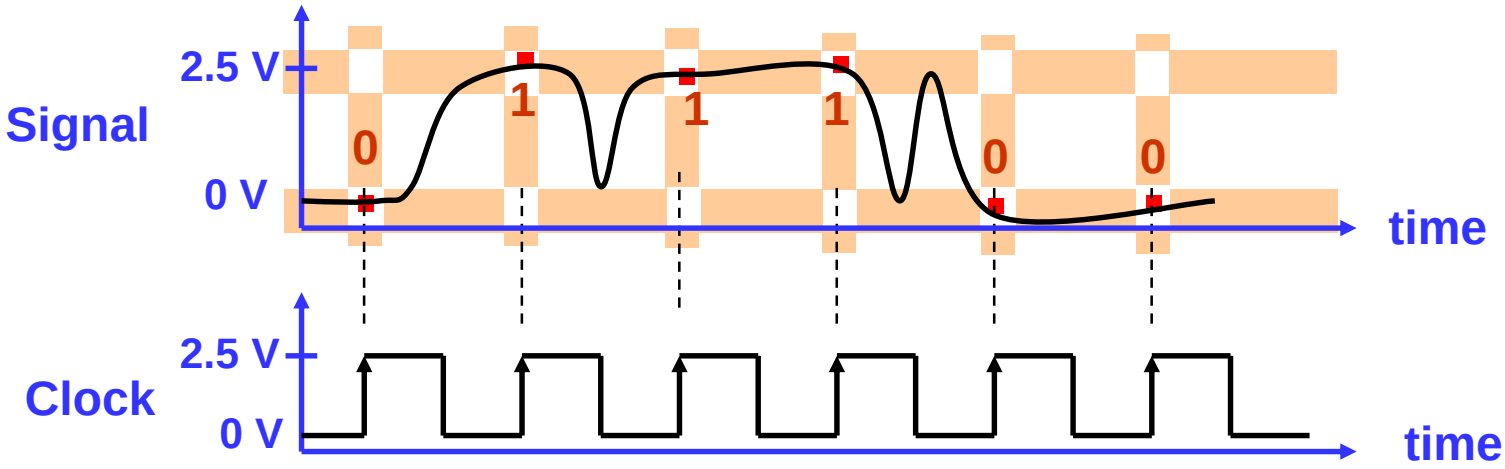
Outline

- Why Digital?
- History & Roadmap
- Device Technology & Platforms
- System Representation
- Design Flow
- RTL (register transfer level) Basics

Digitalization



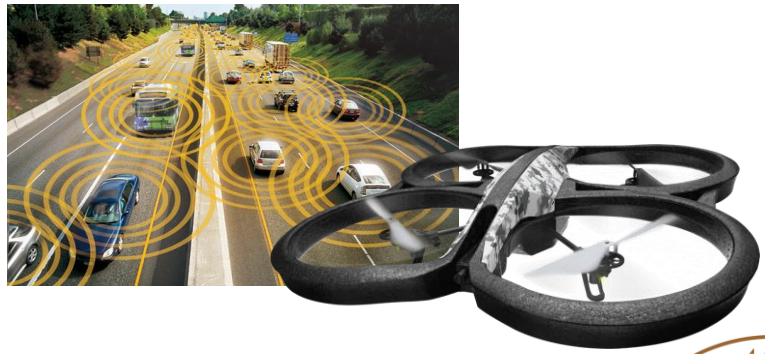
- **Digital is an abstraction**
  - Discrete in time: Sampling
  - Discrete in value: Quantization
- **Digital vs. Analog**
  - Flexibility & functionality: easier to store and manipulate information
  - Reliability: tolerant to noise, mismatch, variations, etc.
  - Economic: “easy” to design, and friendly to technology evolvement

Applications 4C:CCCC

Computation

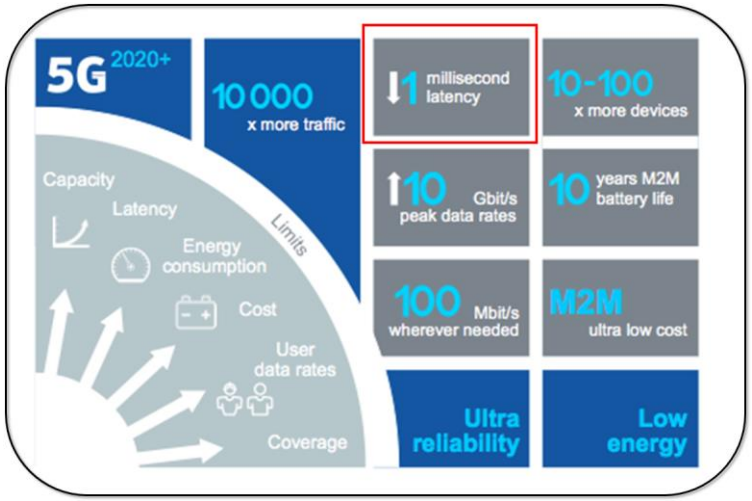
Communication

Consumer

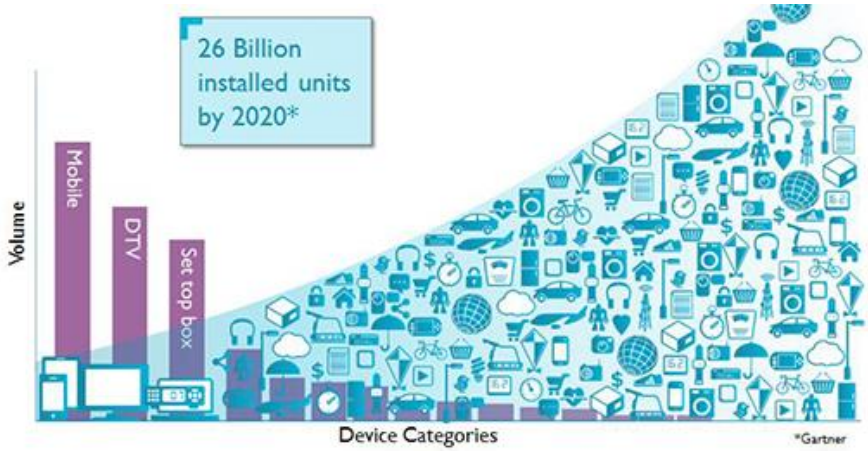


Control

Coming soon


5G 2020+
10 000
x more traffic
1 millisecond latency
10-100
x more devices
10 Gbit/s peak data rates
10 years M2M battery life
100 Mbit/s wherever needed
M2M ultra low cost
Ultra reliability
Low energy
Capacity
Latency
Energy consumption
Cost
User data rates
Coverage
Limits


#1
Computing Everywhere

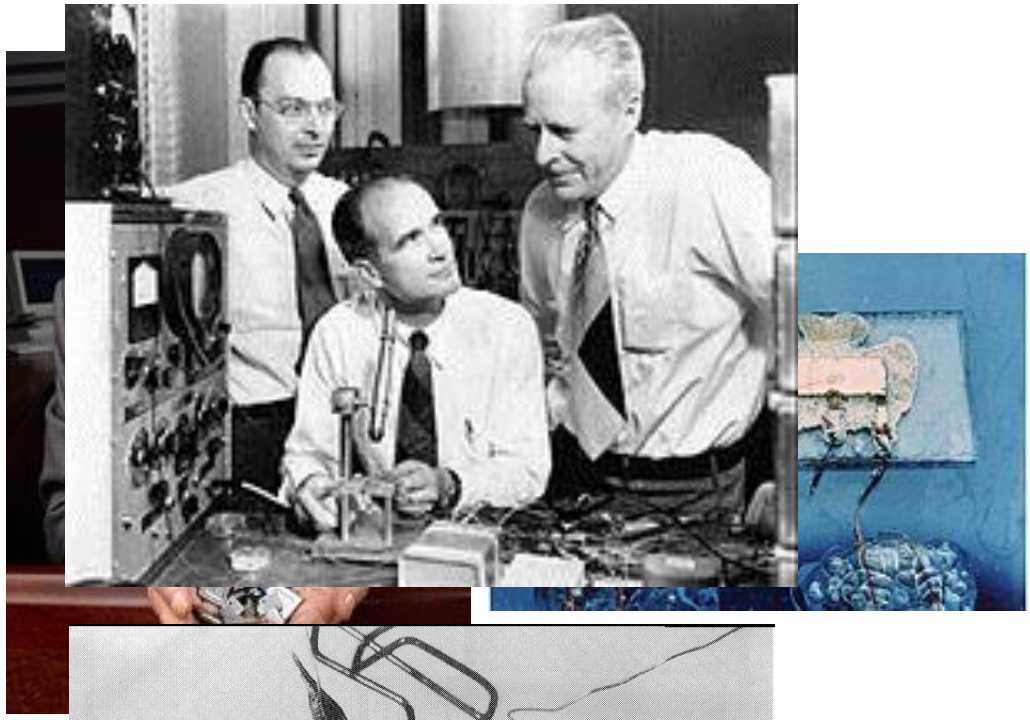

26 Billion installed units by 2020*
Volume
Mobile
DTV
Set top box
Device Categories
*Gartner

Outline

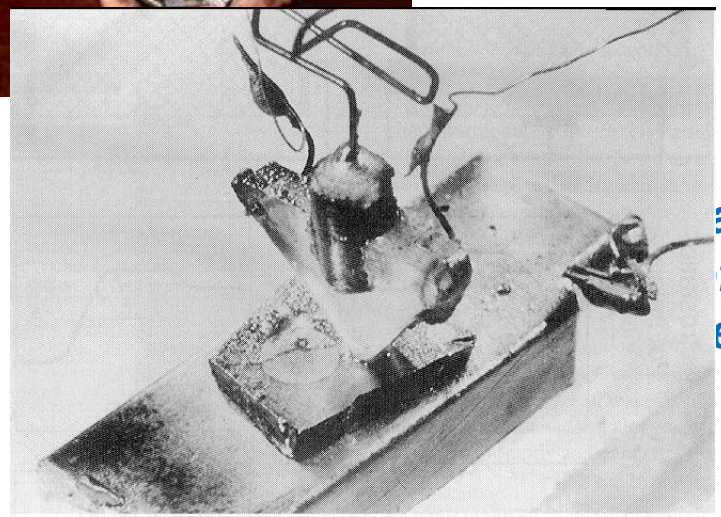
- Why Digital?
  - Advantages
  - Some applications
- **History & Roadmap**
- Device Technology & Platforms
- System Representation
- Design Flow
- RTL Basics

Brief History

- **Transistor Evolution**
  - First Transistor
    - ***Bell Labs (1947)***
    - ***Bardeen, Brattain, Shockley***
    - ***Nobel Prize (1956)***



- **Integration Evolution**
  - First Integrated circuit
    - ***Jack Kilby***
    - ***TI (1960)***
    - ***Nobel Prize (2000)***



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Technology Evolution

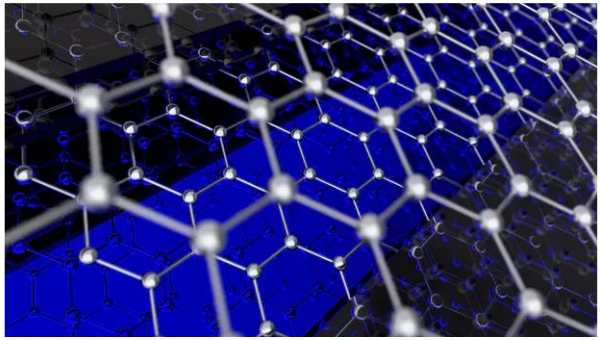
- **Bipolar**
  - Transistor
    - ***1947, Bardeen/Bell Lab***
  - Bipolar junction transistor
    - ***1949, William Shockley***
  - Logic gate
    - ***1956, Harris***
  - Integrated circuit
    - ***1958, Kilby/Noyes***
  - Transistor–transistor logic (TTL)
    - ***1962, James L. Buie***
  - High-speed Emitter-coupled logic (ECL)
    - ***1974, Masaki***

- **MOSFET (metal-oxide-semiconductor field-effect transistor)**
  - Bipolar faces **power** and **size** limitation
  - **CMOS logic gate**
    - ***1963, Wanlass***
  - PMOSFET
    - ***1970, first practical MOS IC, Calculator***
  - NMOSFET
    - ***1970, high-density storay(4K)***
    - ***1972, first microprocessor(4004)***
    - ***1974, 8080 microprocessor***

Technology Evolution (cont.)

Ultra-low power graphene-based transistor could enable 100 GHz clock speeds

Michael Irving | May 24, 2016



Scientists at MIPT have developed a new type of power-efficient transistor using bilayered graphene.

Nanowire Transistors Could Let You Talk, Text, and Tweet Longer

Transistors with compound-semiconductor nanowires could consume less power than today's silicon FinFETs

By Richard Stevenson
Posted 26 Jan 2016 | 20:34 GMT

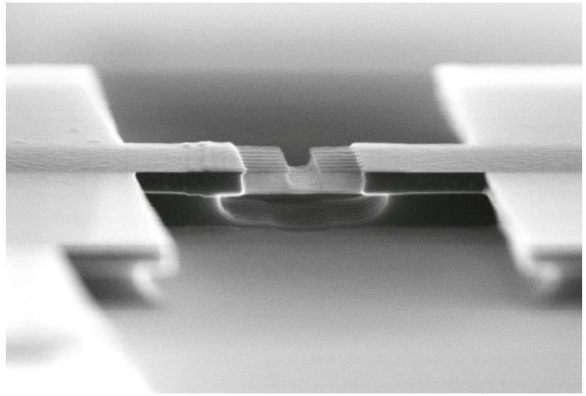


Image: Purdue University

Hybrid III-V/silicon SOA for photonic integrated circuits

Conference Paper (PDF Available) *in* Proceedings of SPIE - The International Society for Optical Engineering 9277:9277-6 · October 2014 *with* 239 Reads

DOI: 10.1117/12.2074617
Conference: Proc. SPIE, At Beijing, China, Volume: 9277

1st Peter Kaspar
24.57 · III-V Lab, Alcatel Lucent Bell Labs

2nd R. Brenot

3rd A. Le Liepvre

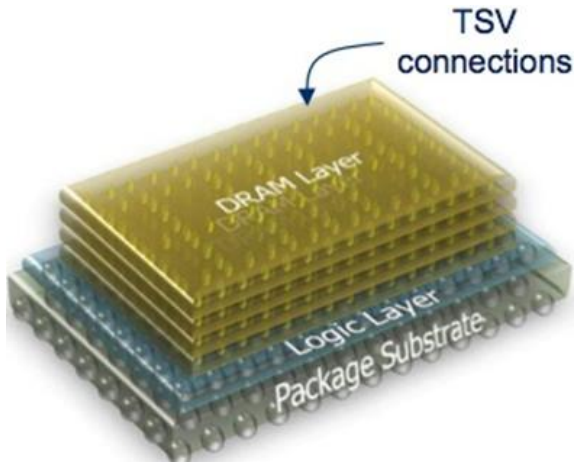
+ 9

Last Sylvie Menezo
25.36 · Cea Leti

Show more authors

Abstract

Silicon photonics has reached a considerable level of maturity, and the complexity of photonic integrated circuits (PIC) is steadily increasing. As the number of components in a PIC grows, loss management becomes more and more important. Integrated semiconductor optical amplifiers (SOA) will be crucial components in future photonic systems for loss compensation. In addition, there are



Moore's Law

The experts look ahead

Cramming more components onto integrated circuits

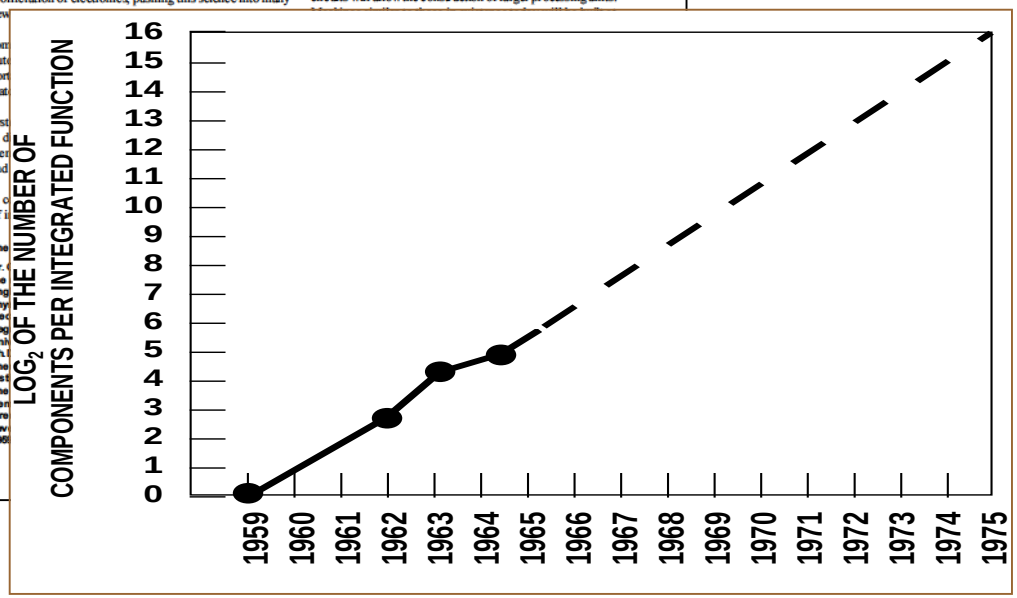
With unit cost falling as the number of components per circuit rises, by 1975 economics may dictate squeezing as many as 65,000 components on a single silicon chip

By Gordon E. Moore

Director, Research and Development Laboratories, Fairchild Semiconductor division of Fairchild Camera and Instrument Corp.

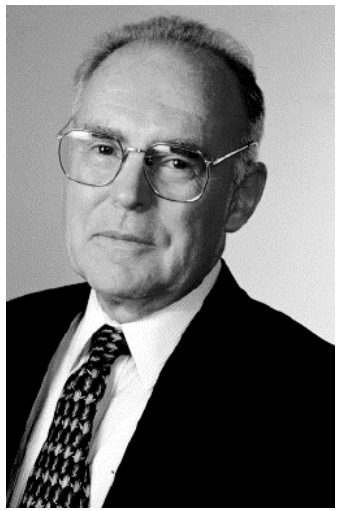
The future of integrated electronics is the future of electronics itself. The advantages of integration will bring about a proliferation of electronics, pushing this science into many

machine instead of being concentrated in a central unit. In addition, the improved reliability made possible by integrated circuits will allow the construction of larger processing units.

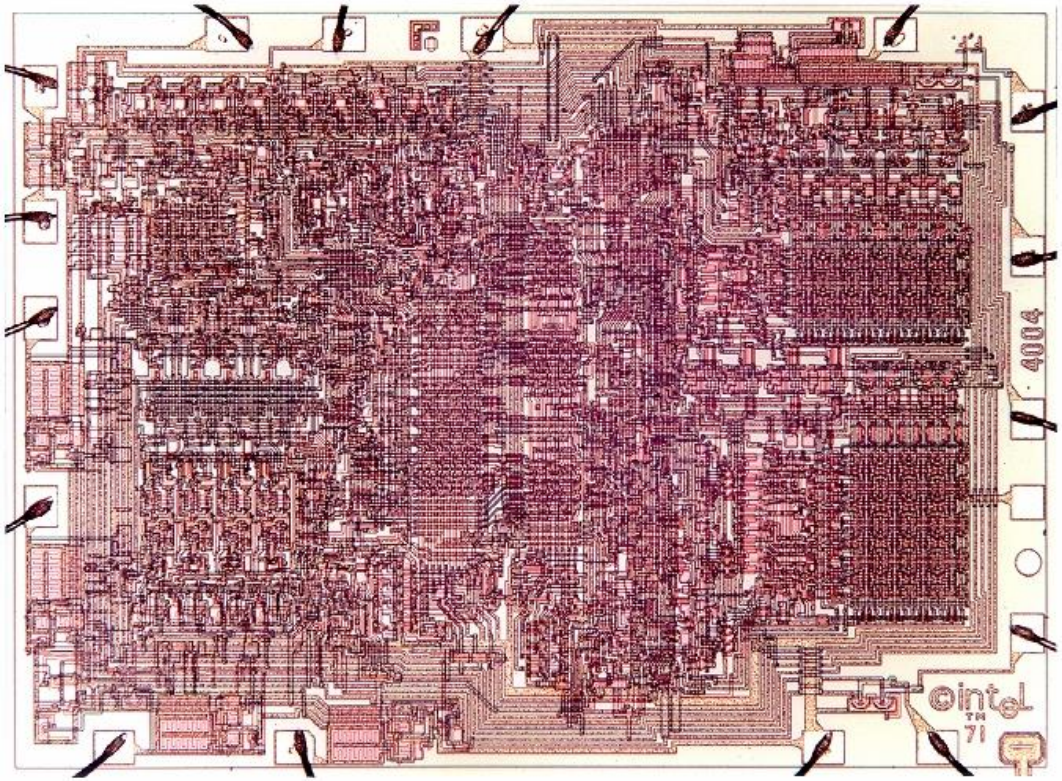


- **Electronics, Apr. 19, 1965**

Gordon Moore (co-founder of Intel) made a prediction that semiconductor technology will double its effectiveness every 18 months



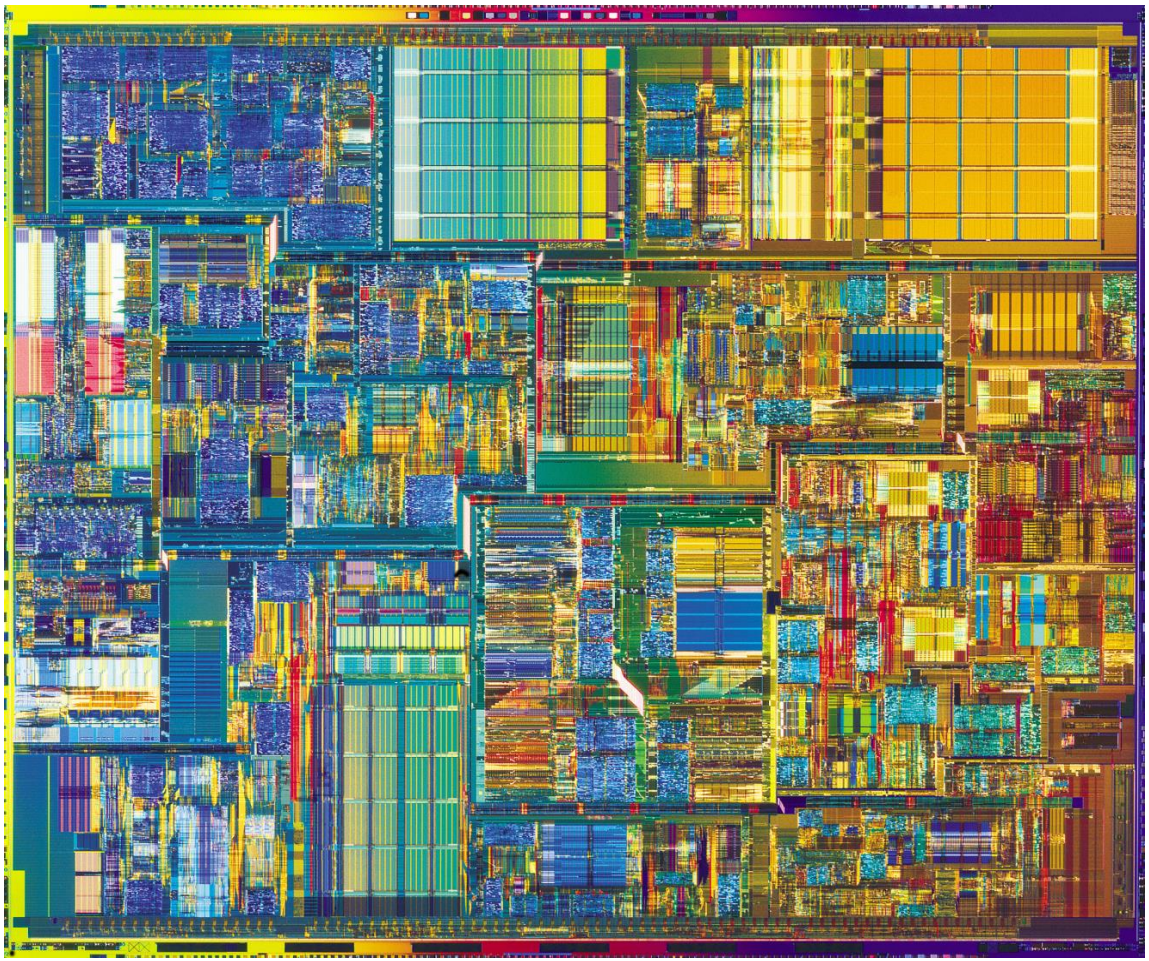
Intel 4004:1972



- First micro-processor on a single chip
- 2 300 transistors
- 0.3 mm x 0.4 mm
- 4 bit words
- Clock: 0.108 MHz

You will have the possibility to design a more powerful processor in one of our courses

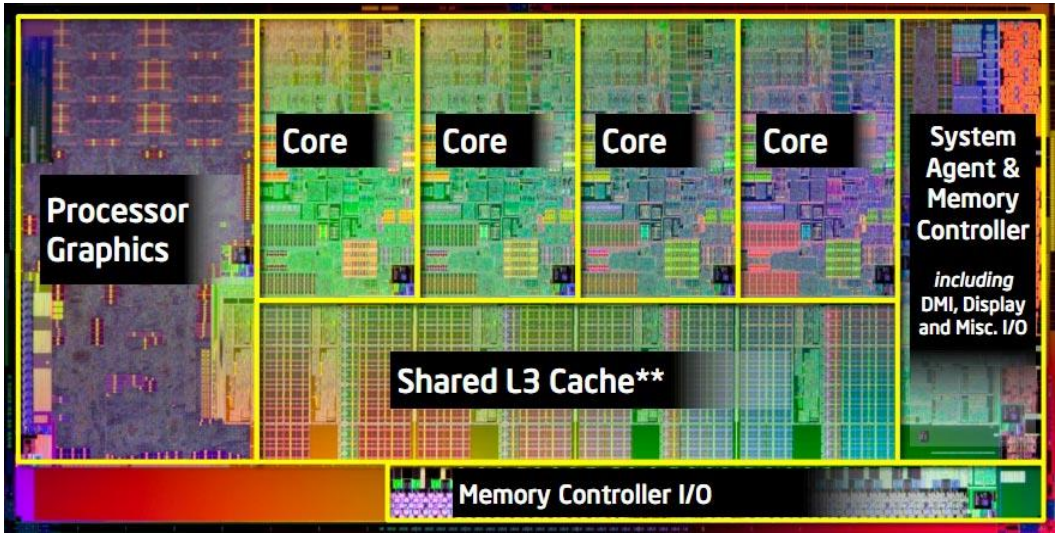
Intel Pentium 4 (2000)



- 42 000 000 transistors
- 0.18 micron CMOS
- Clock: 1.5 GHz
- Die: 20 mm^2

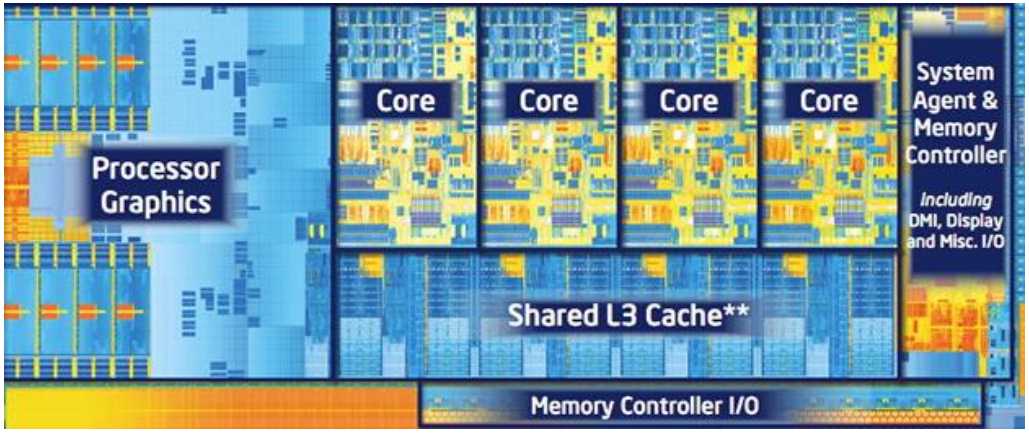
Baseband ASIC of a modern mobile phone has easily 10 times more transistors.

SandyBridge (2009)



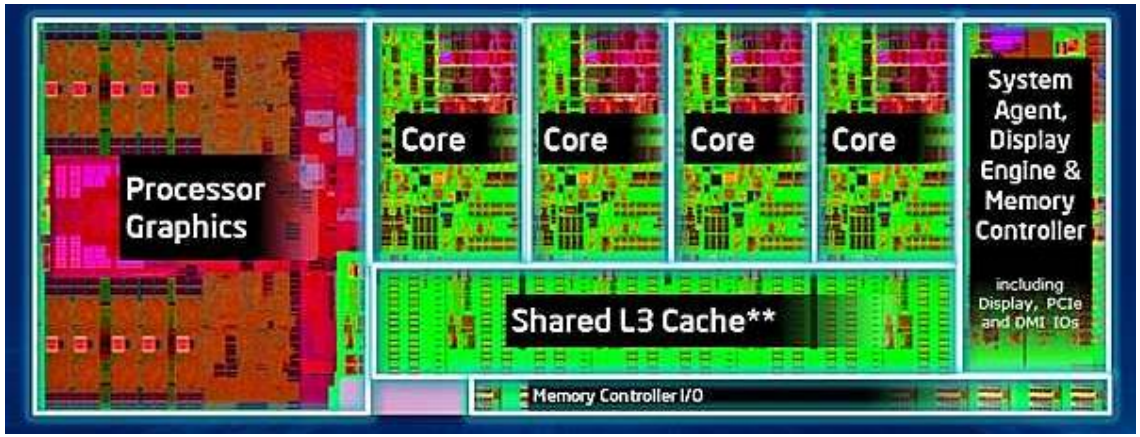
- 32 nm-64 bit
- 995 000 000 Transistors (23 × P4)
- ~3.5 GHz
- 216 mm²

IvyBridge (2011)

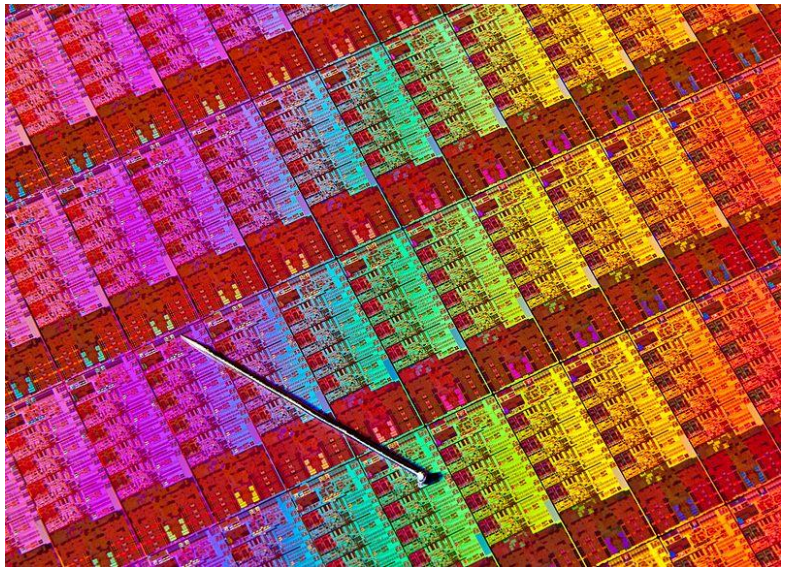


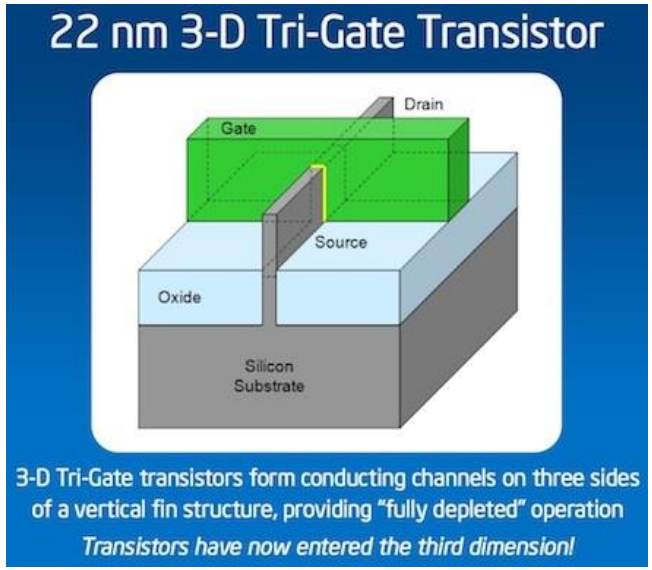
- 22 nm-64 bit
- 1.4b Transistors
- ~3.5 GHz
- 160 mm²

Haswell (2013)

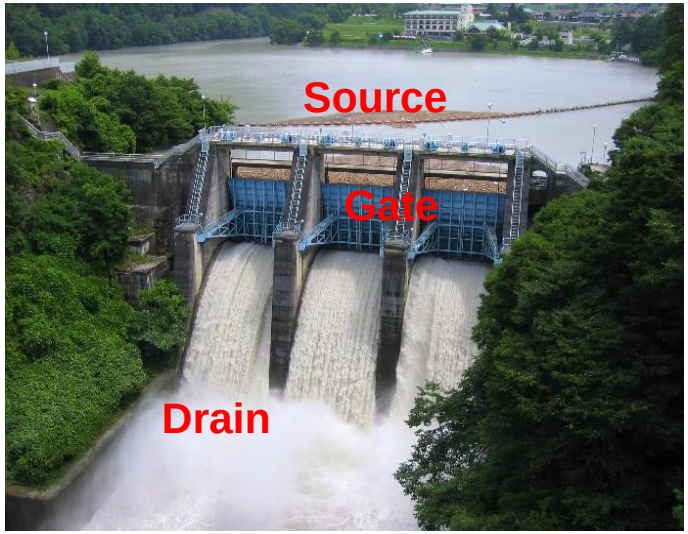


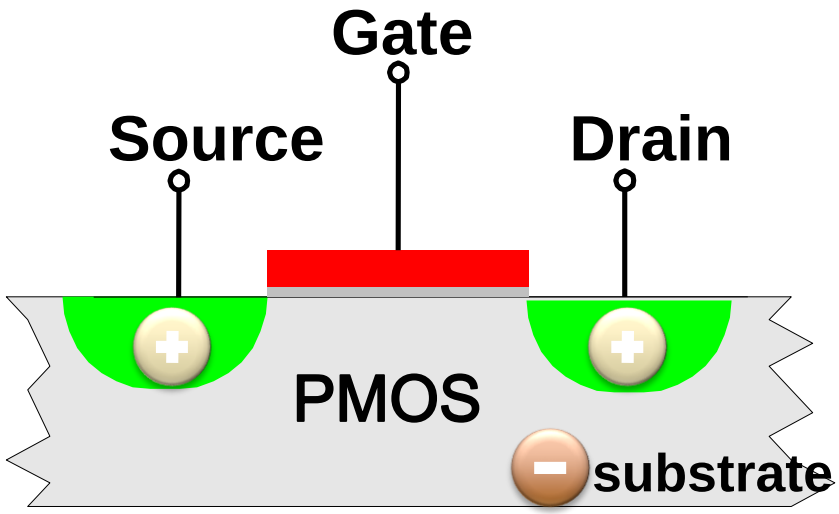
- 22 nm
- Tri-gate 3D transistor
- 1.4b Transistors
- ~3.5 GHz
- 177 mm^2

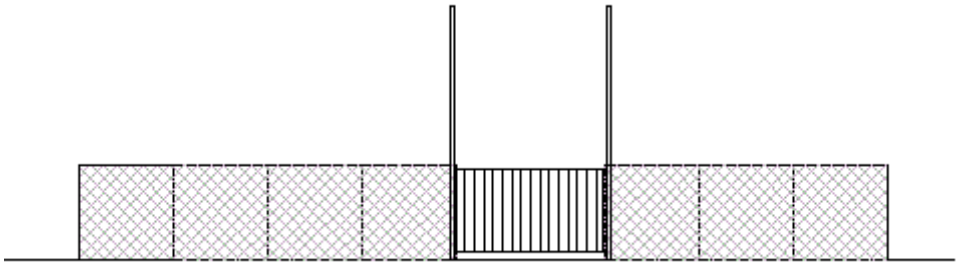


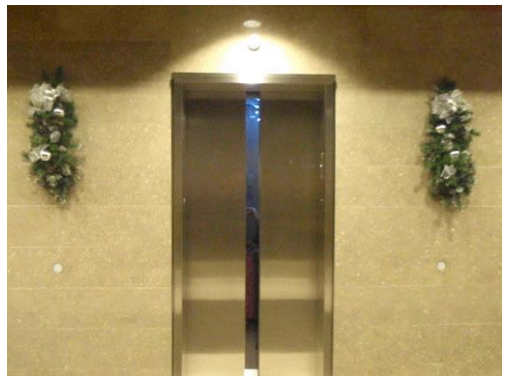


FinFET

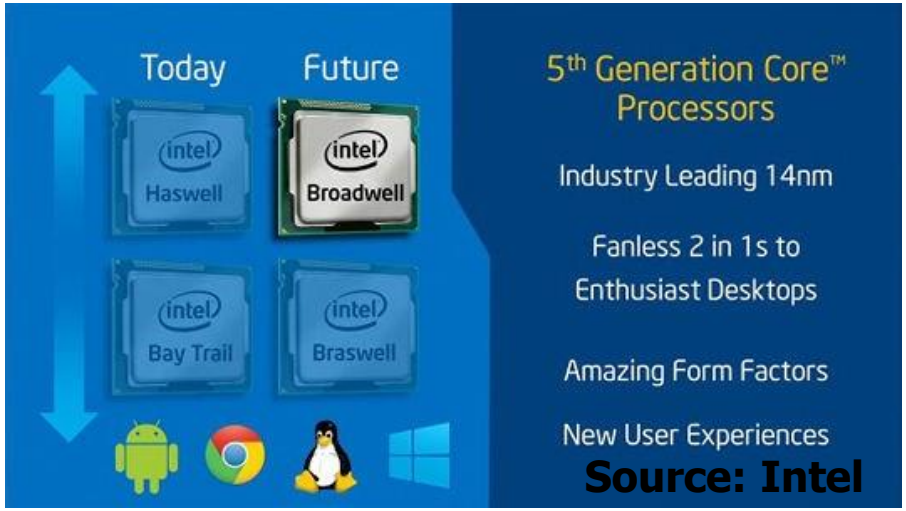




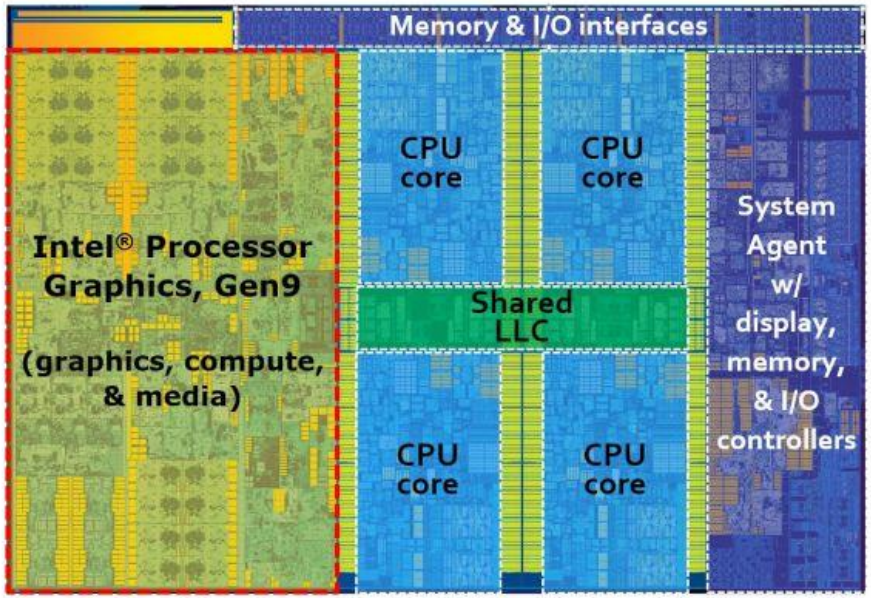




Braswell (2014)

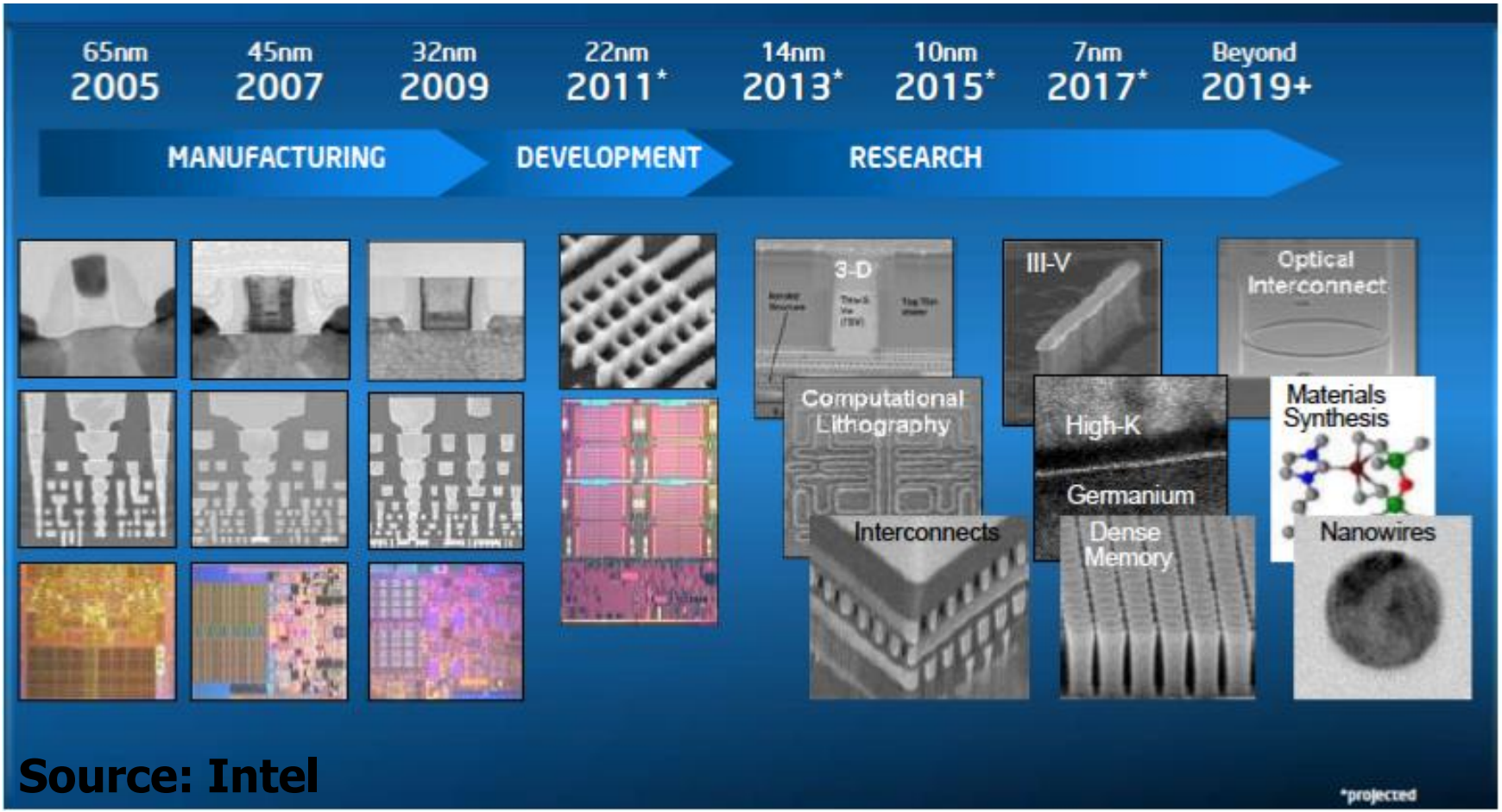


Skylake (2015)

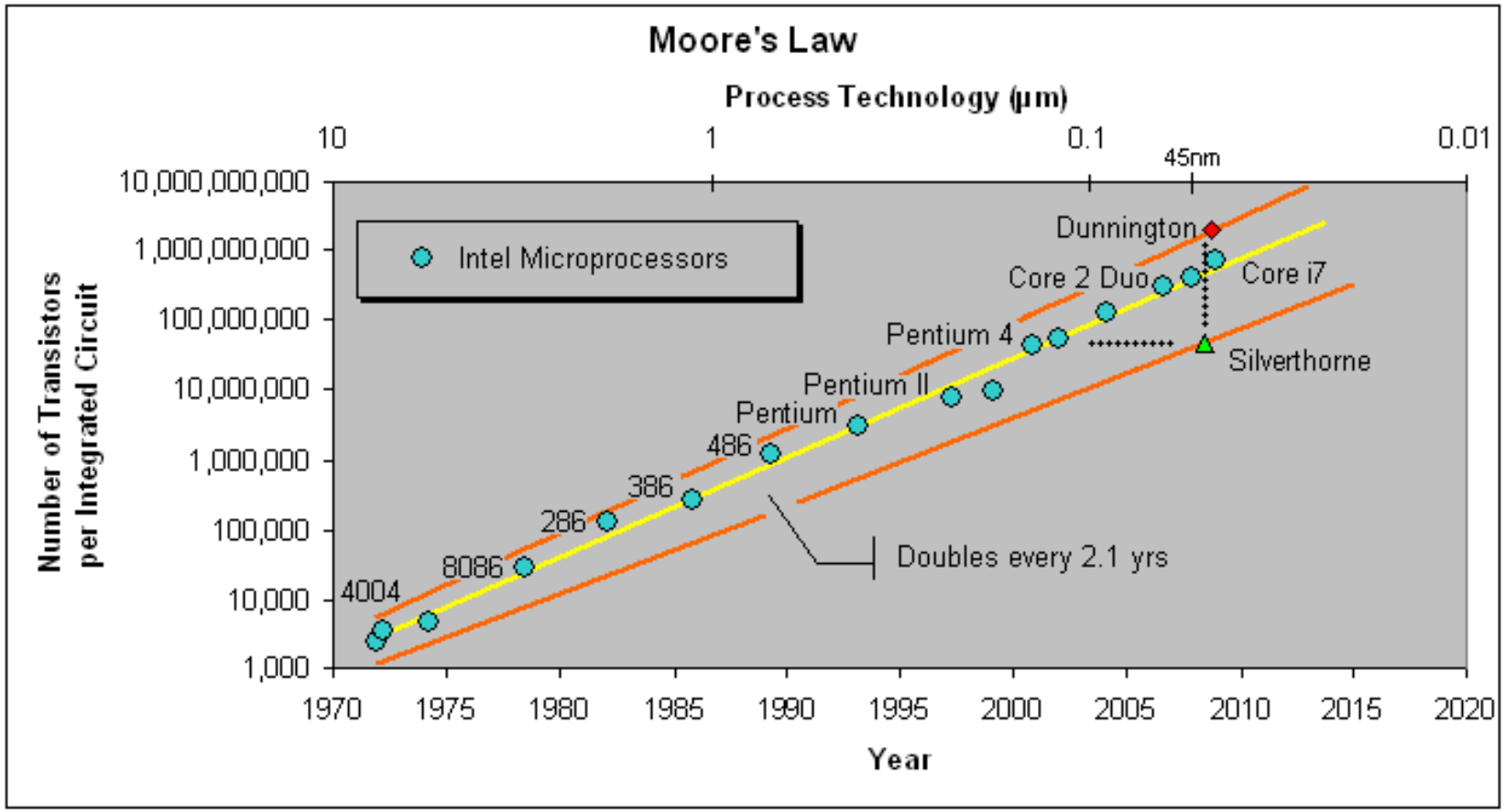


- 14 nm
- Tri-gate 3D transistor (FinFET)
- 1.4b Transistors
- ~4 GHz
- 8MB Cache

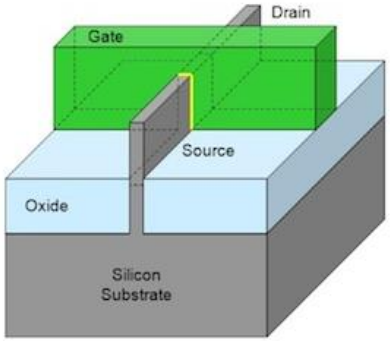
On-Time 2 Year Cycles

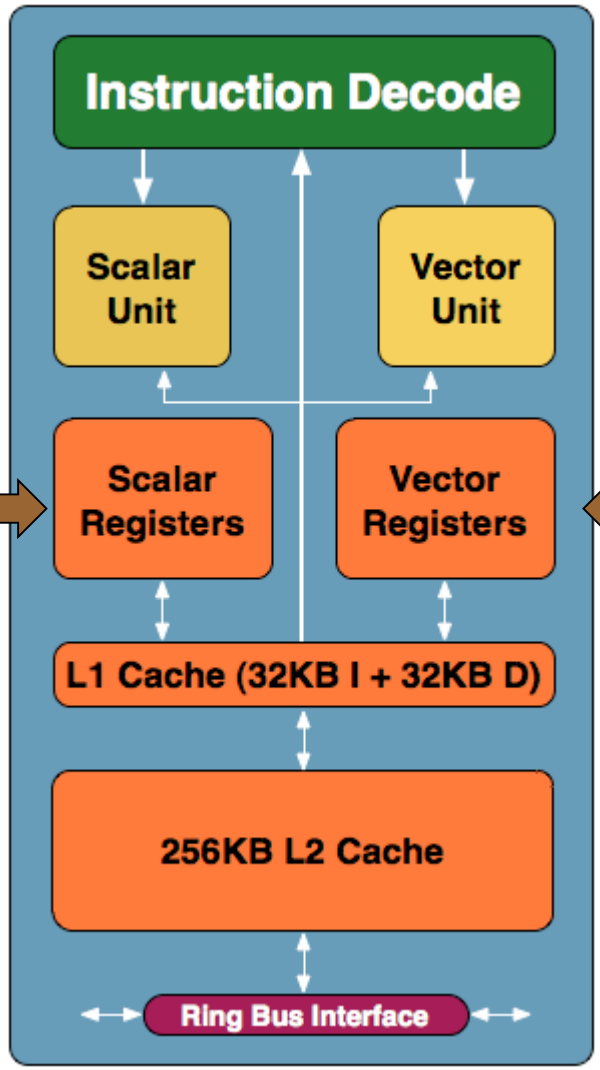


Moore's Law: number of transistors



Intel Architecture

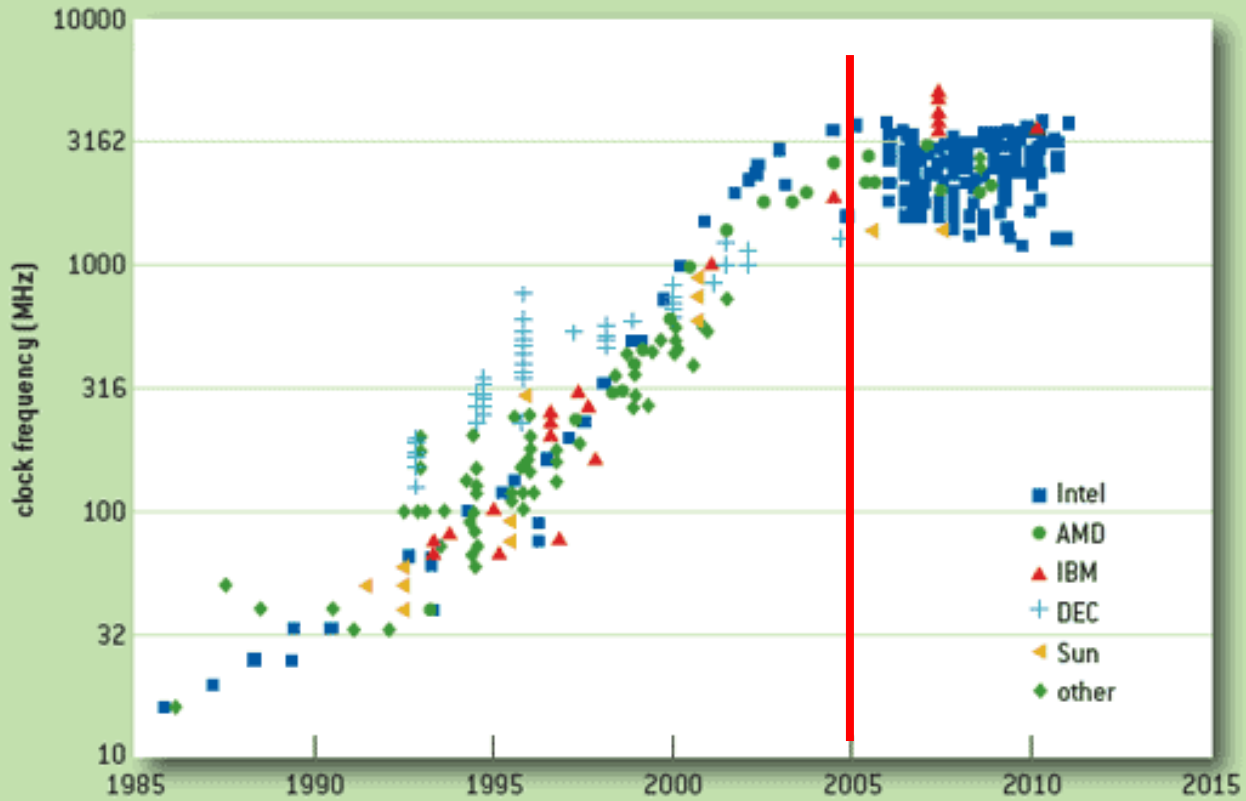




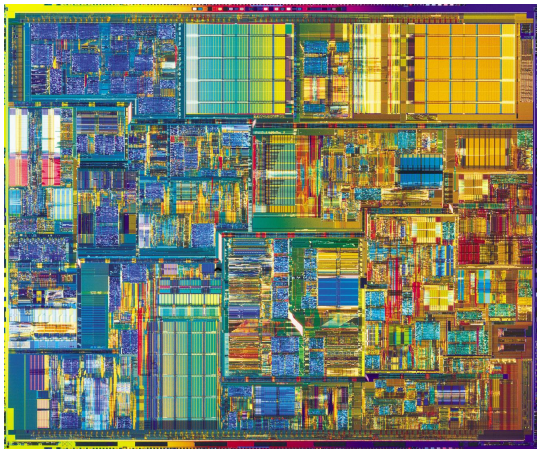
Moore's Law: frequency

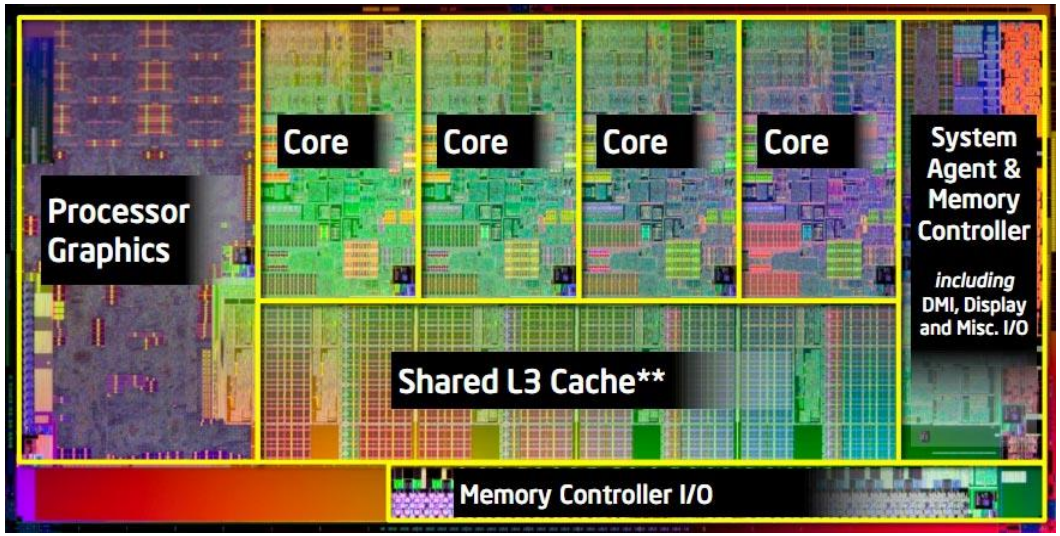
FIGURE 7

Source: CPU DB: Recording Microprocessor History

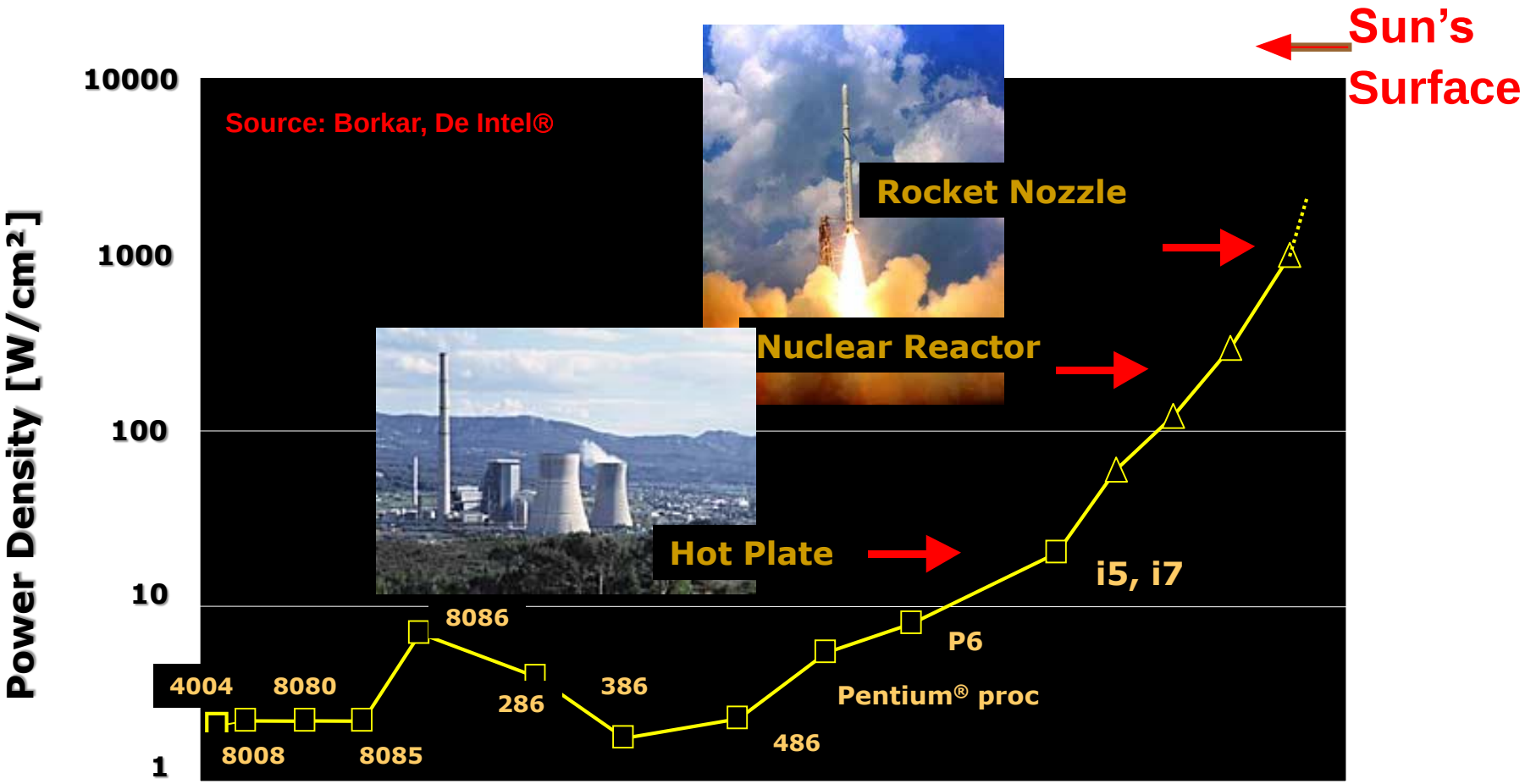


Architecture change due to physical limitation

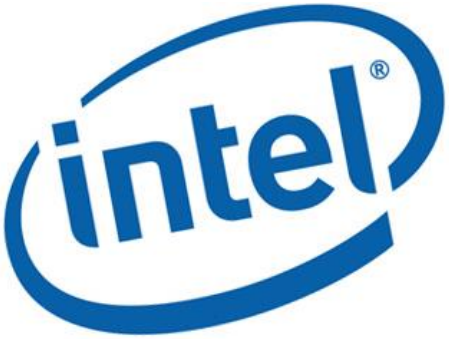




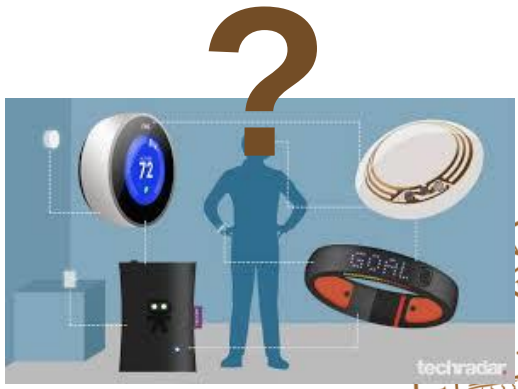
Moore's Law: power density



Architecture change due to new applications



ARM



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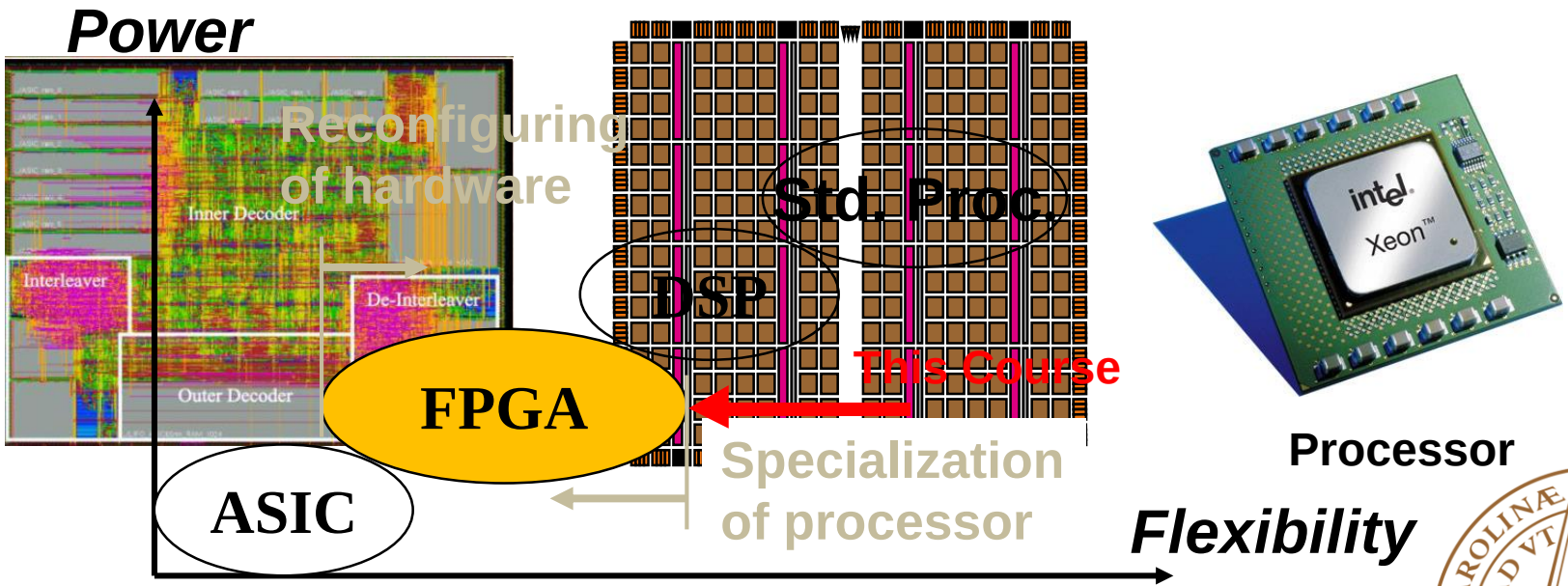
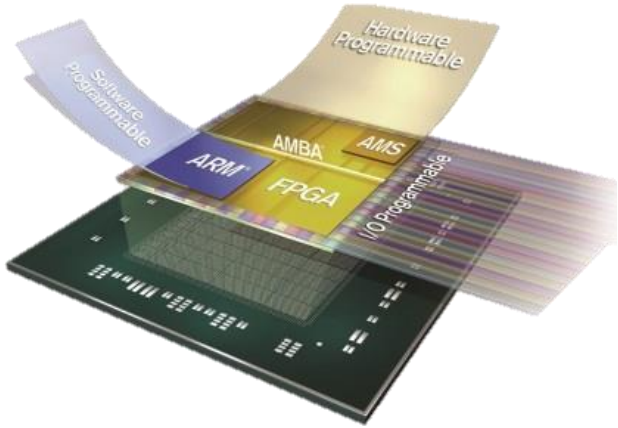
Devices

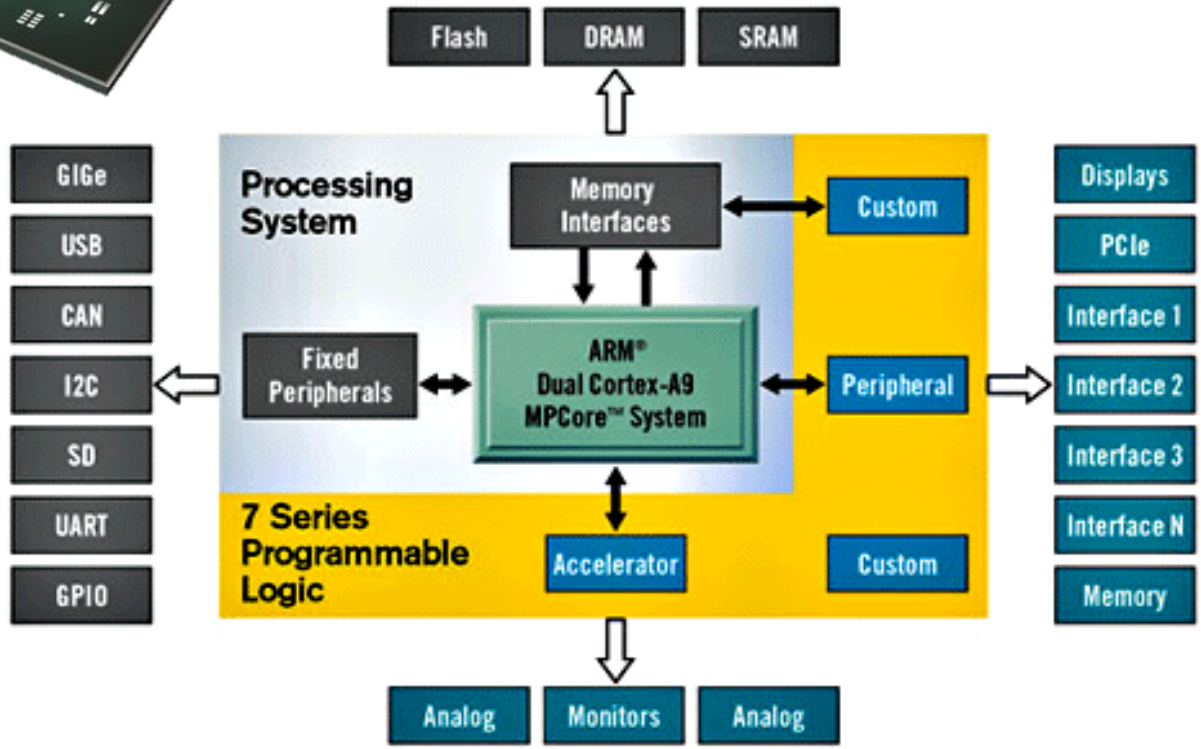
- **General-purpose integrated circuits**
  - **Microprocessors**, digital signal processors, ***FPGA*** and memories
- **Application-specific integrated circuits (ASIC)**
  - Designed for a narrow range of applications
  - Full-custom ASIC
  - ***Standard-cell ASIC***



Devices (heterogeneous)



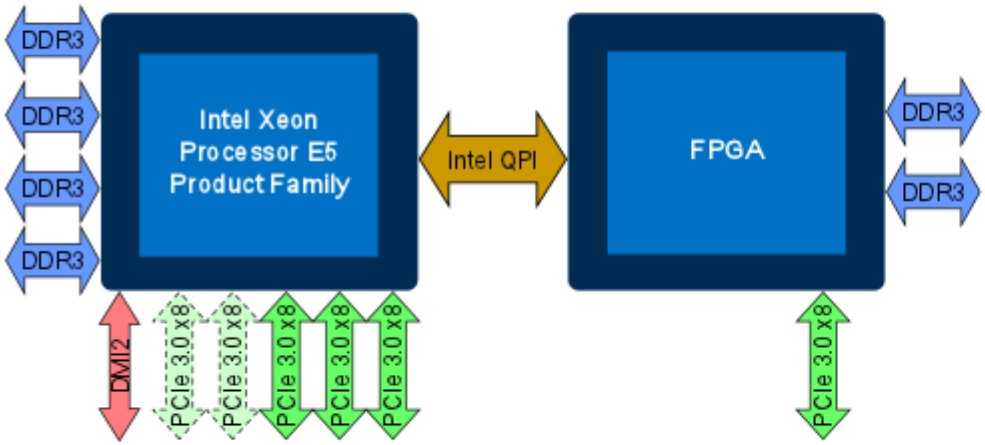
All Programmable SoC



Devices

Intel® Xeon® Processor + Field Programmable Gate Array Software Development Platform (SDP) Shipping Today

Software Development for Accelerating Workloads using Intel® Xeon® processors and coherently attached FPGA in-socket



Processor	Intel® Xeon® Processor E5
FPGA Module	Altera® Stratix® V
QPI Speed	6.4 GT/s full width (target 8.0 GT/s at full width)
Memory to FPGA Module	2 channels of DDR3 (up to 64 GB)
Expansion connector to FPGA Module	PCI Express® (PCIe) 3.0 x8 lanes - maybe used for direct I/O e.g. Ethernet
Features	Configuration Agent, Caching Agent, (optional) Memory Controller
Software	Accelerator Abstraction Layer (AAL) runtime, drivers, sample

Available as part of Intel & Altera co-sponsored Hardware Accelerator Research Program

IDF15 INTEL DEVELOPER FORUM

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- Why Digital?
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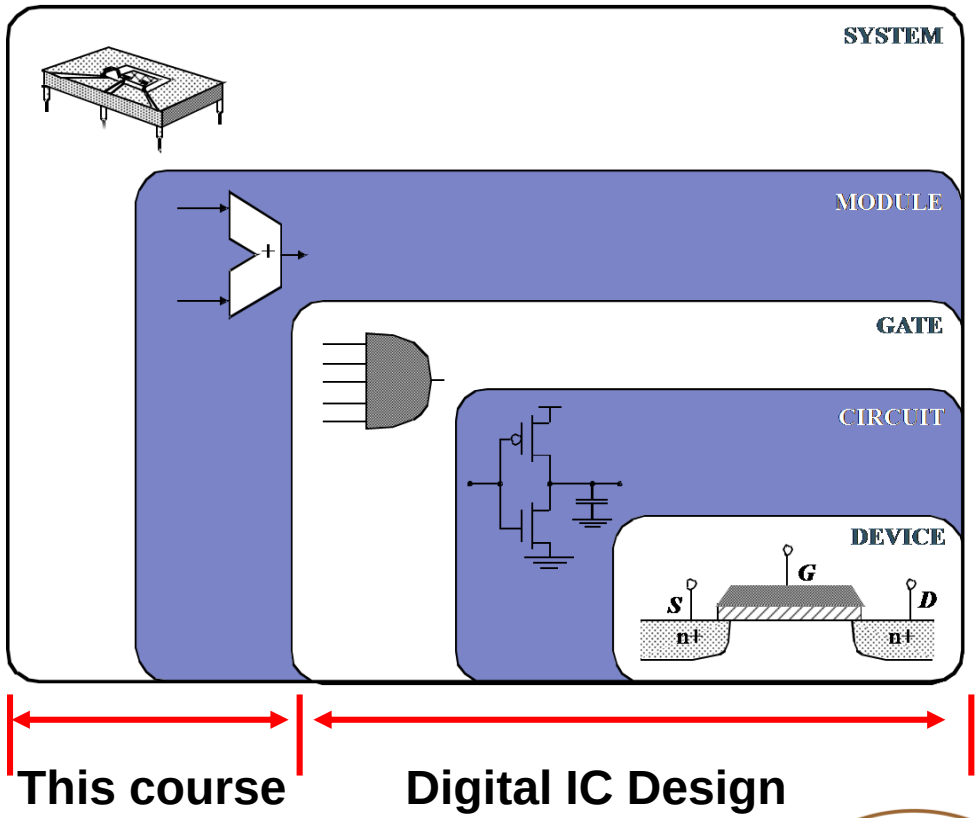
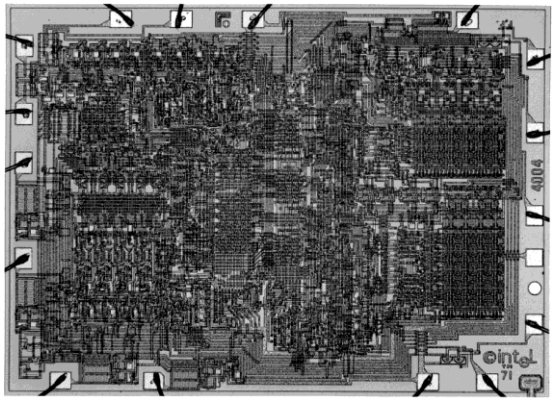
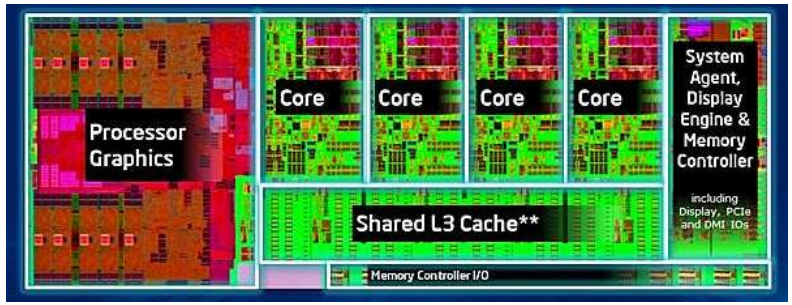
System Representation

- System
  - SoC: a CPU chip …
- Module
  - Macro cell in a chip : ALU…
- Gate
  - Basic logic block : xor, nor…
- Circuit
  - Transistors
- Device
  - Gate, source, drain



View a Design in a Proper Way





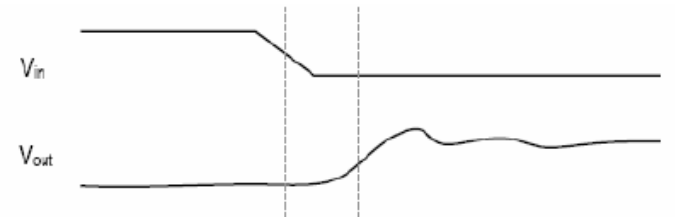
Intel 4004 (2.3K transistors)

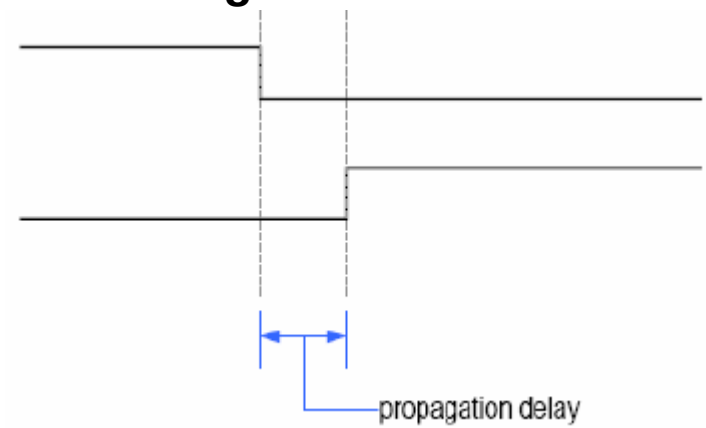
Full-custom

Intel Haswell (1.4B transistors)

?

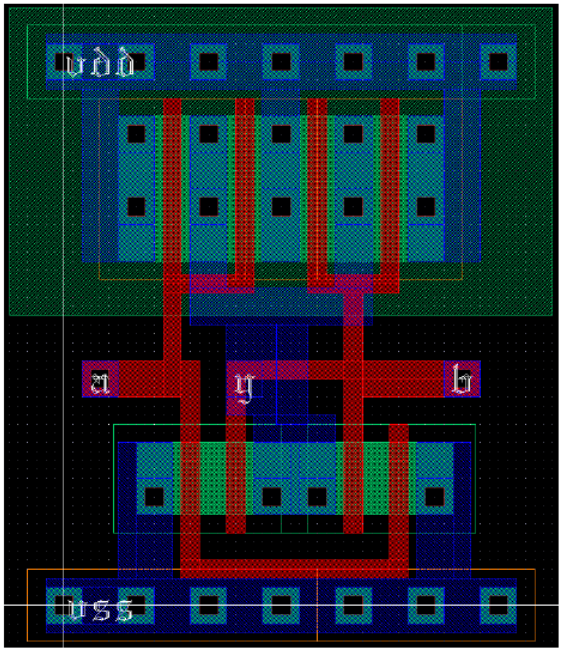
- **Abstraction: simplified model of a system**
  - **Show the selected features accurate enough**
  - **Ignore the others**





VLSI Design Flow

- **Evolution of circuit design (Design Hierarchy)**
  - Full-custom⇒Design-automation
    - ***Based on library cells and IPs***
    - ***Top-down methodology***
  - Design abstraction⇒“Black box” or “Model”
    - ***Parameter simplification***
    - ***Accurate enough to meet the requirement***



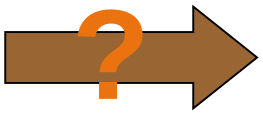

```
module HS65_GH_NAND2AX14 (Z, A, B);
   output Z;
   input A,B;
   not    U1 (INTERNAL1, B) ;
   or   #1 U2 (Z, A, INTERNAL1) ;
   specify
     (A +=> Z) = (0.1,0.1);
     (B -=> Z) = (0.1,0.1);
   endspecify
endmodule // HS65_GH_NAND2AX14
```

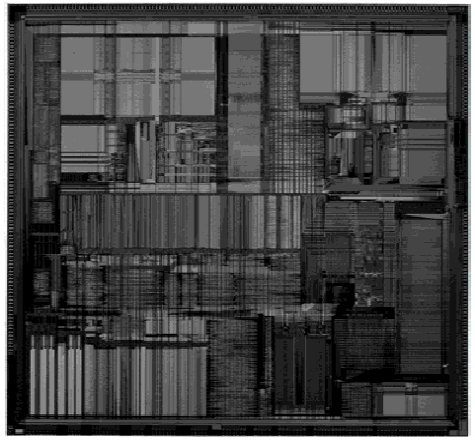
Outline

- Why Digital?
  - Advantages
  - Some applications
- History & Roadmap
- Device Technology & Platforms
- System Representation
- **Design Flow**
- RTL Basics

VLSI Design

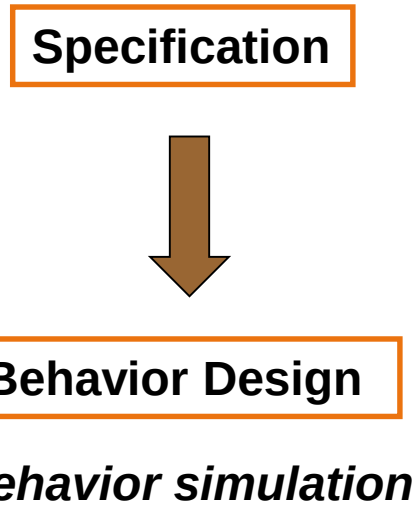
- **Set of specification:**
  - What does the chip do?
  - How fast does it run?
  - How reliable will it be?
  - How is the silicon area?
  - How much power will it consume?
  - ……





VLSI Design Flow

- An iterative process that transfer the specification to a manufacturable chip through at least five levels of design abstraction.



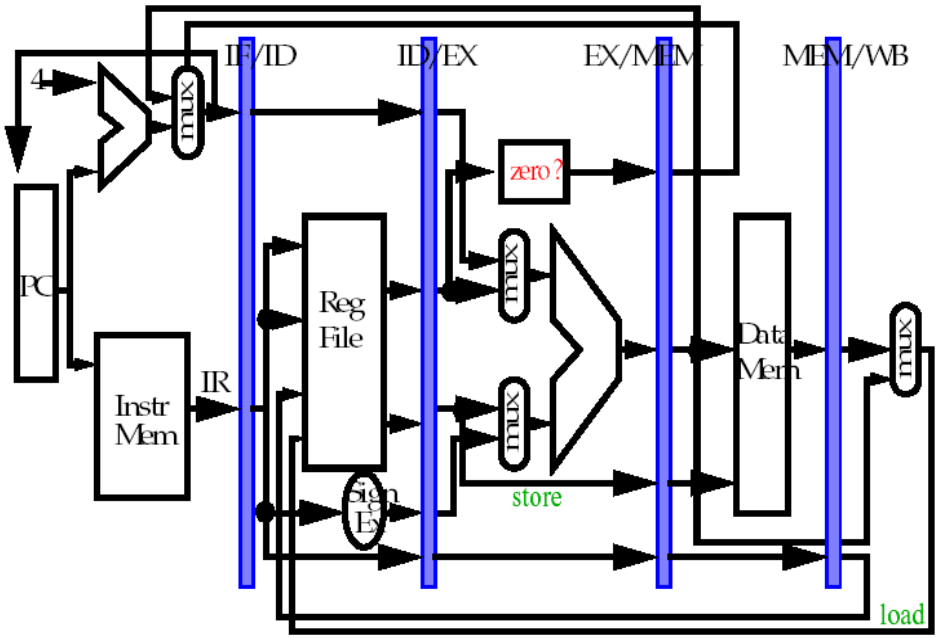
Function, performance, definition: English

Behavior, algorithm: C/C++, SystemC, Matlab …

VHDL
Verilog

Register Transfer Level Design

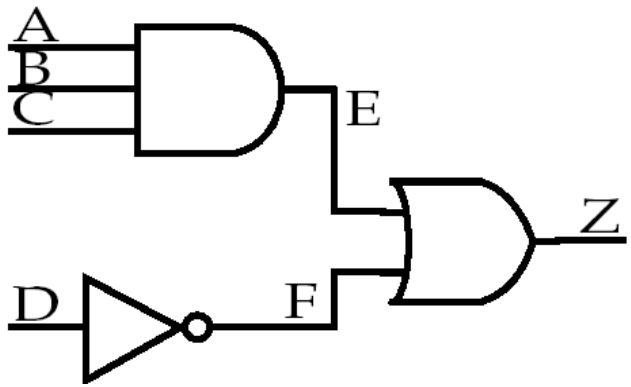
RTL simulation



Synthesis

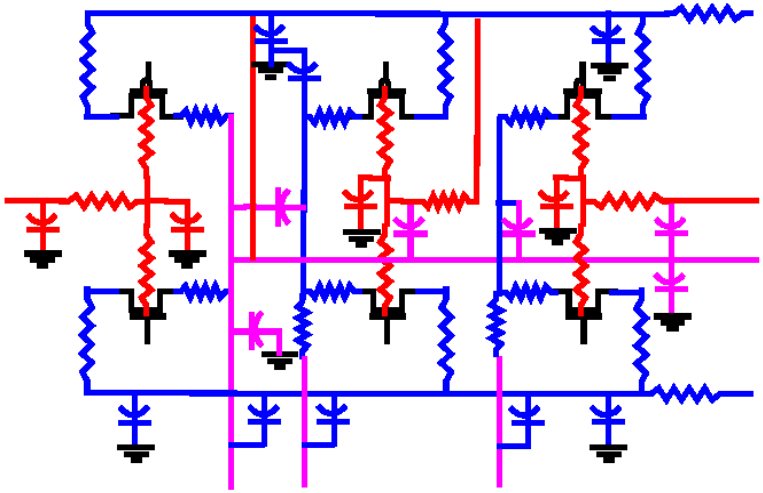
Logic Design

Gate-level simulation
Timing analysis
Power analysis



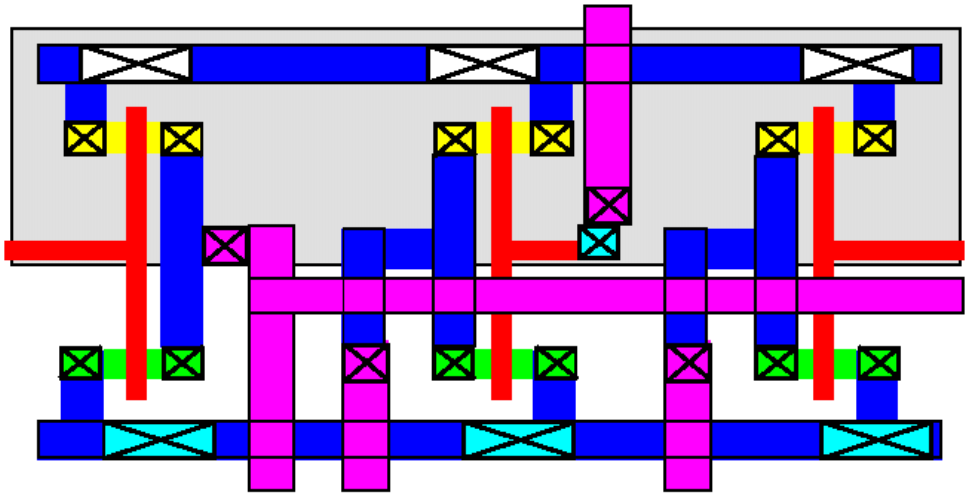
Custom Design

Circuit Design



Layout

Physical Design



Design rule checking
Post layout simulation

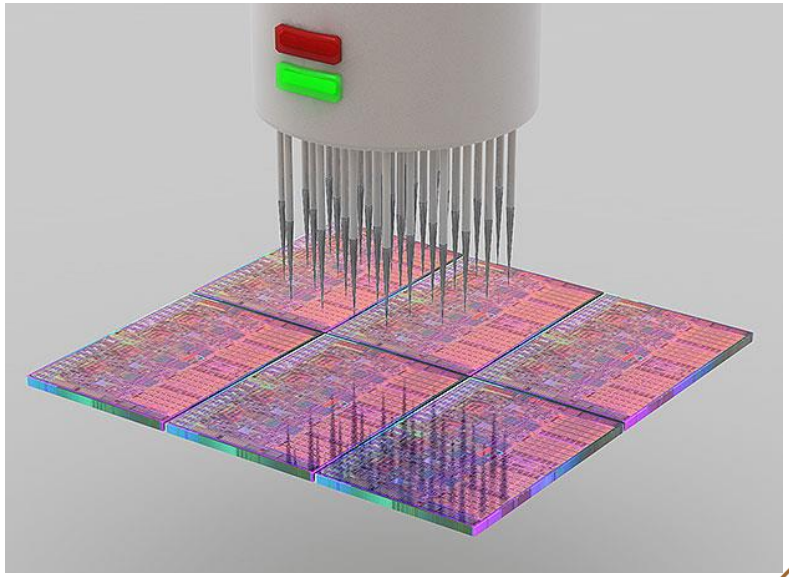
Verification

- **Verification**
  - Check whether a design meets the specification and performance goals
- **Two aspects**
  - ***Functionality***
  - ***Performance (timing/power/area)***
- **Method of Verification**
  - **Simulation**
    - ***Spot check: cannot verify the absence of errors***
    - ***Can be computation intensive***
  - **Timing analysis**
    - ***Just check delay***
  - Formal verification
    - ***Apply formal math techniques determine its property***
    - ***E.g, equivalence checking***
  - **Hardware emulation**

Fabrication

Testing

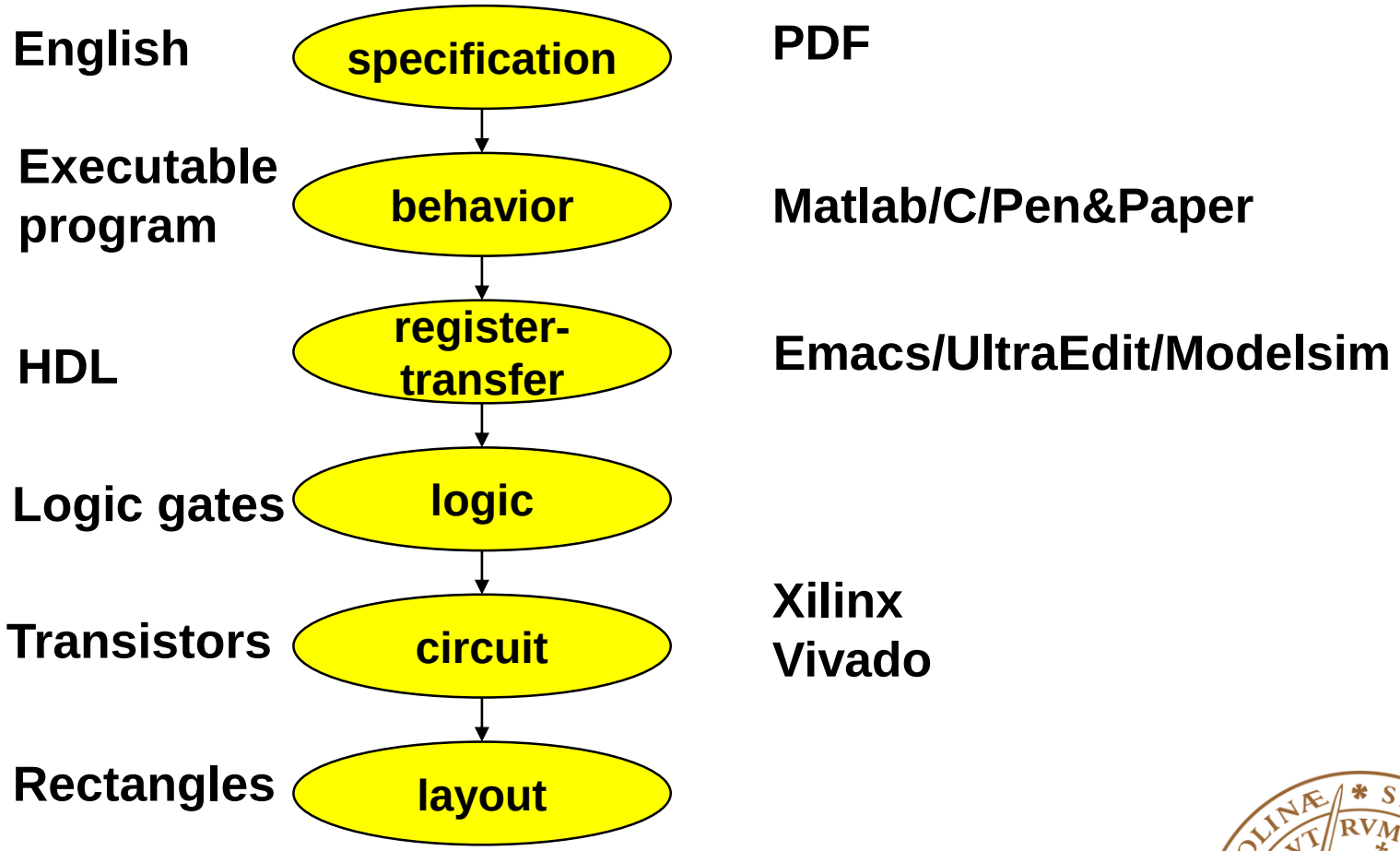
- **Testing is the process of detecting physical defects of a die or a package occurred at the time of manufacturing**
- **Testing and verification are different tasks.**
- **Difficult for large circuit**
  - Need to add auxiliary testing circuit in design
  - E.g., built-in self test (BIST), scan chain etc.



VLSI Design Flow: Tools

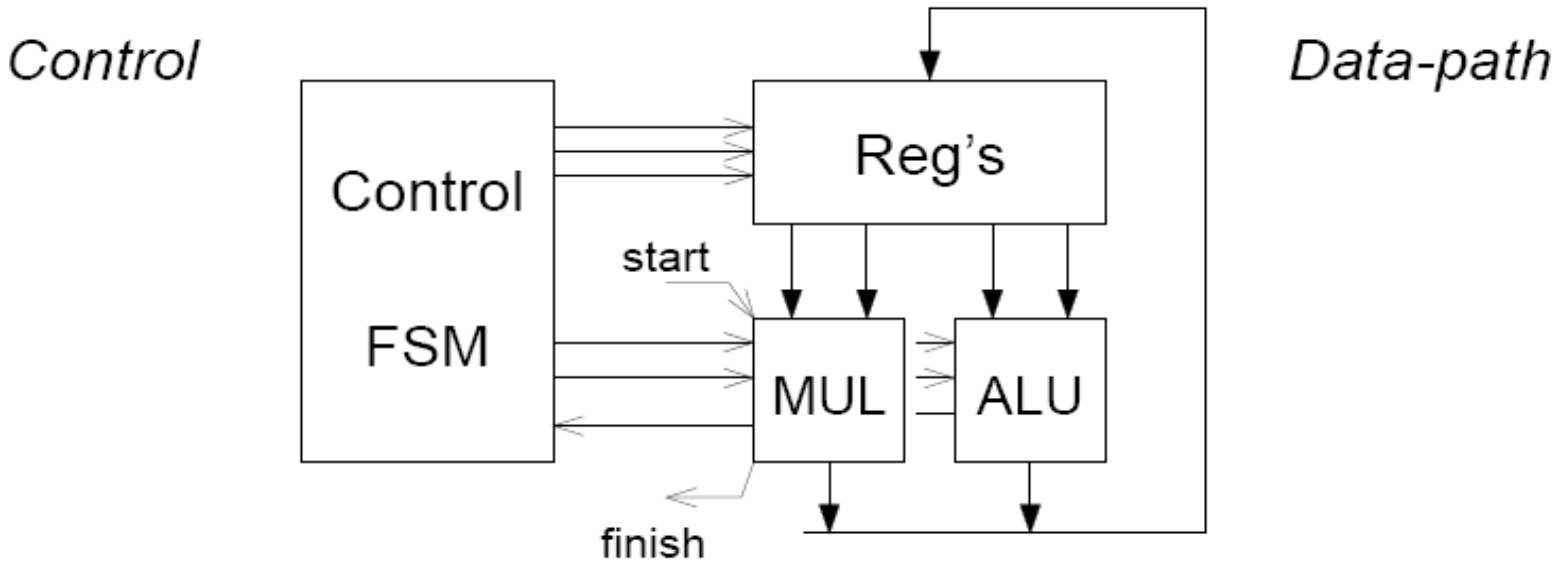
- **Algorithm**
  - **Matlab**
- **RTL Simulation**
  - ***Modelsim, Mentor***
  - VCS, Synopsys
  - VerilogXL, Cadence
- **Logic Synthesis**
  - **Design Compiler, Synopsys**
  - Blast Create, Magma
- **Transistor Simulation**
  - **Hspice/Starsim, Synopsys**
  - Spectra, Cadence
  - Eldo, Mentor
- **Mixed-Signal Simulation**
  - **AMS Designer, Cadence**
  - ADMS, Mentor
  - Saber, Synopsys
- **Place & Route**
  - Astro, Synopsys
  - **Silicon Encounter, Cadence**
  - Blast Fusion, Magma
- **Layout**
  - **Icfb/Dracula, Cadence**
  - ICstation/Calibre, Mentor
- **FPGA**
  - ***Vivado, Xilinx***
  - Quatus, Altera

VLSI Design Flow: Summary



Following slides should fresh up your memory

Overall VLSI Structure

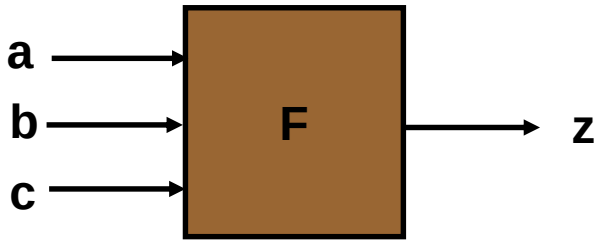


- **Scheduling / ordering / sequencing of operations**
- **Mapping / allocation:**
  - Variables -> {Reg1, ... ,RegN}
  - Operations -> {MUL, ADD, ALU, ... ,}

We will implement something similar in this course

Two Basic Digital Components (What)

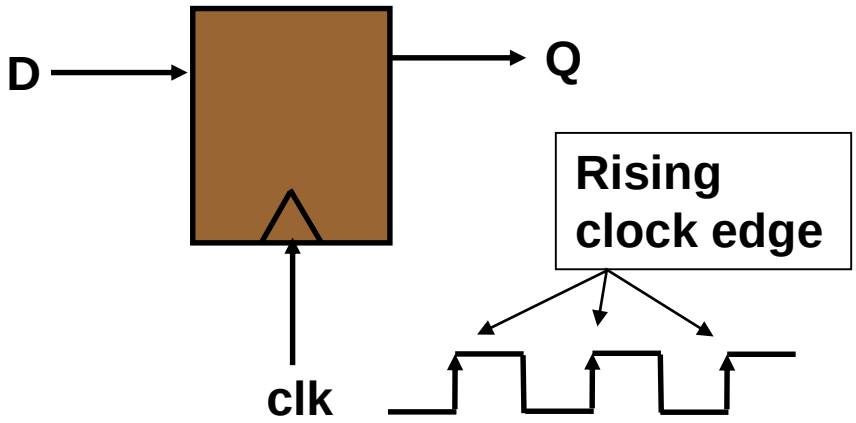
Combinational Logic



Always:
z <= F(a, b, c);

i.e. a function that is always evaluated when an input changes. Can be expressed by a truth table.

Register



if clk' event and clk= '1' then
Q <= D;

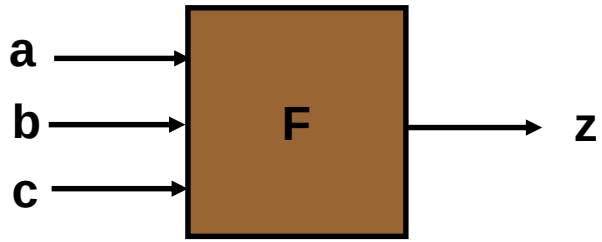
i.e. a stored variable, Edge triggered D Flip-Flop with enable.

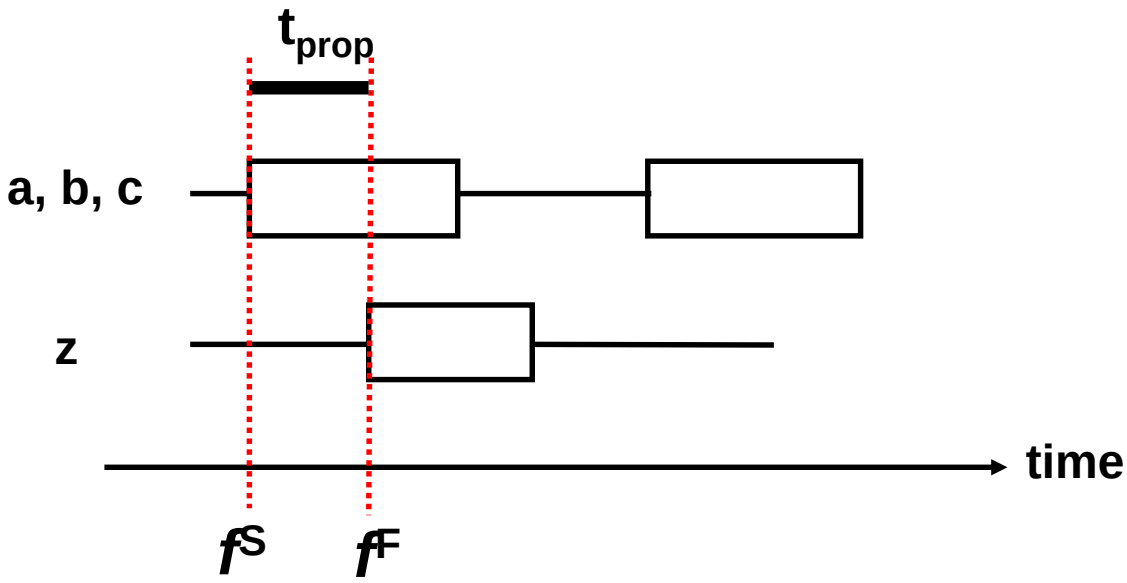
Timing (When)

Only if we guarantee to meet the timing requirements

... do the components guarantee to behave as intended.

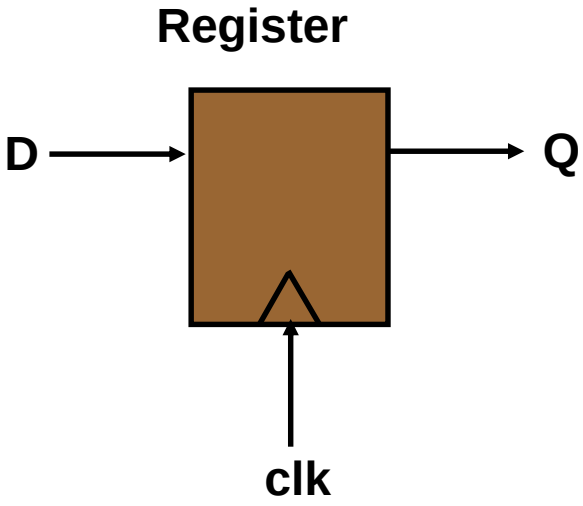
Combinational Logic Timing

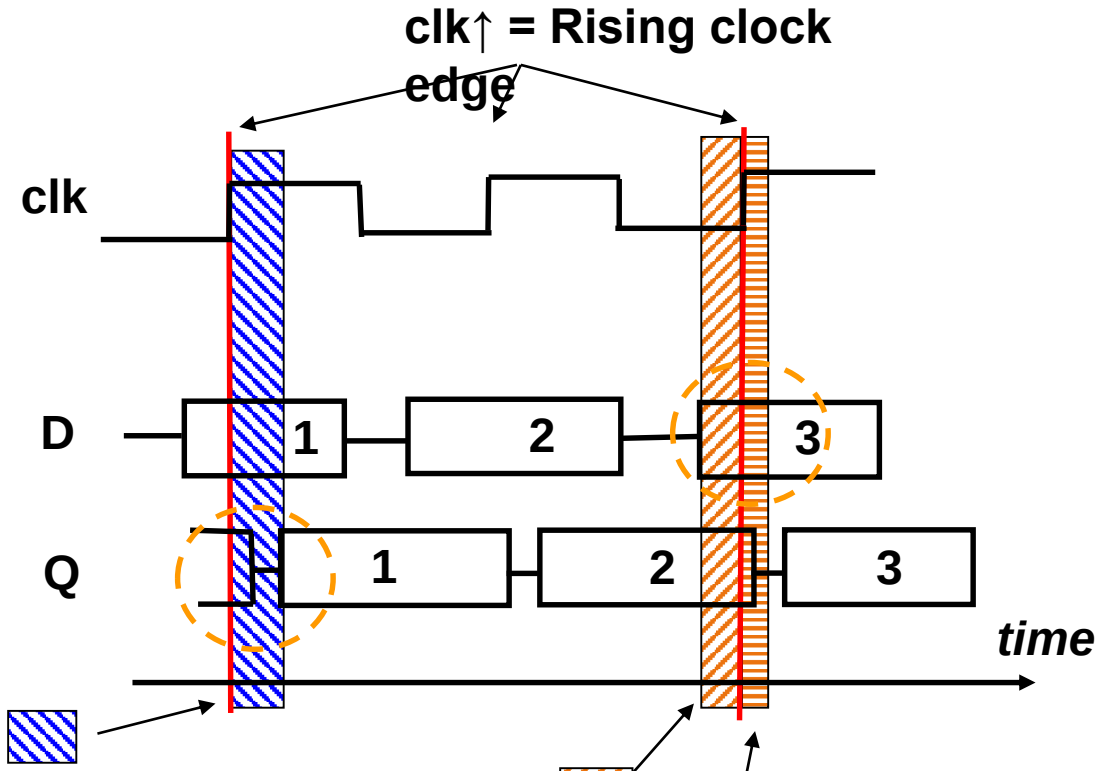




- **Propagation delay:**
  After presenting new inputs
  Worst case delay before producing correct output

Register timing





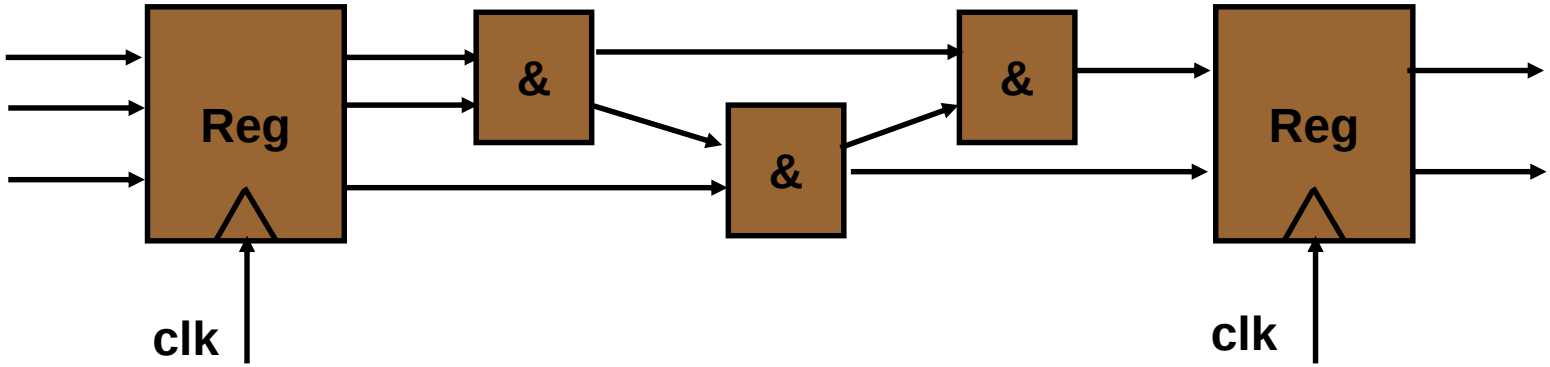
Propagation delay (clk_to_Q):
Worst case (maximum) delay after clk↑ before new output data is valid on Q.

Setup time:
Minimum time input must be stable before clk↑

Hold time:
Minimum time input must be stable after clk↑

Clock Frequency (RTL)

- What is the maximum clock frequency?



Register

Propagation delay:	Tckl-Q	250ps
Setup time:	Tsu	200ps
Hold time:	Th	100ps

AND-gate

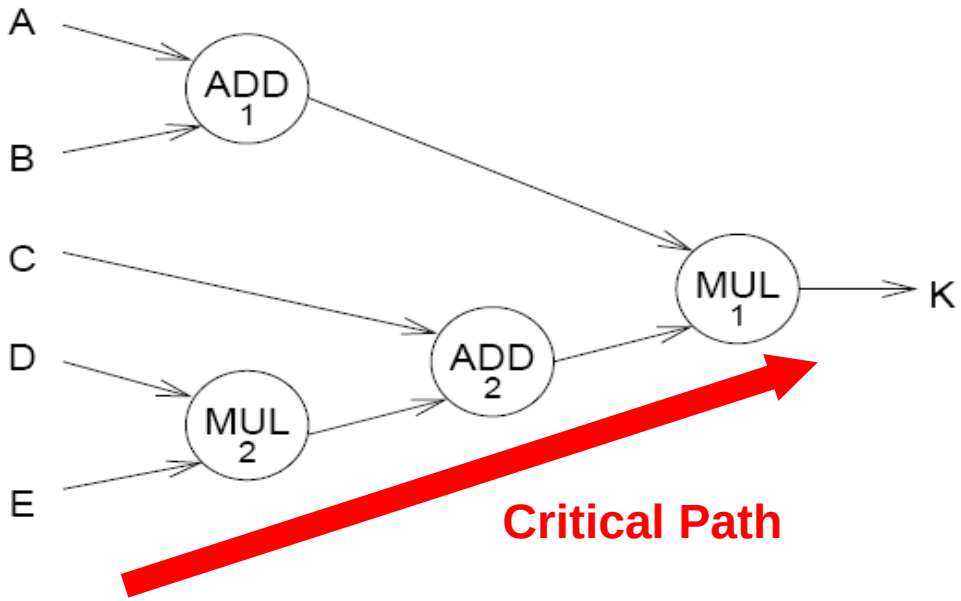
Propagation delay:	Tprop	250ps

250+250×3+200=1.2ns

***f*=833MHz**

Critical path

- …begin to explore the construction of digital systems with complex behavior
  - Example: K = (A $+_1$ B) $*_1$ (C $+_2$ D $*_2$ E)
- Combinational circuit:



Thanks