EITF35: Introduction to Structured VLSI Design

Part1.1.1: Course Introduction

Liang Liu
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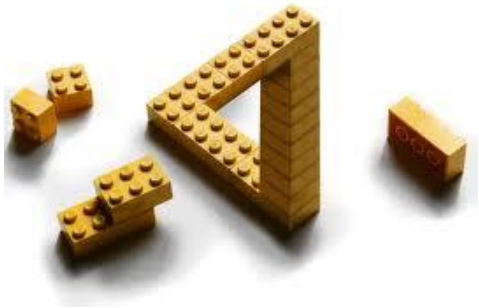
Course Factor

- **Introduction to Structured VLSI (very large scale integration) Design (7.5HP)**

http://www.eit.lth.se/course/eitf35

Digital IC



This Course

Outline

- Course Objective
- Teachers
- Lectures and Labs
- Language, Tools, Device
- Assignments
- Examination
- What's next

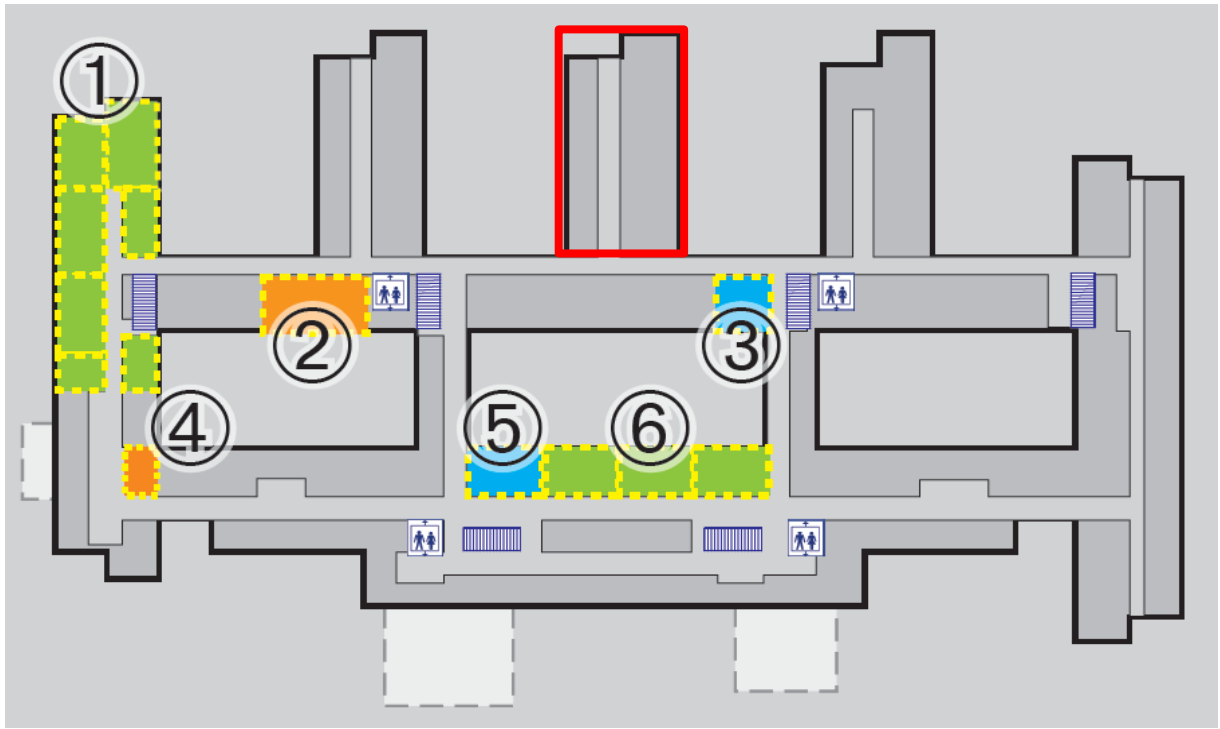
Course Objective

- **To introduce the basic concept and knowledge on digital VLSI realization**
  - Typical function blocks of a large digital system, controller (state machines), datapaths, storage elements
  - Optimization techniques for area, speed, and power
- **To provide the basic VHDL knowledge, design flow and tool training**
- **To provide real-life digital VLSI design experience**
  - Fast prototyping several assignments and projects on commercial FPGA platform

Teachers

Lecture

- Liang Liu, Associate Professor
- Email: liang.liu@eit.lth.se
- Room: E2342
- Homepage: http://www.eit.lth.se/staff/Liang.Liu



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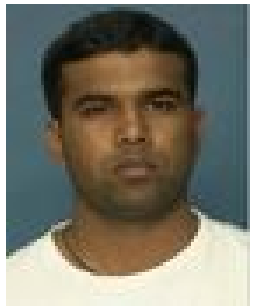
Teaching Assistants

- Rakesh Gangarajaiah
- Mojtaba Mahdavi
- Steffen Malkowsky
- Siyu Tan



Rakesh Gangarajaiah

Mojtaba Mahdavi

Steffen Malkowsky

Siyu Tan

Guest Lecturers

Guest Lecturers from EIT

- Erik Larsson, Associate Professor

Invited Lecturers from Industry

- Charlotte Sköld, Manager, Digital ASIC, Business Unit Radio at Ericsson

- Stefan Lundberg, Expert Technologies Engineer, Axis
  - ASIC history
  - Practical ASIC projects
  - New-starters
  - Security electronics
  - Consumer electronics
  - Industrial trends
  - Camera technology

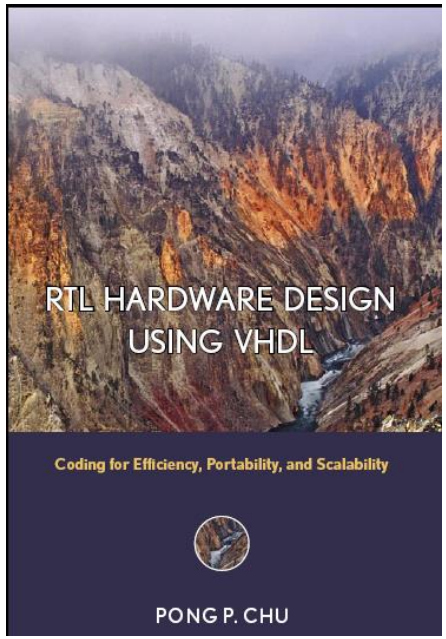
Book Recommendation

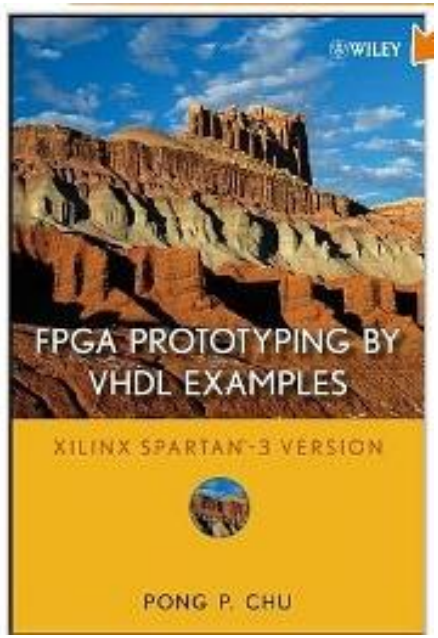
RTL Hardware Design Using VHDL

- Coding for Efficiency, Portability, and Scalability
- Pong P. CHU

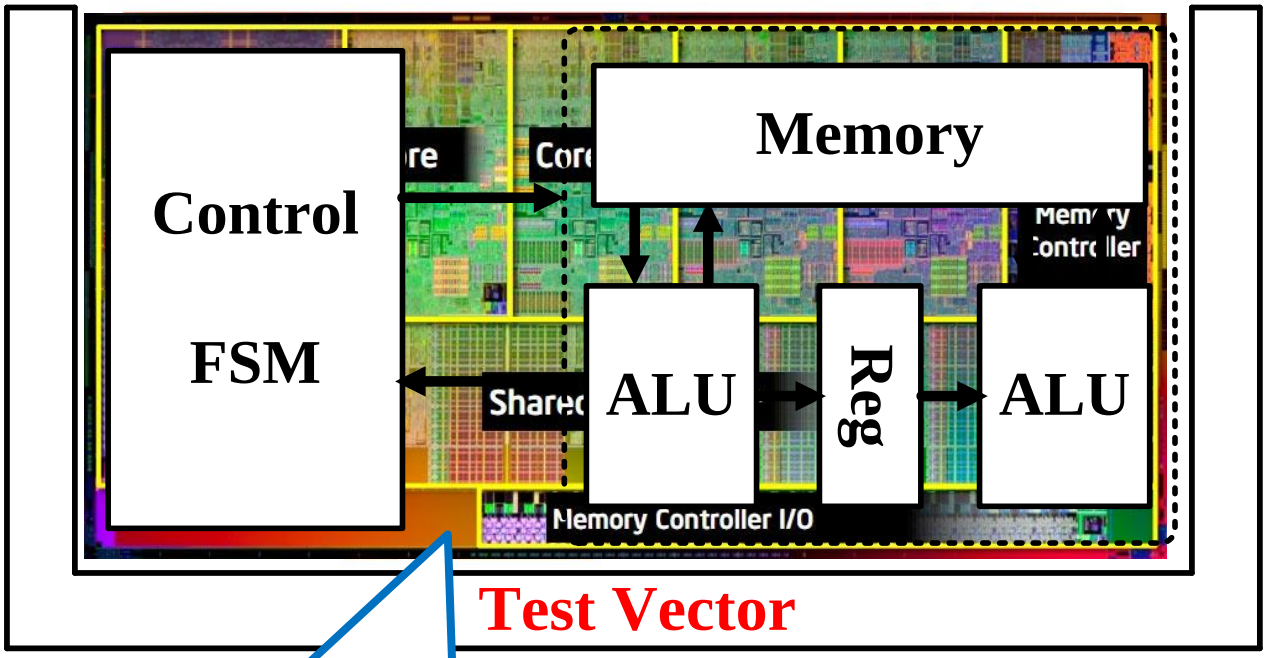
FPGA Prototyping by VHDL Examples

- Xilinx Spartan-3 Version
- Pong P. CHU





Course Content & Schedule



- Concept &Theory
- VHDL Knowledge
- Assignment & Project

- Overview
- Controller
  - FSM
- Data-Path
  - Combinational circuit
  - Sequential circuits
  - Storage elements
- Test & Verification
- FPGA
- Design Optimization

Lectures and Labs

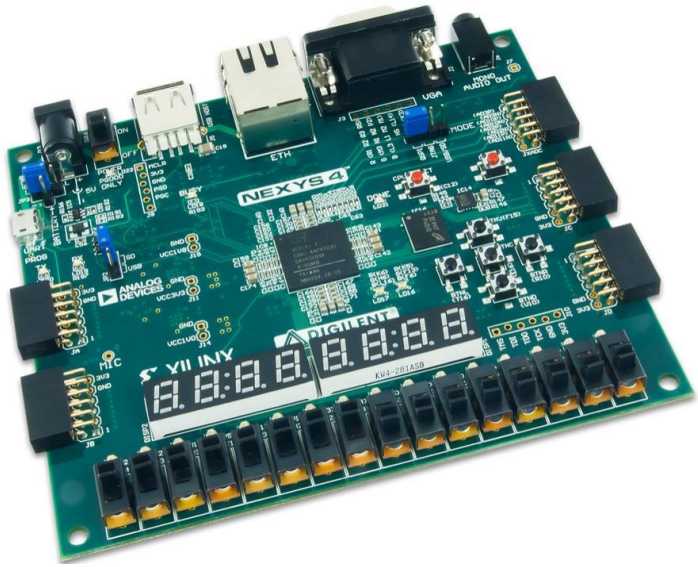
- **Lectures (10)**
  - **Monday: 13:15-15:00**
  - **Tuesday: 13:15-15:00**
  - **Check lecture rooms here: https://se.timeedit.net/web/lu/db1/lth1/ri11565740000YQQ95Z5587057y5Y3013gQ6g5X6Y55ZQ276lZ6Qu00.html**

  In the 1st Week a lecture on FPGA and Vivado will be given for Friday at 13:15

- **Labs E:4121** **Group A** **Group B**
  - **Wednesday** **13:00-15:00, 15:00- 17:00**
  - **Thursday** **13:00-15:00, 15:00-17:00**
  - **Friday** **08:00-10:00, 10:00-12:00**
  - **Friday** **13:00-15:00, 15:00- 17:00**
  - **Will present the assignments before the lab**
  - **Each group will have 3 lab slots with TA's per week**
- **Labs are accessible 24/7 if not occupied by other courses**
- **You need to sign up for the lab before you can get access**
  - **Regisit as team of 2 students**

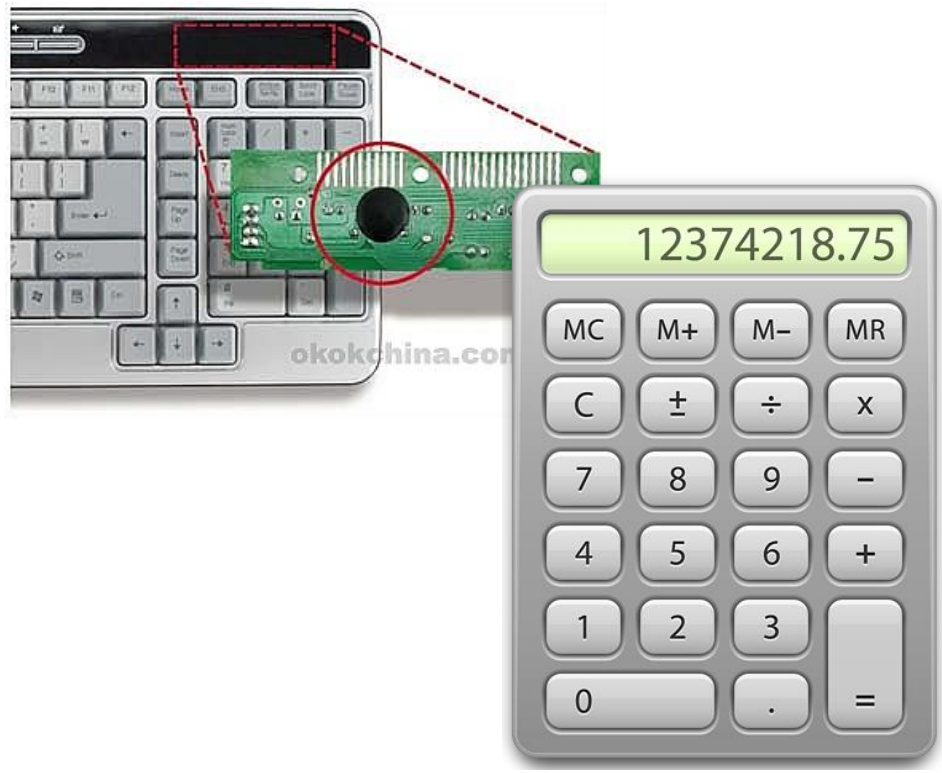
Language, Tools, Device

- **Language**
  - VHDL (Verilog) will be used to develop the circuits
- **Tools**
  - Xilinx Vivado
  - Modelsim (QuestaSim): VHDL simulator
- **Device**
  - XILINX Nexys 4



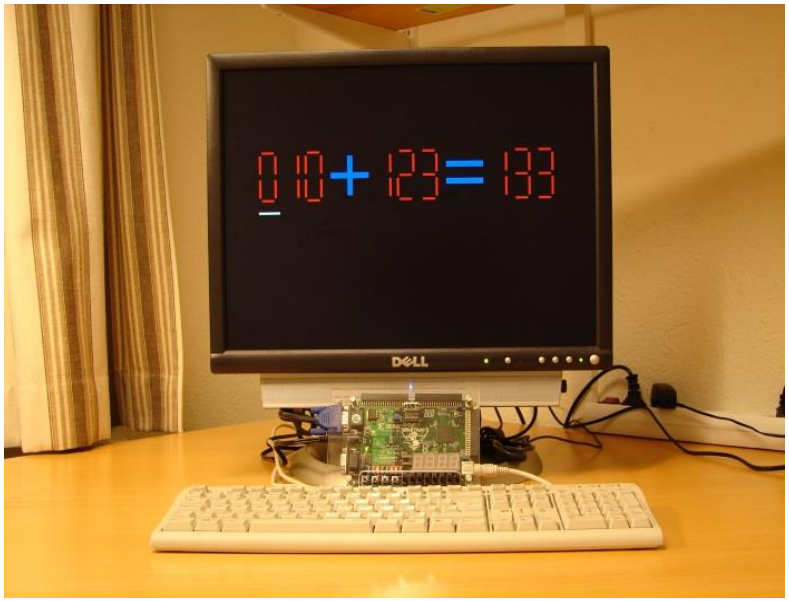
Assignments

- **To pass the course, 3 assignments need to get approved**
  - Sequence Detector
    - ***Simulation***
  - Keyboard Controller
    - ***FPGA implementation***
  - Alrithmetic Logic Unit (ALU)
    - ***FPGA implementation***

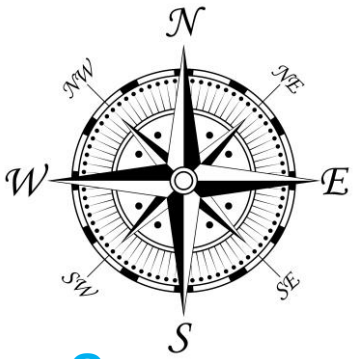


- **Assignments approved in time will result in grade 3**

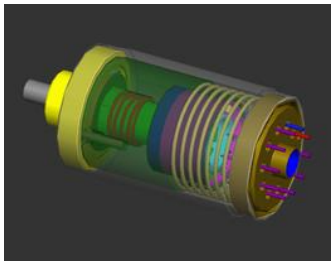
Assignments cont'd



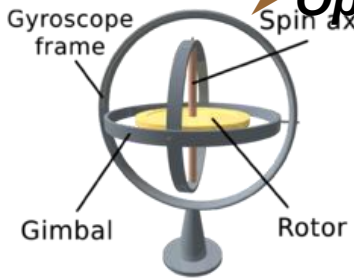
- **Extra projects are required to get grade 4 /5**
  - FPGA implementation (4)
    - ***ALU with input memory***
    - ***ALU output on VGA***
  - Advanced arithmetic funtion in the ALU (5)
    - ***Optimize for area and/or speed constraint***
    - ***Utilize sensor on the FPGA***
    - ***Open projects***



Compass



Accelerometer



Gyroscope

Examination

Before the lab

- All assignments must be prepared and handed in
- Without preparation you are NOT allowed to continue the lab

Examination cont'd

Design Approval

- **All assignments must be demonstrated to the TA's to get approved before deadline**
- **Students need to demonstrate their understanding of the assignment to get it approved**
- **Graded as a team, but individual grading may be applied if an ”unbalance” is discovered**
  - Both team members need to be present at design approval
  - Oral test might be given to both team members

Examination cont'd (new this year)

Good news

Before

- Assignment 1
  - ***Deadline 1***
- Assingment 2
  - ***Deadline 2***

  ...
- Assingment 5
  - ***Deadline 5***

This year

- Assignment 1
- Assingment 2

  ...
- Assingment 5

- ***Deadline: Oct 28, 17.00***

Examination cont'd (”new” this year)

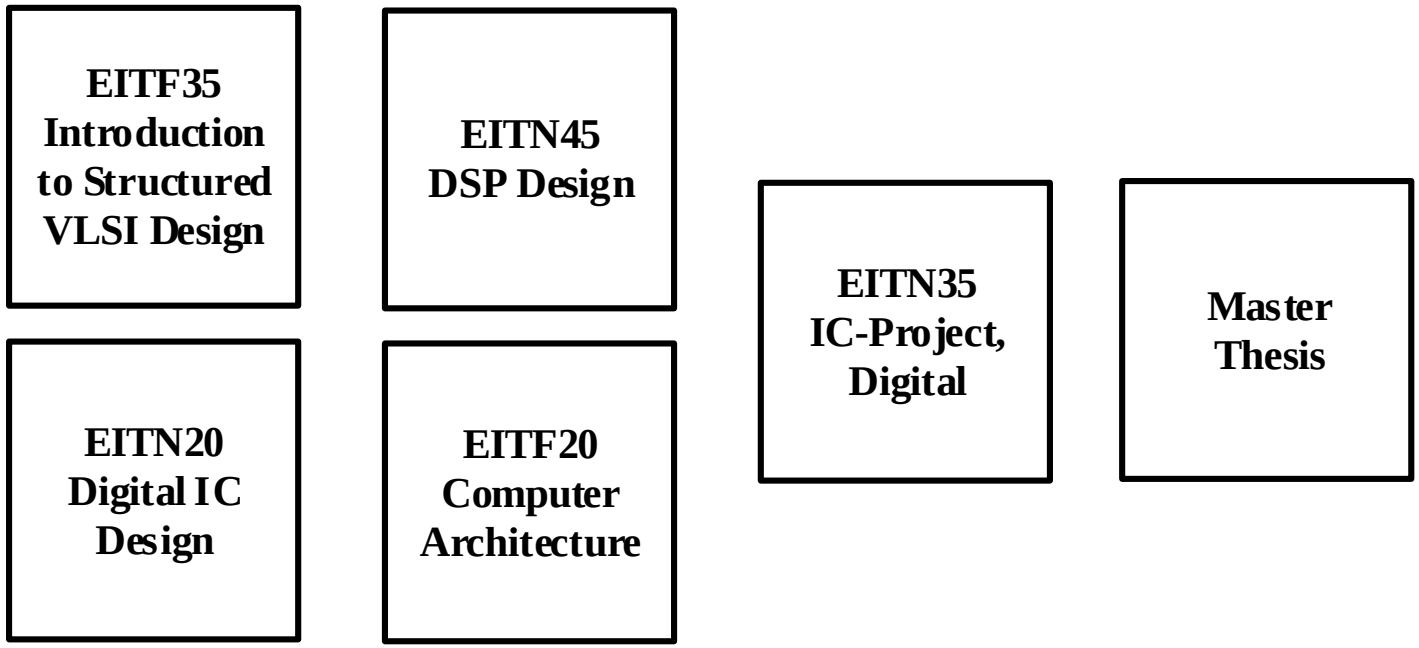
”Bad” news

- Very strict check during project approval
  - Application of learned knowledge
  - Good VHDL (verilog) coding style
  - Understanding of circuits and timing
  - ...

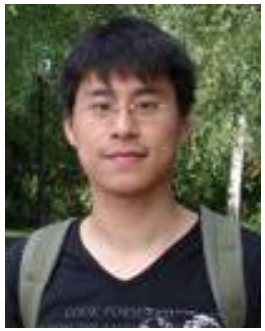
Next Step

What can we do after finishing this course?

Digital Path



Digital Path



Chenxin Zhang

Intro. VLSI (mouse control)

DSP Design IC Project Comp. Arc. (MIPS processor)

Master Thesis (multi-core MIPS)

PHD (Processor for LTE-A.)

MediaTek (Processor for LTE-A.)

Projects and Thesis (University)

- **Ultra-fast laser measurement**
  - Cooperate with Anne L'Huillier (committee Chair, Nobel Physics Prize) in Atomic Physics
- **Implementation of readout system for a prototype detector in particle physics**
- **ESS, MAX IV**

EUROPEAN SPALLATION SOURCE

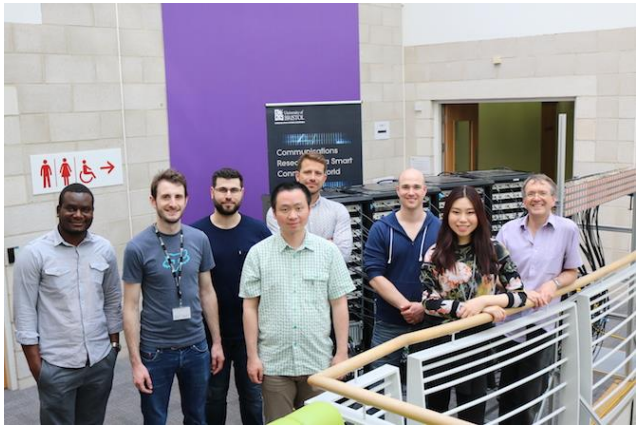
Projects and Thesis (industry)

Researches at EIT

Leading 5G research

Bristol and Lund once again set new world record in 5G wireless spectrum efficiency

Press release issued: 17 May 2016



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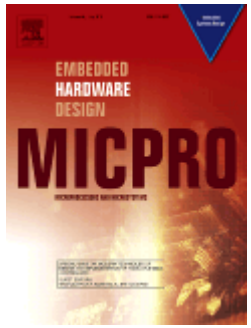
Other Opportunities

NORCAS

JTRES 2016

29 Aug. - 2 Sept.
Lugano, Switzerland



International Conference and Journal

Xilinx FPGA and SOC University Design contest

The Xilinx Open Hardware Design Contest gives students the opportunity to showcase their technical and creative skills.

There are two project categories:

- **Embedded Design**
- **Digital design**

A prize of €1500 will be awarded to the best PhD, and under-graduate project in each category (4 prizes in total).

The winning participants will also receive sponsored travel to the Open Hardware awards ceremony in August 2016.

Questions?