Using the Xilinx ILA

This document briefly describes a project in which we will instantiate some Xilinx Ips using the IP generator. We will also use the Xilinx Integrated Logic Analyzer to perform on chip debug.

A block diagram of the design in the zip file is shown below. We will instantiate three IPs. The clock generator, the Dual port RAM and the integrated Logic analyser. The top level file also contains a counter which generates the write address, read address, write data to the simple dual port RAM when the top level start writes and start reads are set to high.

The Clock is connected to the onboard crystal oscillator, the reset start_writes and start_reads are connected to the first three switches on the board. The read data is connected to eight LEDs.
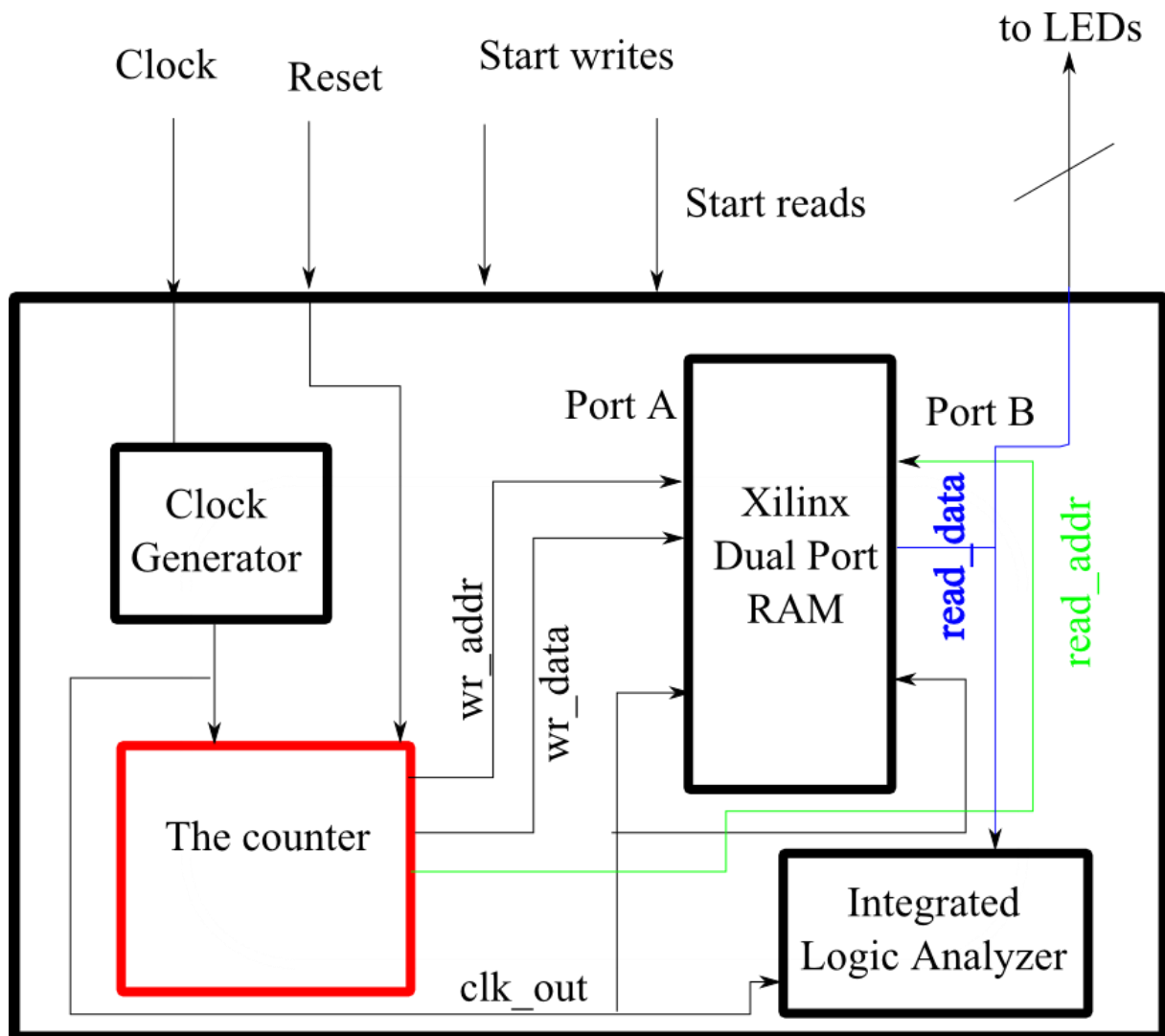

Figure 1: Example design

Generating the design:

- Create a new project and target the Artix-7 FPGA
- Add the top level file into the design sources
- Add the constraints
- Add the simulation TB
- Notice that there are three undefined blocks under your top level which need to be generated
- Choose the IP catalog and search for "Clock"
- Open the clocking wizard and generate a clock with one output pin with 100MHz clock frequency. Do not change anything else and click "generate"
  - The tool will update the file status and you should see the newly created clock generator under your top level file.
- Similarly instantiate a Simple Dual port RAM with data width of 8 bits and depth of 256.
- Instantiate the Integrated Logic Analyzer with a depth of 1024 points.

When you have successfully completed this, all the IPs will be defined and the files can be simulated.

Run a simulation and verify the counter operation.

Generate a bit file and verify that the ILA can capture the counter values.