EITF35: Introduction to Structured VLSI Design

Part1.1.1: Course Introduction

Liang Liu
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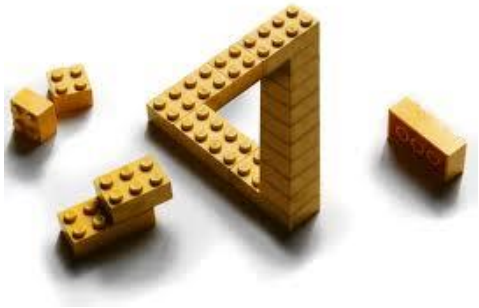
Course Factor

- **Introduction to Structured VLSI (very large scale integration) Design (7.5HP)**

http://www.eit.lth.se/course/eitf35

Digital IC



This Course

Outline

- Course Objective
- Teachers
- Lectures and Labs
- Language, Tools, Device
- Assignments
- Examination
- Continuation

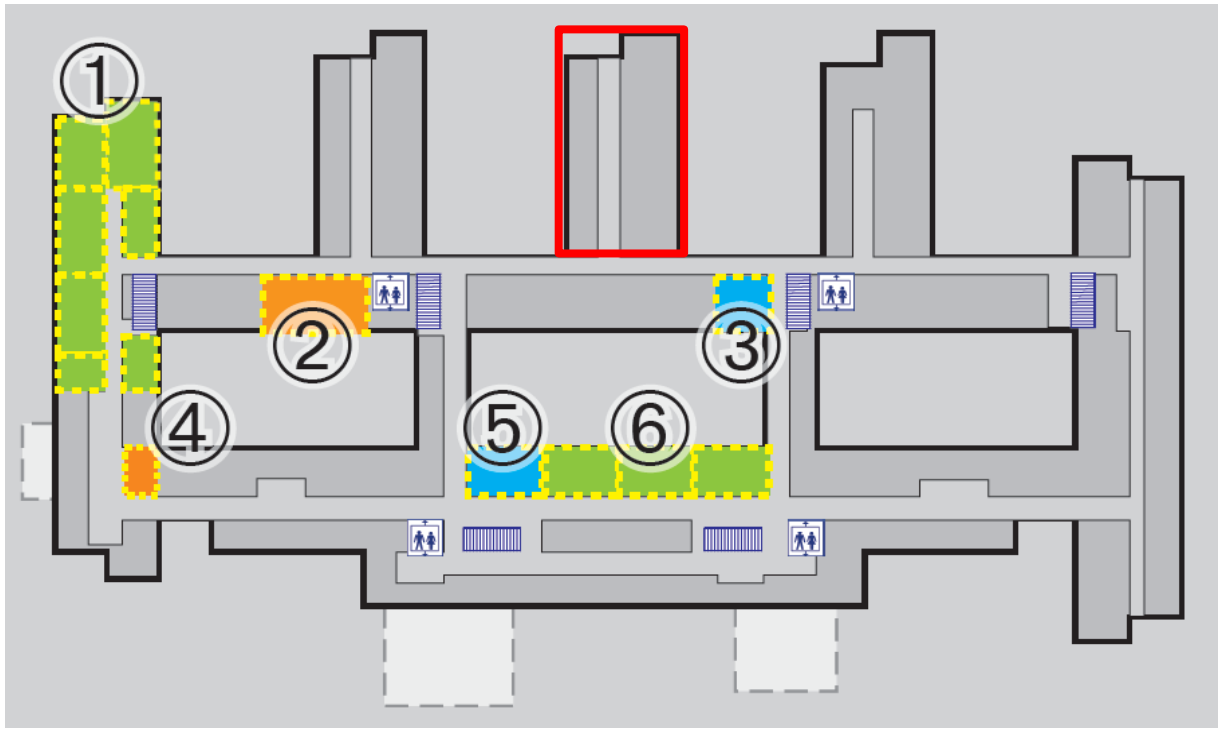
Course Objective

- **To introduce the basic concept and knowledge on digital VLSI realization**
  - Typical function blocks of a large digital system, controller (state machines), datapaths, storage elements
  - Optimization techniques for area, speed, and power
- **To provide the basic VHDL knowledge, design flow and tool training**
- **To provide real-life digital VLSI design experience**
  - Fast prototyping several assignments and projects on commercial FPGA platform

Teachers

Lecture

- Liang Liu, Assistant Professor
- Email: liang.liu@eit.lth.se
- Room: E2342
- Homepage: http://www.eit.lth.se/staff/Liang.Liu



Teachers

Lecture

- Liang Liu, Assistant Professor
- Email: liang.liu@eit.lth.se
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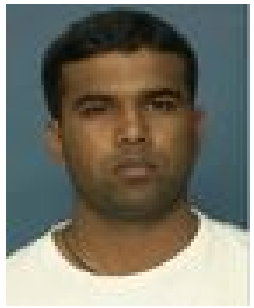
Teaching Assistants

- Rakesh Gangarajaiah
- Oskar Andersson
- Hemanth Prabhu
- Siyu Tan



Rakesh Gangarajaiah

Oskar Andersson

Hemanth Prabhu

Siyu Tan

Guest Lecturers

Guest Lecturers from EIT

- Erik Larsson, Associate Professor

Invited Lecturers from Industry

- Igor Tasevski, Head of Hardware Design Lund, Business Unit Radio at Ericsson

- Stefan Lundberg, Expert Technologies Engineer, Axis

ERICSSON

AXIS COMMUNICATIONS

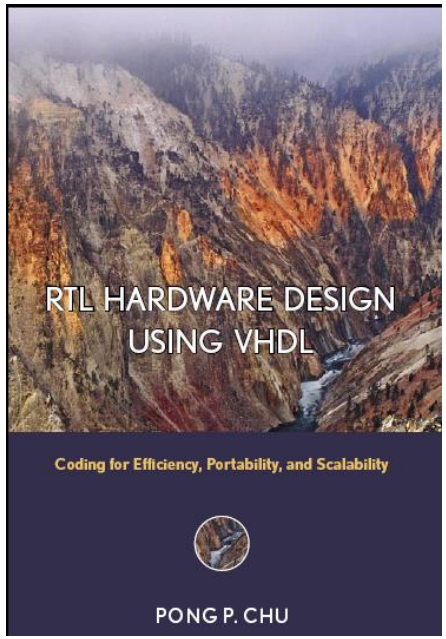
Book Recommendation

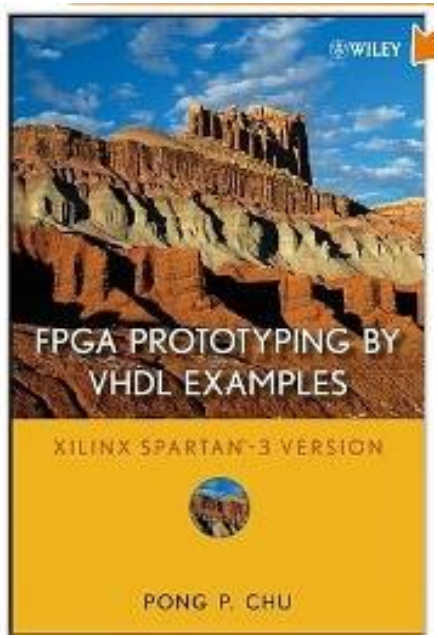
RTL Hardware Design Using VHDL

- Coding for Efficiency, Portability, and Scalability
- Pong P. CHU

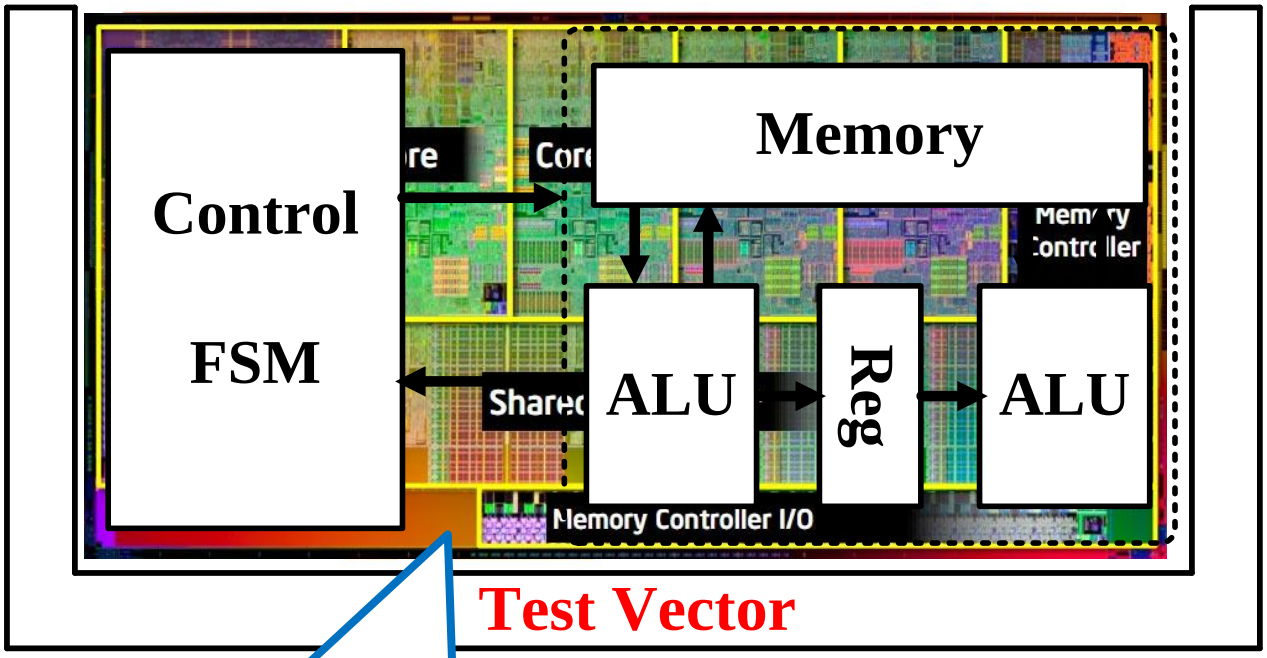
FPGA Prototyping by VHDL Examples

- Xilinx Spartan-3 Version
- Pong P. CHU





Course Content & Schedule



- Concept &Theory
- VHDL Knowledge
- Assignment & Project

- Overview
- Controller
  - FSM
- Data-Path
  - Combinational circuit
  - Sequential circuits
  - Storage elements
- Test & Verification
- FPGA
- Design Optimization

Lectures and Labs

- **Lectures (10)**
  - **Monday: 08:15-10:00 in E:2311**
  - **Tuesday: 08:15-10:00 in E:3308**

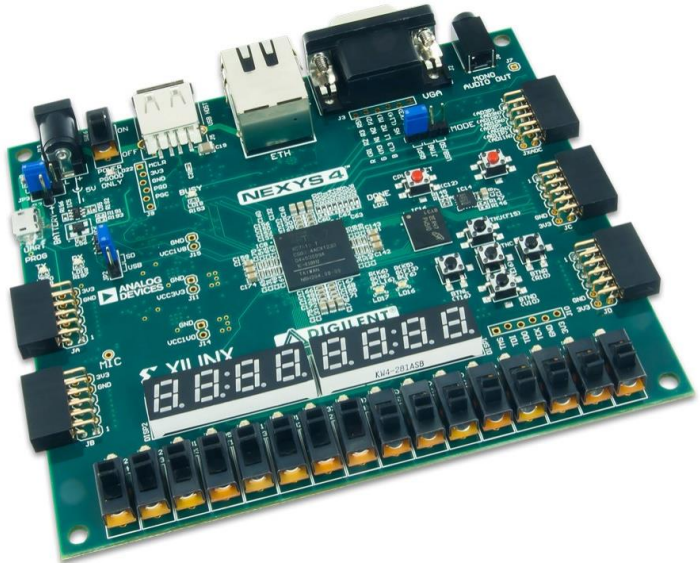
  In the 1st Week a lecture on FPGA and ISE will be given for Friday at 08:15 (E:3308)
- **Labs E:4121**

	Group A	Group B
Tuesday	13:00-15:00,	15:00-17:00
Wednesday	13:00-15:00,	15:00- 17:00
Thursday	13:00-15:00,	15:00-17:00
Friday	08:00-10:00,	10:00-12:00 (13:00-15:00, 15:00-17:00 from Week 38)

  - **Will present the assignments before the lab**
  - **Each group will have 3 lab slots with TA's per week**
- **Labs are accessible 24/7 if not occupied by other courses**
- **You need to sign up for the lab before you can get access to the 4th floor.**

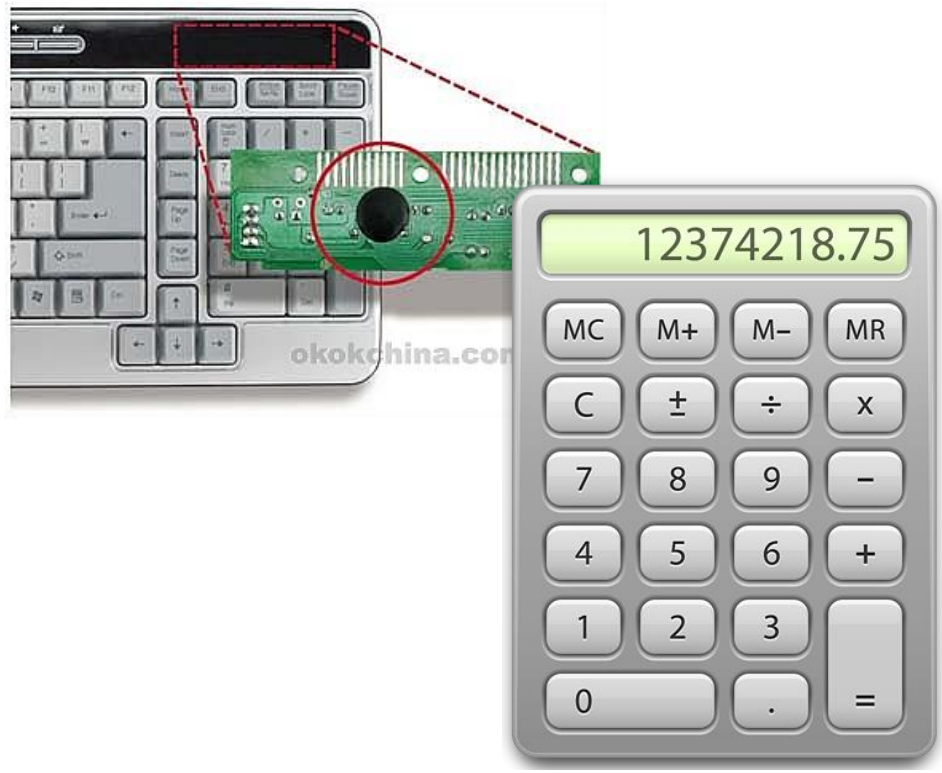
Language, Tools, Device

- **Language**
  - VHDL will be used to develop the circuits
- **Tools**
  - Modelsim (QuestaSim): VHDL simulator
  - Xilinx Vivado
- **Device**
  - XILINX Nexys 4



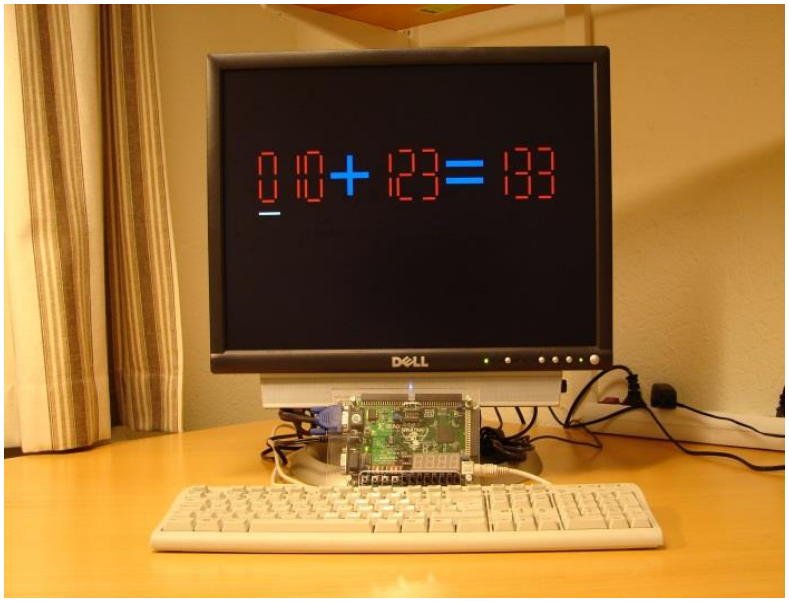
Assignments

- **To pass the course, 3 assignments need to get approved**
  - Sequence Detector
    - ***Simulation***
  - Keyboard Controller
    - ***FPGA implementation***
  - Alrithmetic Logic Unit (ALU)
    - ***FPGA implementation***



- **Assignments approved in time will result in grade 3**

Assignments cont'd



- **Extra projects are required to get grade 4 /5**
  - FPGA implementation
    - ***ALU with input memory***
    - ***ALU output on VGA***
  - Squre-root funtion in the ALU
    - ***Optimize for area and/or speed constraint***
    - ***Utilize sensor on the FPGA***
    - ***Open projects***

Examination

Before the lab

- All assignments must be prepared and handed in
- Without preparation you are NOT allowed to continue the lab

Examination cont'd

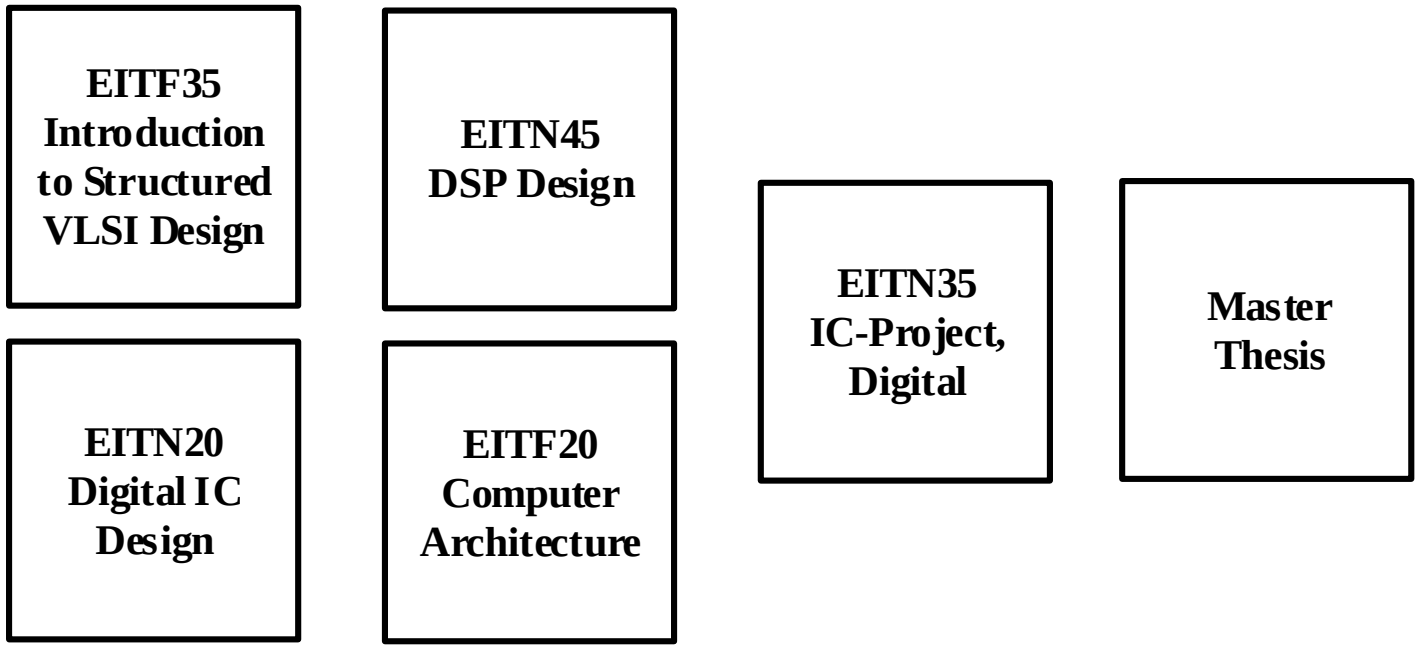
Design Approval

- **All assignments must be demonstrated to the TA's to get approved before deadline.**
- **Students need to demonstrate their understanding of the assignment to get it approved.**
  - Application of learned knowledge
  - Good VHDL coding style
  - Understanding of circuits and timing
- **Graded as a group, but individual grading may be applied if an "unbalance" is discovered.**
  - Both team members need to be present at design approval
  - Oral test might be given to both team members

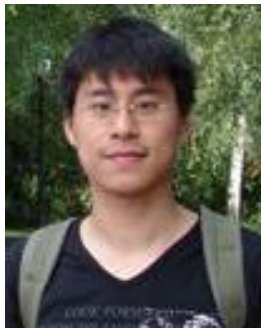
Next Step

What can we do after finishing this course?

Digital Path



Digital Path



Chenxin Zhang

Intro. VLSI (mouse control)

DSP Design IC Project Comp. Arc. (MIPS processor)

Master Thesis (multi-core MIPS)

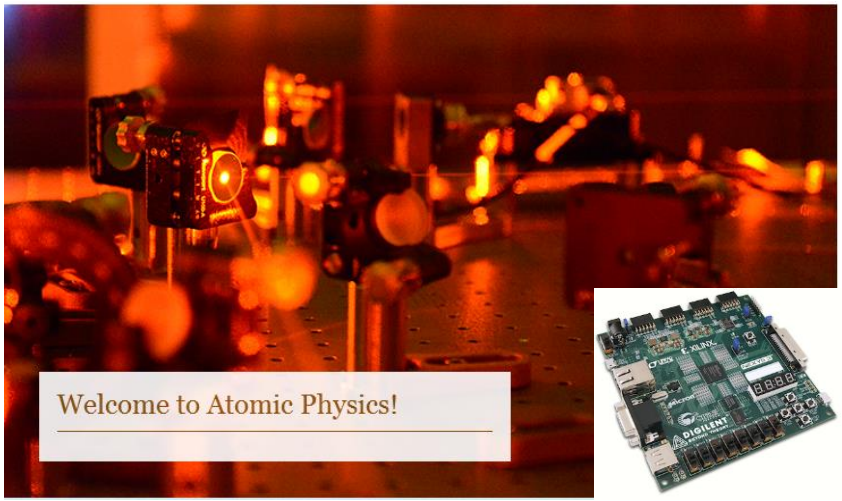
PHD (Processor for LTE-A.)

MediaTek (Processor for LTE-A.)

Projects and Thesis

Ultra-fast laser measurement

- **Cooperate with Anne L'Huillier (committee member, Nobel Physics Prize) in Atomic Physics**

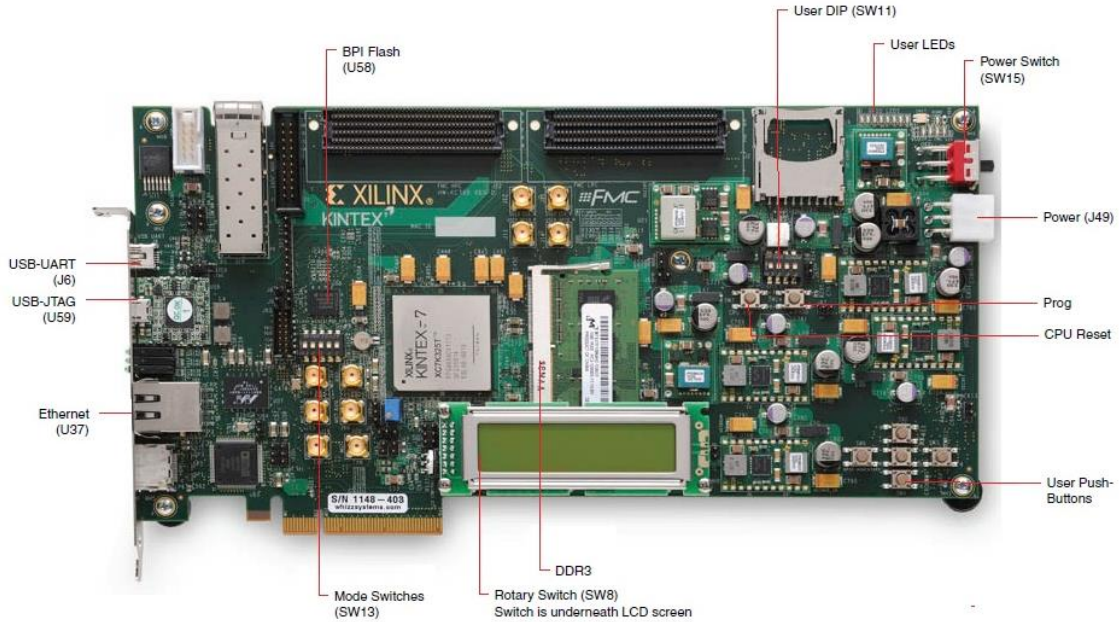


Projects and Thesis

- **Verification of LTE modems**
  - **Ericsson Lund**
- **Real-Time Lossless Compression of SOC Trace Data**
  - **Ericsson Stockholm**
- **Higher-level synthesis**
  - **ARM Lund**

Researches at EIT

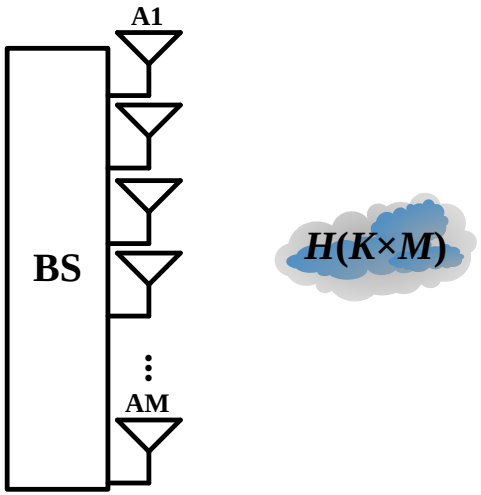
Baseband processing for LTE-A and beyond

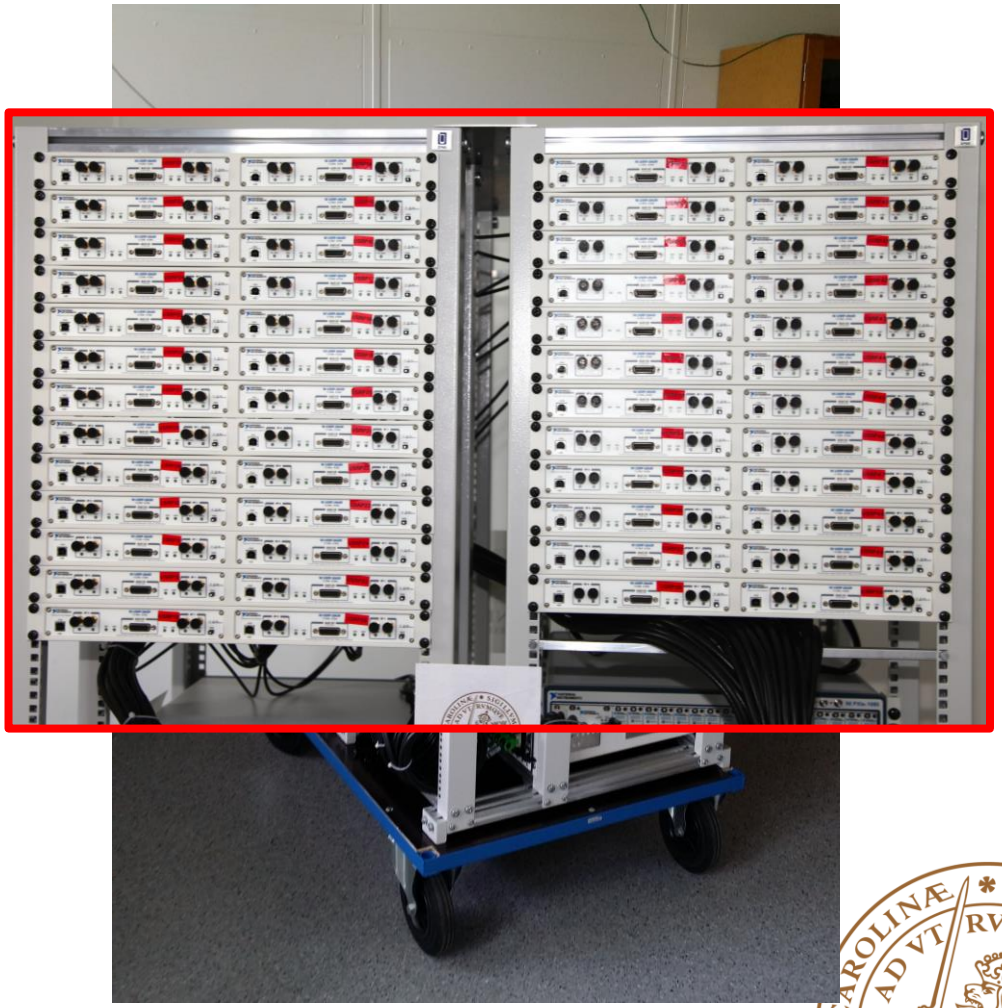


	XC7A100T	XC7K410T
Logic Cells	101,440	406,720
BlockRAM (Kb)	4,860	28,620
DSP Slices	240	1,540
PCIe® Gen2 Blocks	1	1
I/O Pins	300	500

Researches at EIT

- **World-first** Massive MIMO test-bed for 5G





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Questions?