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Introduction to structured VLSI design: Design for Test

ERIK LARSSON

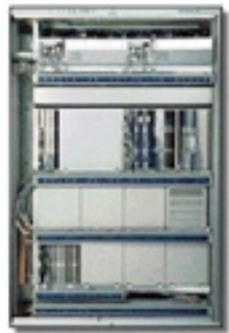
Outline

- Electronics
- Test generation
  - Creation of tests
- Design-for-test
  - Design modifications to ease test

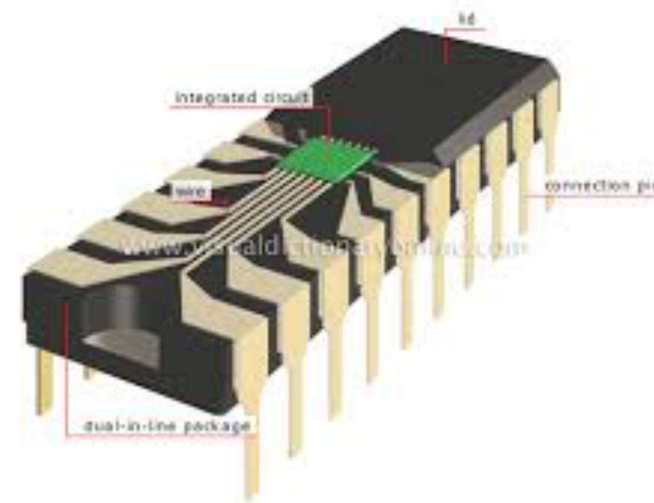
Motivation

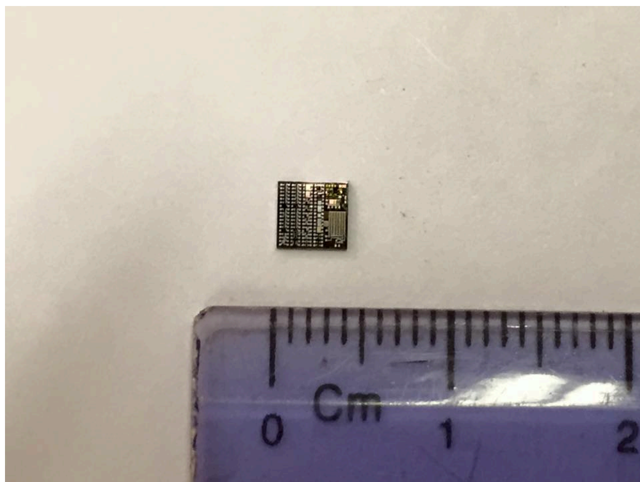
The young generation **The old generation**

Computers everywhere….

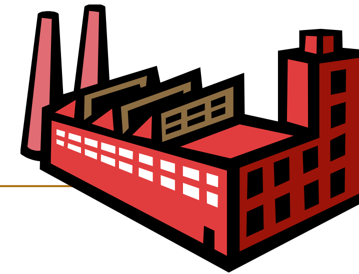


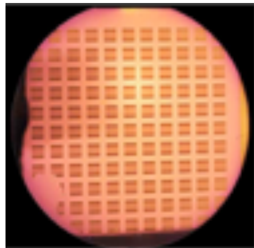
And inside there is electronics

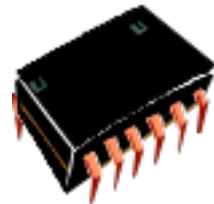


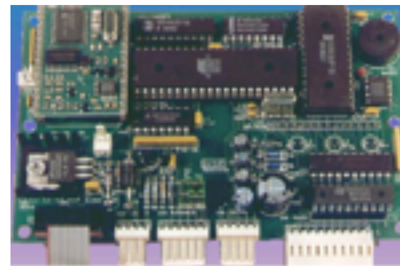


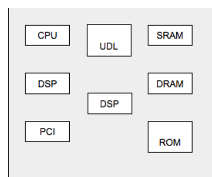
Electronics

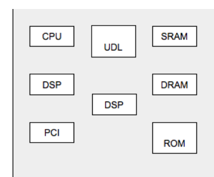


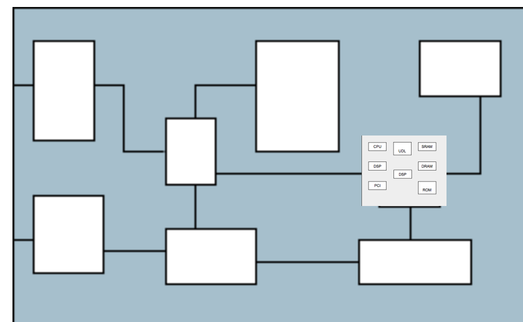


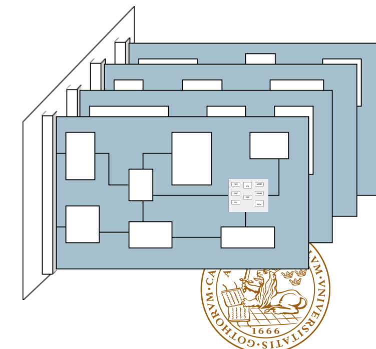












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Number of transistors

Transistor count

Date of introduction

curve shows transistor count doubling every two years

1 billion transistors on a die sized 1 cm x 1 cm

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Definitions

- Design synthesis: Given an I/O function, develop a procedure to manufacture a device using known materials and processes.
- Verification: Predictive analysis to ensure that the synthesized design, when manufactured, will perform the given I/O function.
- Test: A manufacturing step that ensures that the physical device, manufactured from the synthesized design, has no manufacturing defect.

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Verification vs. test

- Verifies correctness of design.
- Performed by simulation, hardware emulation, or formal methods.
- Performed once prior to manufacturing.
- Responsible for quality of design.

- Verifies correctness of manufactured hardware.
- Two-part process:
  - Test generation: software process executed once during design
  - Test application: electrical tests applied to hardware
- Test application performed on every manufactured device.
- Responsible for quality of devices.

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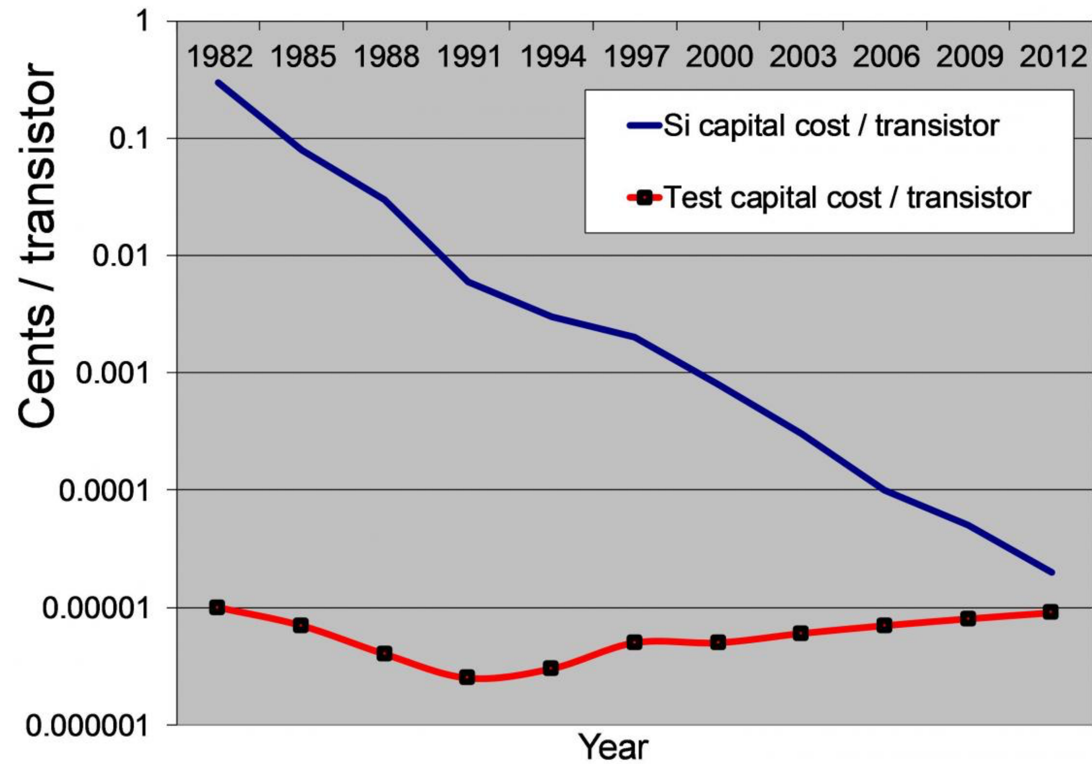
Cost per transistor



Beth Martin, Addressing Moore's Law with the First Law of Real Estate: Location, location, location, 08-02-2015, SemiWiki.com

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IC manufacturing

Silicon ingot

Slicer

Blank wafers

20 to 40 processing steps

Patterned wafers

Wafer tester

Tested wafer

Dicer

Tested dies

Bond die to package

Packaged dies

Part tester

Tested packaged dies

Ship to customers

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IC manufacturing

optical mask

oxidation

photoresist coating

stepper exposure

photoresist removal (ashing)

Typical operations in a single photolithographic cycle (from [Fullman]).

photoresist development

acid etch

spin, rinse, dry

process step

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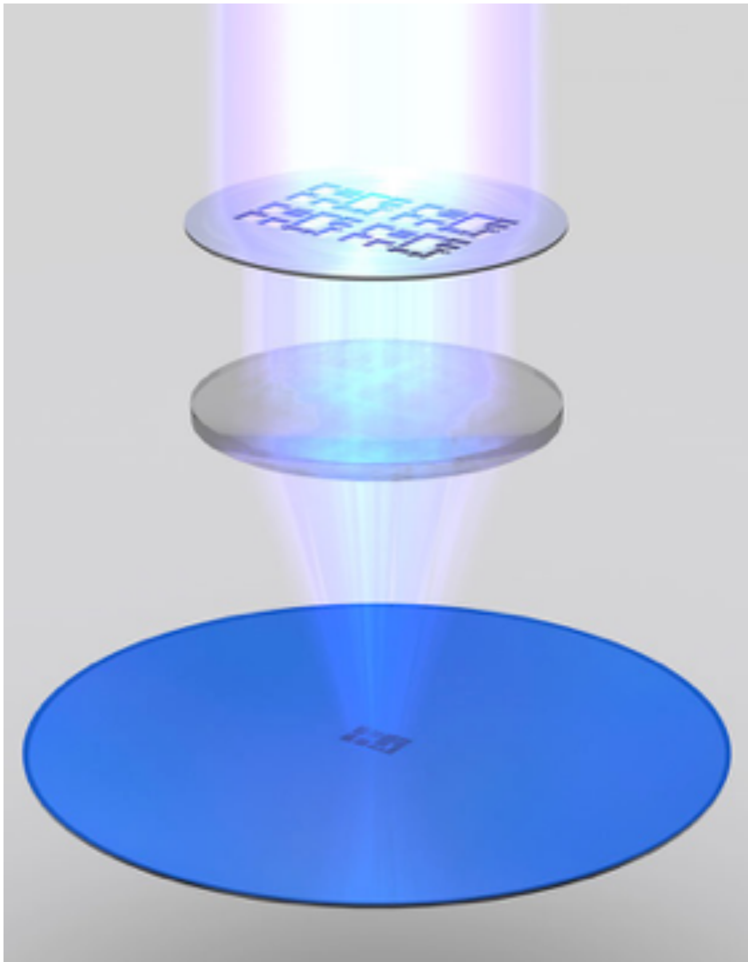
IC manufacturing



- The cost to set up a modern 45 nm process is $200–500 million
- The purchase price of a photomask can range from $1,000 to $100,000 for a single mask.
- As many as 30 masks (of varying price) may be required to form a complete mask set.

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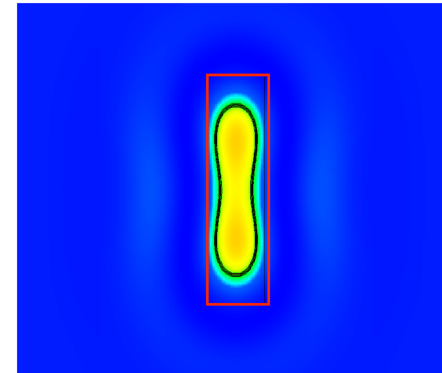
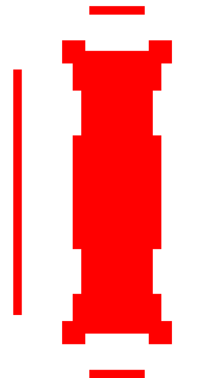
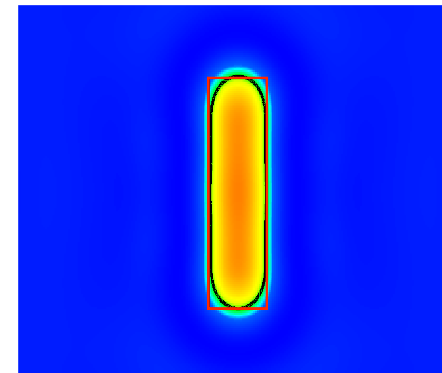
IC manufacturing

- Straight forward:

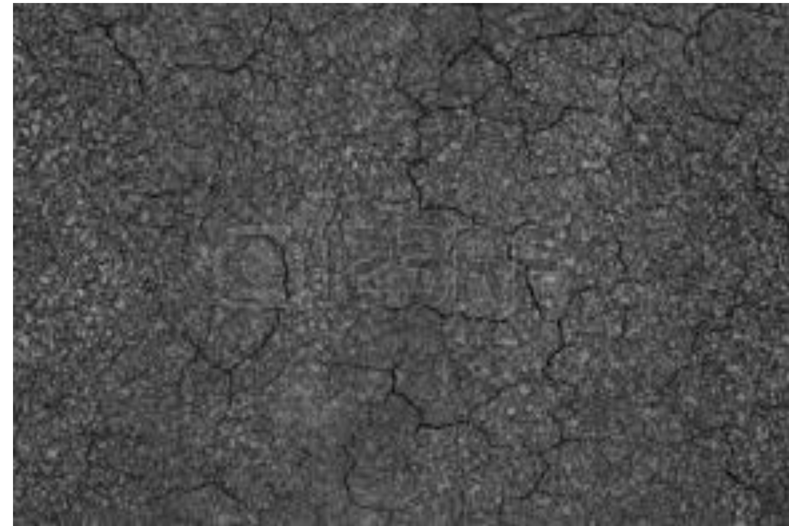


- Corrective modifications:



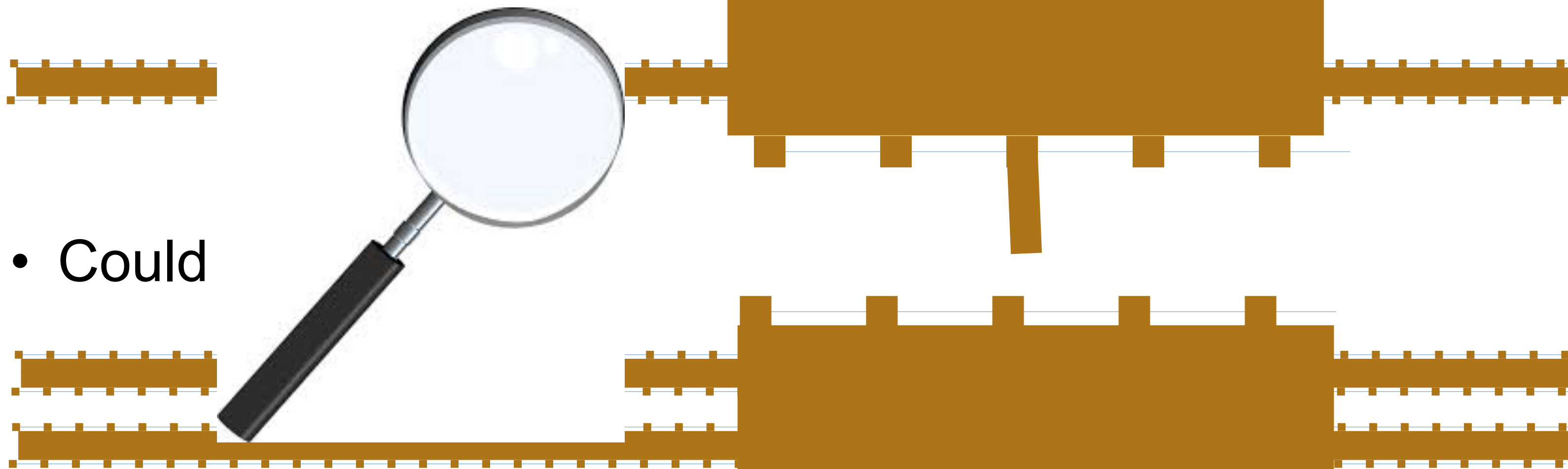


How flat is a road?

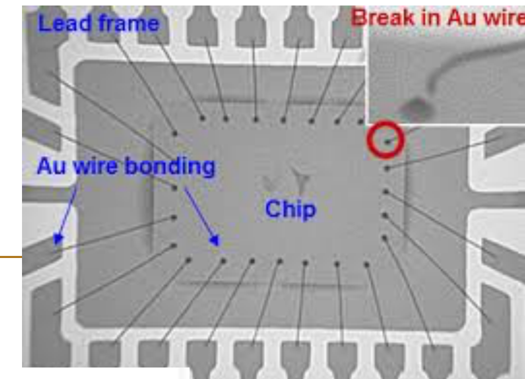


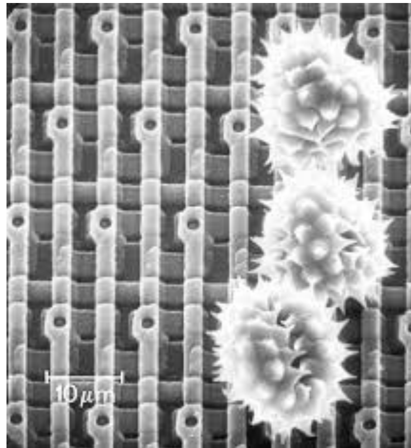
How straight is a line in an IC?

- At a distance
- Closer look
- Could



Examples of defects





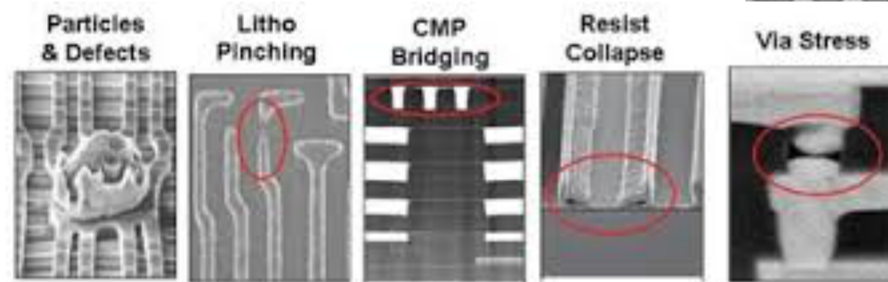
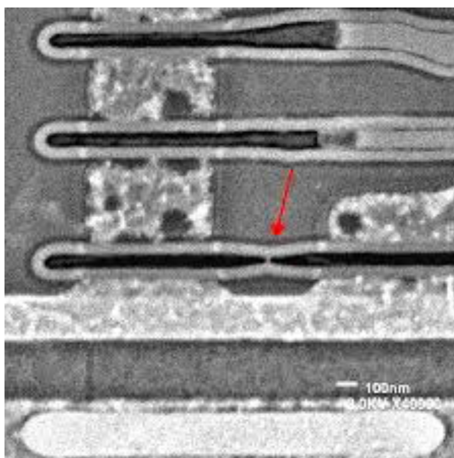


Figure 3 Both feature-related and particle defects cause a chip to fail.



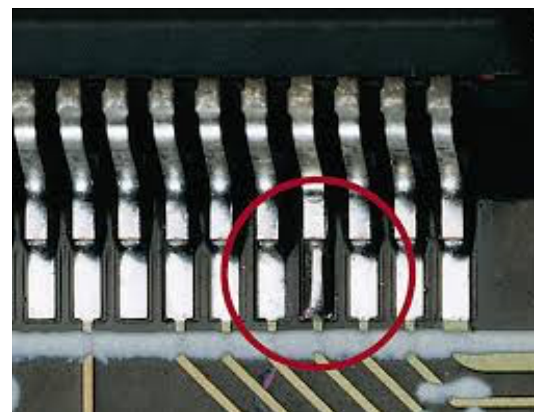
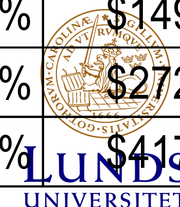


Fig. 1. With "tombstoning" only one side of a two-leaded chip component may be soldered to the target pad, but its other termination may not come in contact with the associated target pad. Photo courtesy of IPC-610

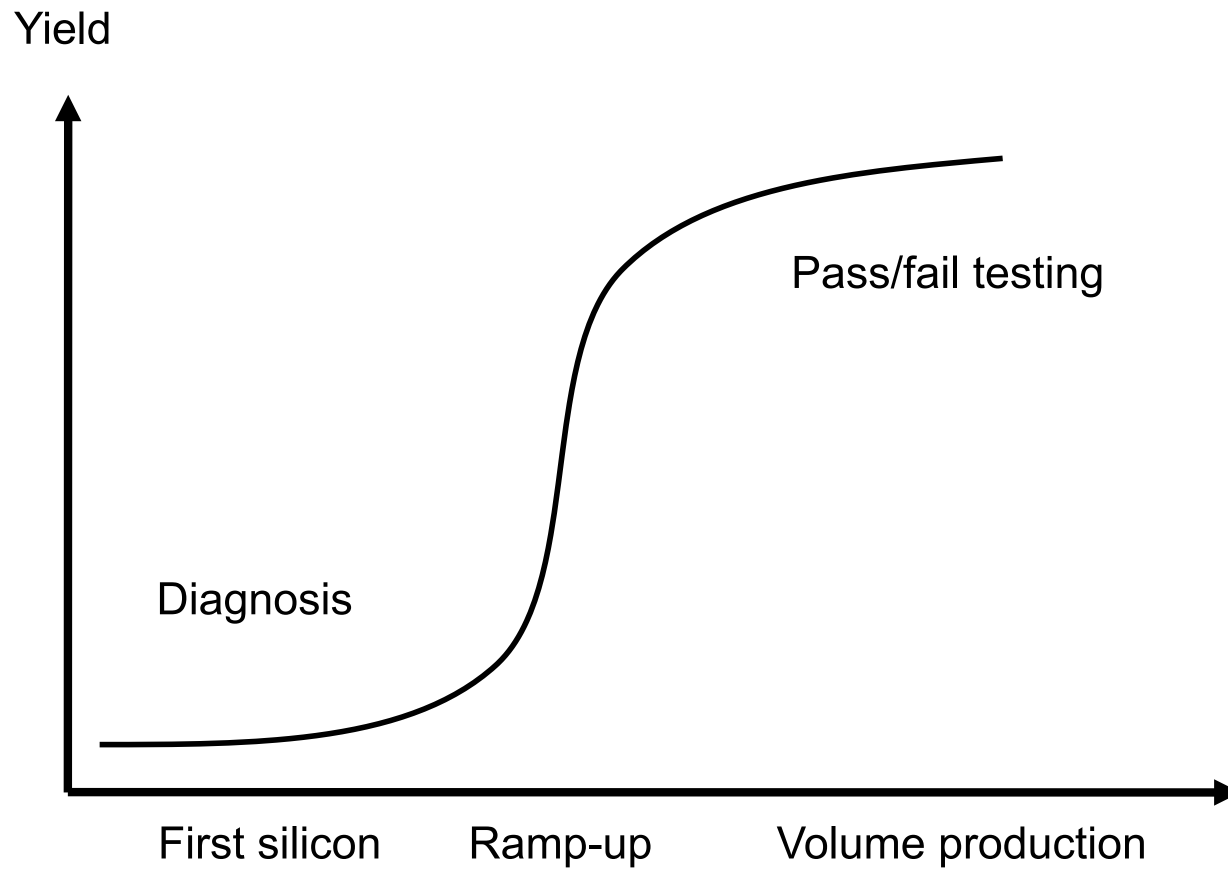
Yield

- Yield is good devices over produced devices
- Perfect manufacturing results in 100% yield
  - No need of test!

Chip	Layers	Wafer cost	Defect/cm^2	Area (mm^2)	Dies/Wafer	Yield	Die Cost
386DX	2	$900	1.0	43	360	71%	$4
486DX2	3	$1200	1.0	81	181	54%	$12
PowerPC 601	4	$1700	1.3	121	115	28%	$53
HP PA 7100	3	$1300	1.0	196	66	27%	$73
DEC Alpha	3	$1500	1.2	234	53	19%	$149
SuperSPARC	3	$1700	1.6	256	48	13%	$272
Pentium	3	$1500	1.5	296	40	9%	$417

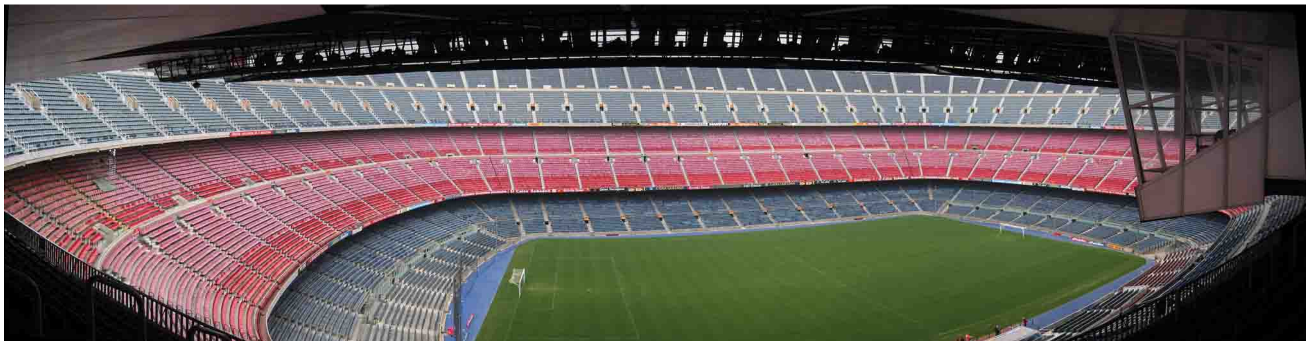


Yield over time



Challenge: test vs. diagnosis

- Each seat in a football stadium is a chip to be sold
- The test challenge is to tell if there is a bug on any of the seats
- The diagnosis challenge is for a given seat to tell where the bug is



Chip

Outcome of test

- Good IC that pass the test -> OK //this chip is sold
- Bad IC that fail the test -> OK //this chip is not sold
- Bad IC that pass the test -> test escape (lose costumer confidence) //a bad chip is sold
- Good IC that pass the test – yield loss //a good chip is thrown away (lose money)

		Outcome of test	
		Pass	Fail
Status of IC	Good	OK	Yield loss
	Bad	Test escape	OK

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Test escape and yield

- Assume 2 million ICs manufactured with yield 50%
  - 1 million GOOD shipped
  - 1 million BAD shipped
- Target DPPM (Defective parts per million) = 100
- For 100 BAD parts in 1 million shipped (DPPM=100)
  - Test must detect 999900 out of all the 1000000 BAD
    - » Test coverage: 99.99% (999900/1000000)

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DPPM and yield

- Consider 1 Million parts. Assume test coverage: 99.99% (100 escapes per million defective)
- DPPM @ 50% yield = 100
- DPPM @ 10% yield
  - » 0.1 million GOOD -> shipped
  - » 0.9 million BAD -> 90 test escapes (900000*(100%-99.99%))

  DPPM = 90/0.1=900
- DPPM @90% yield
  - » 0.9 million GOOD -> shipped
  - » 0.1 million BAD -> 10 test escapes (100000*(100%-99.99%))

  DPPM=10/0.9=11

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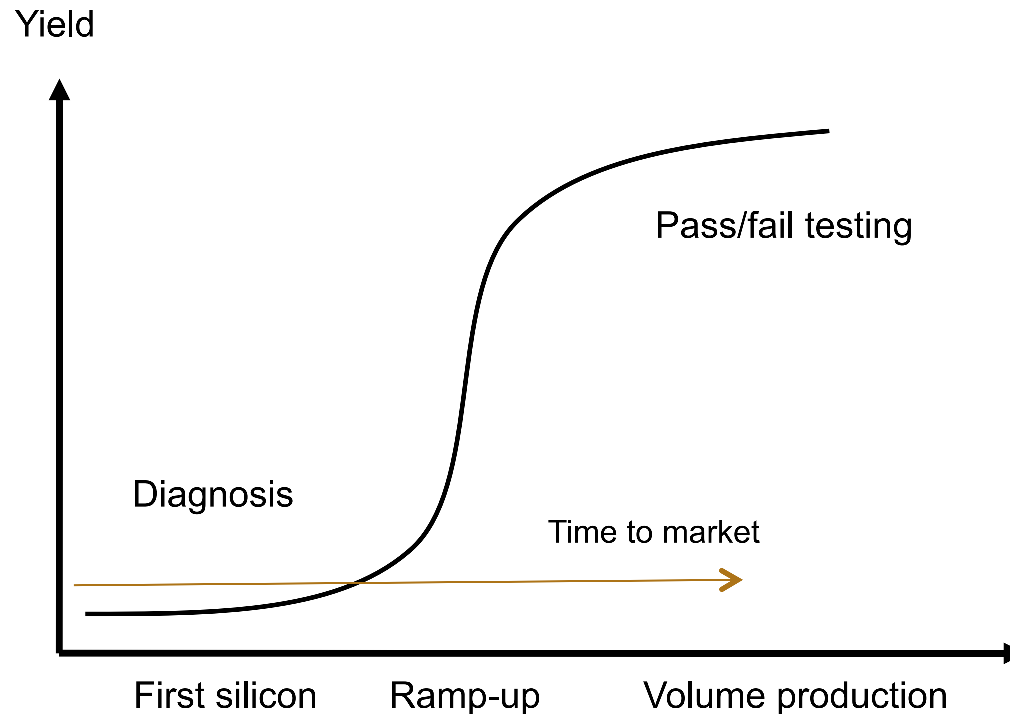
Cost of test

- Diagnosis: enough information to pinpoint root cause of defects
- Pass/fail: enough information to determine if a device is good or bad



Outline

- Electronics
- Test generation
  - Creation of tests
- Design-for-test
  - Design modifications to ease test

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Testing basics

- Functional Tests: Exercise the circuit in “mission mode”
  - Expensive to develop
    - » no effectiveness measure
  - Today mostly used to evaluate speed
- Structural Tests: Target “modeled” faults
  - Scan stuck-at tests: low cost, effective DC tests
  - Transition Delay Faults (TDF) tests now widely used

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Perfect test vs. real test

- Perfect test:
  - Detects all defects
  - Pass all functionally good devices
- Real test:
  - Based on analyzable fault models
  - Some good chips are rejected (yield loss)
  - Some bad chips pass test (test escape)

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Objective of test generation

- Specify the test vector
- Determine correct response (expected response)
- Evaluate cost of test (# patterns related to cost)
- Evaluate quality of test

- Fault coverage = No of faults detected / No. faults modeled

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Defects, faults and fault models

- Example: assume a break system in a car
- A <u>defect</u> is if there is weak joint in the brake fluid pipe (could be due to manufacturing mistake)
- A <u>fault</u> is if the weak joint break (but still you could drive the car and there is no problem unless you break)
- A <u>failure</u> is when you there is a fault in the braking system and you break.

Defects, faults and fault models

- Real defects too numerous and often not analyzable
- A fault model
  - identifies targets for testing
  - makes analysis possible
- A defect manifests itself as a fault
- A fault is modeled by a fault model
- Example of fault models:
  - Stuck-at Fault, Bridging Fault, Shorts (Resistive shorts), Opens, Delay Faults, Transient Fault

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Fault classes

- Faults/defects detected by single vector tests
  - Stuck-at, bridging faults, many open defects
  - High ATPG coverage (stuck-at, bridging, N-detect tests)
- Faults/defects requiring two-pattern tests
  - Timing defects, some opens defects
  - 1-3% of all failing parts need two-pattern tests
  - Moderate test coverage

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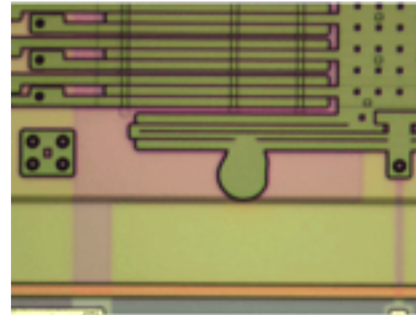
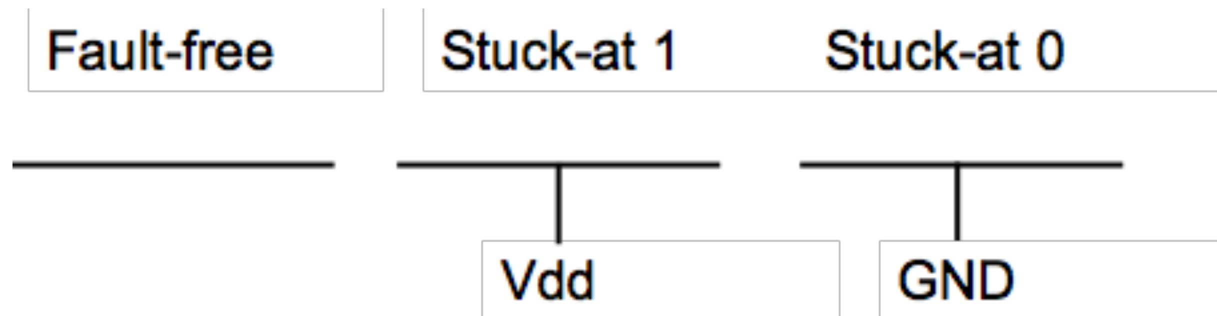
Defects, faults and fault models

- Example of a defect:



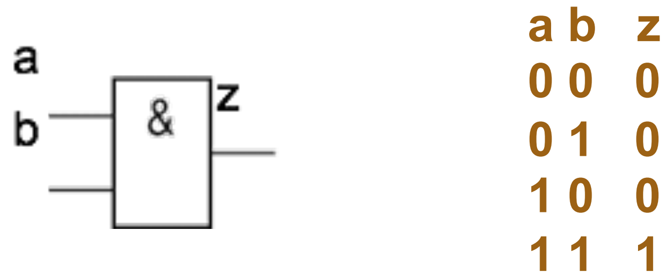
- Example of a fault model:



- A defect manifests itself as a fault
- A fault is modeled with a fault model

Exhaustive tests

- Try all possible alternatives
- For a 2-input design, 2^2 (4) vectors are needed:



- For a 30-input design, 2^{30} (1073741824) vectors are needed
- If we apply 1 vector per second, it will take 34 years to test the circuit (2^{30}/(60*60*24*365)=34)

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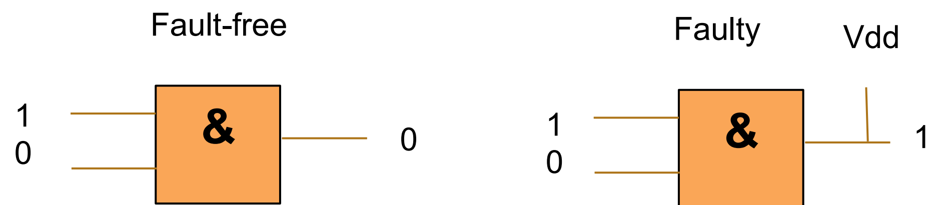
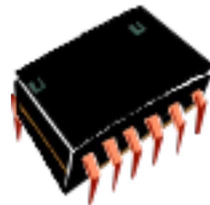
Test generation

- Example: create a test for the output connected to Vdd
- Requirement: response from fault-free case must be different from faulty case



- At manufacturing:

Apply stimuli:
1
0



Produced response:
1

- Test pattern: test vector + expected test response
- Produced test response is compared against expected test response

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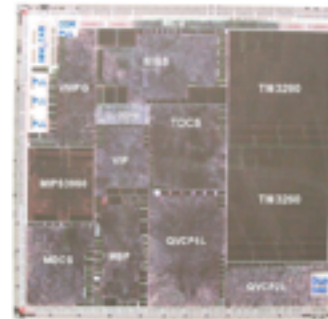
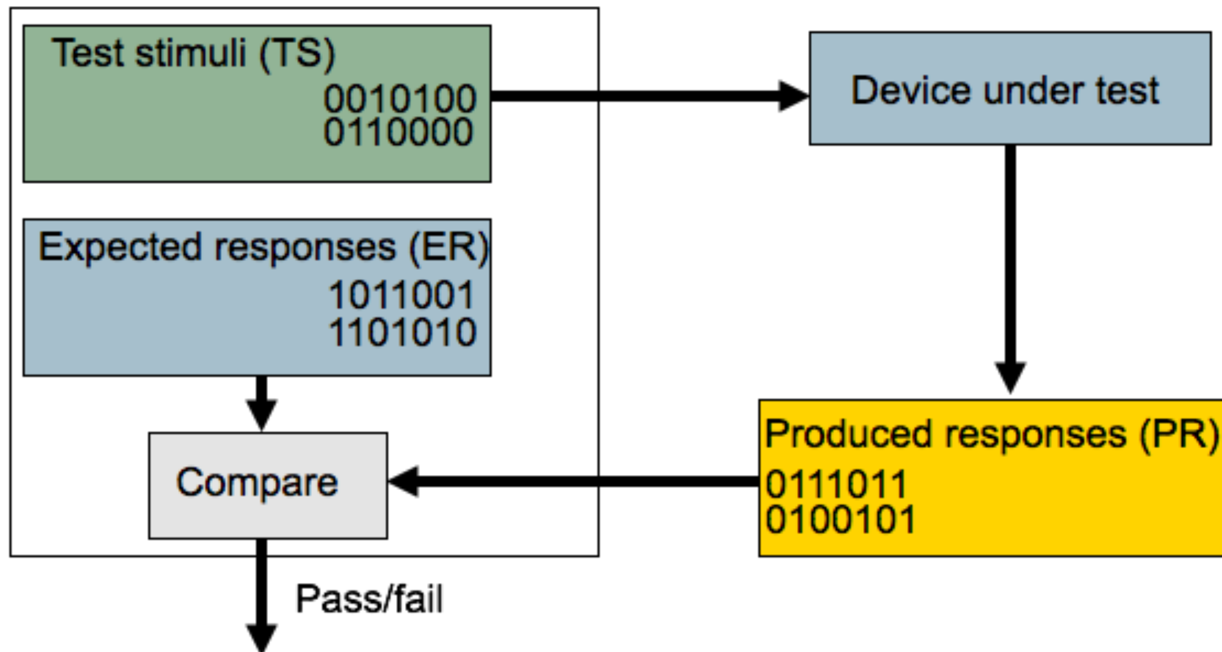
Test application





General scheme for test generation

```
While fault coverage < desired limit {
        Select an uncovered fault f
        Generate test for the fault f
        Evaluate fault coverage
}
```

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Single stuck-at fault

- A basic ATPG (automatic test-pattern generation) algorithm
  - activate one fault at a time
  - work backward from the fault origin to the PIs (primary inputs)
  - work forward from the fault origin to a PO (primary output)
  - work backward from the PO to the Pis to generate the sensitized path.

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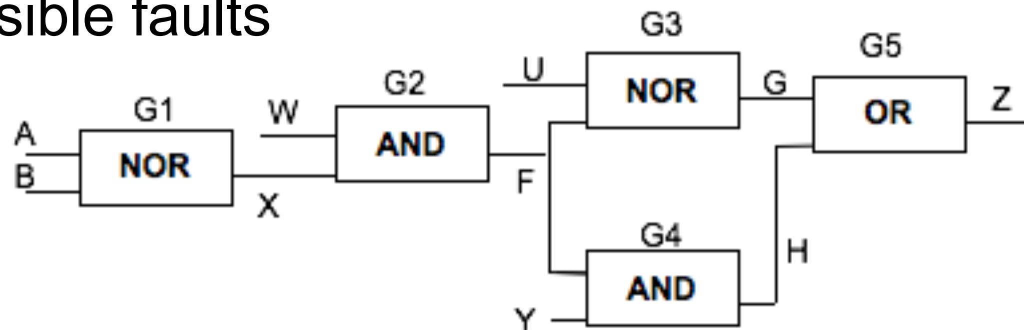
Single stuck-at fault

- One line at the time is fixed to logic value 0 (stuck-at-0) or 1 (stuck-at-1)
- For the stuck-at fault model there are for a circuit with n lines 2*n possible faults

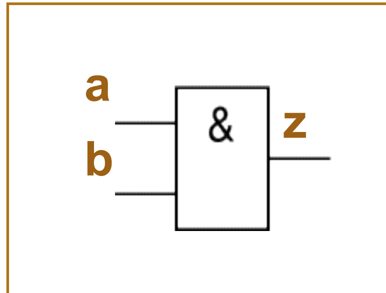


- Quality of a test is given by:

  fault coverage = faults detected / total number of faults

- Example: 12 lines (24 faults) detect 15 faults:
  f.c.=15/24 (63%)

Fault collapsing



- Value fault free/faulty (v/vf)
- Stuck-at 0 on a: a=1/0, b=1 -> z=1/0 //vector (stimulus) 11
- Stuck-at 0 on b: b=1/0, a=1 -> z=1/0 //vector (stimulus) 11
- Stuck-at 0 on z: b=1, a=1 -> z=1/0 //vector (stimulus) 11
- Stuck-at 1 on a: a=0/1, b=1 -> z=0/1 //vector (stimulus) 01
- Stuck-at 1 on b: a=0/1, b=1 -> z=0/1 //vector (stimulus) 10
- Stuck-at 1 on z: a=0, b=x -> z=0/1 //vector (stimulus) 0x or x0

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Equivalence rules

sa0 sa1
sa0 sa1
sa0 sa1
sa0 sa1
sa0 sa1
sa0 sa1
sa0 sa1
sa0 sa1
sa0 sa1
sa0
sa1
sa0 sa1
sa0 sa1
sa0 sa1
sa0 sa1
sa0 sa1

Faults in red removed by equivalence collapsing

Fault simulation

- Given
  - A circuit
  - A sequence of test vectors
  - A fault model
- Determine
  - Fault coverage - fraction (or percentage) of modeled faults detected by test vectors
  - Set of undetected faults
- Motivation
  - Determine test quality and in turn product quality
  - Find undetected fault targets to improve tests

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Test compaction

- ATPG generates too many vectors; faults are covered by several vectors
- Static test set compaction tries to remove vectors after the use of ATPG
- Dynamic test tries to remove vectors during ATPG

	f_1	f_2	f_3	f_4	f_5	f_6	f_7
v_1	x		x		x		
v_2						x	x
v_3	x				x		x
v_4		x	x	x	x		

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Commercial ATPG tools

- Commercial ATPG tools are
  - for combinational circuits
  - make use of a random test generation for 60-80% of the faults (easy to detect) and deterministic test generation for the remaining part (hard to detect)
- Examples of commercial ATPG tools:
  - Encounter Test - Cadence
  - TetraMax - Synopsis
  - FastScan, FlexTest - Mentor Graphics

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Outline

- Electronics
- Test generation
  - Creation of tests
- Design-for-test
  - Design modifications to ease test
    - » Test points
    - » Scan
    - » Built-In Self-Test
    - » IEEE 1149.1 (Boundary scan (JTAG))

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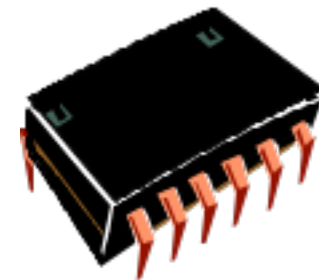
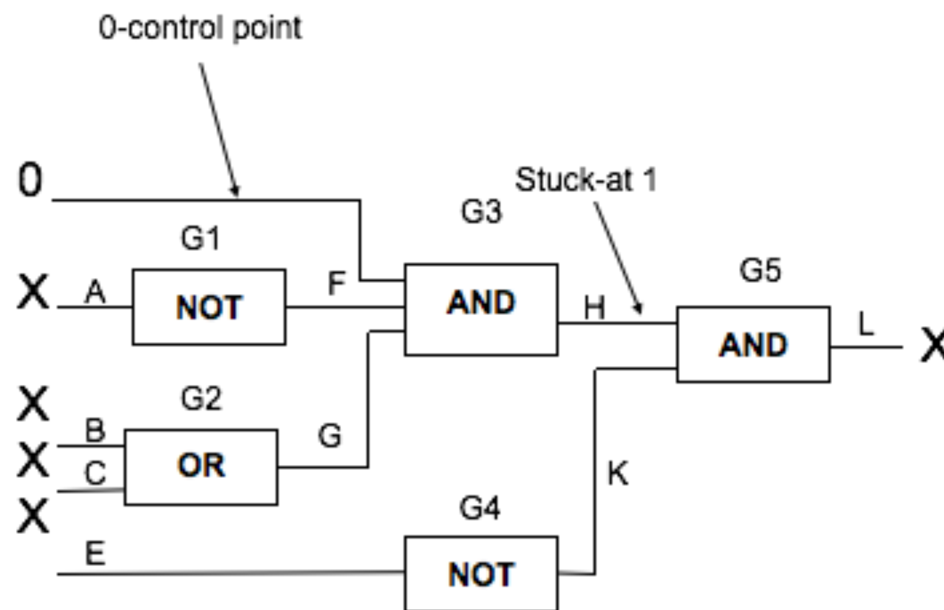
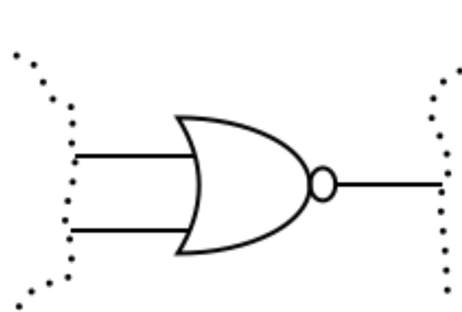
Test point insertion

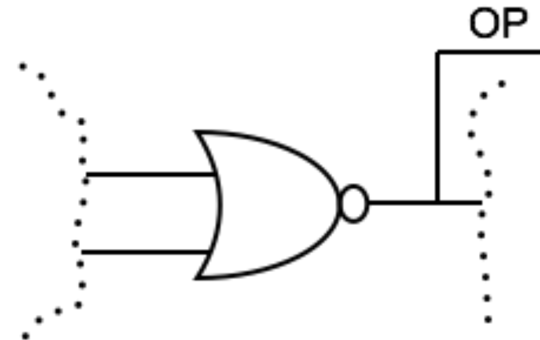
- Add a test point to ease test generation
- Access to chip internal is only through pins

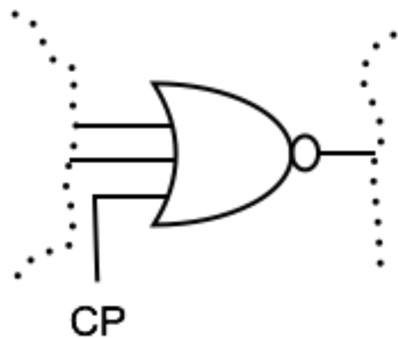


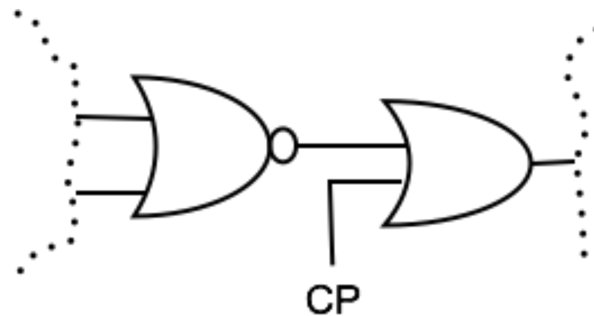


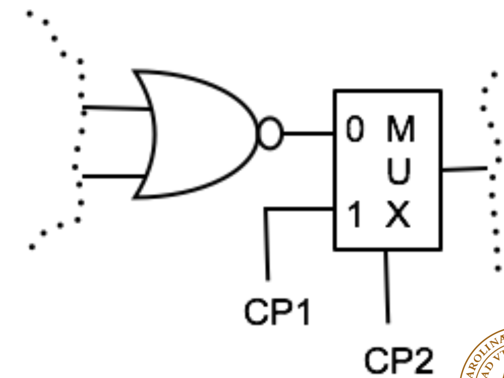
Test point insertion











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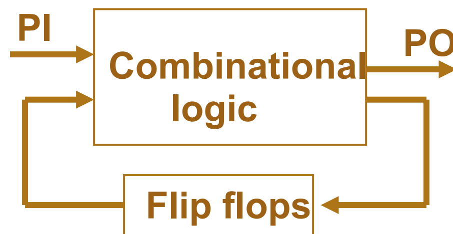
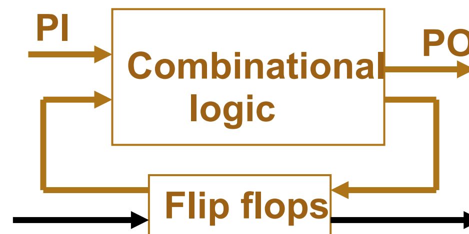
Scan

- Problem: ATPG works for combinational logic while most ICs are sequential
- Solution: Provide a test mode in which flip flops can be accessed directly
- Registers (FFs) provide virtual primary inputs/primary outputs

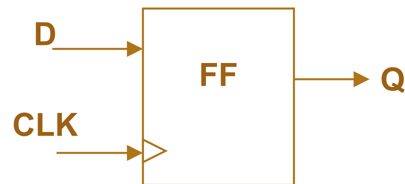


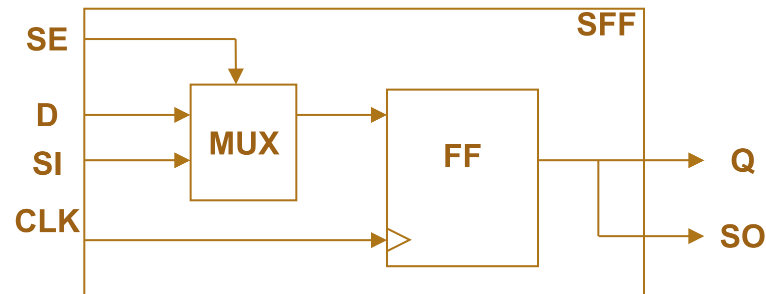


1. **Write flip flops**
2. **Stimulus at inputs**
3. **Normal cycle launch/capture**
4. **Observe output**
5. **Read flip flops**

Scan

- Replace flip flop (FF) with scan flip flop (SFF): extra multiplexer on data input
- Connect SFFs to form one or more scan chains
- Connect multiplexer control signal to scan enable





SE: Scan enable
SI: Scan input
SO: Scan output

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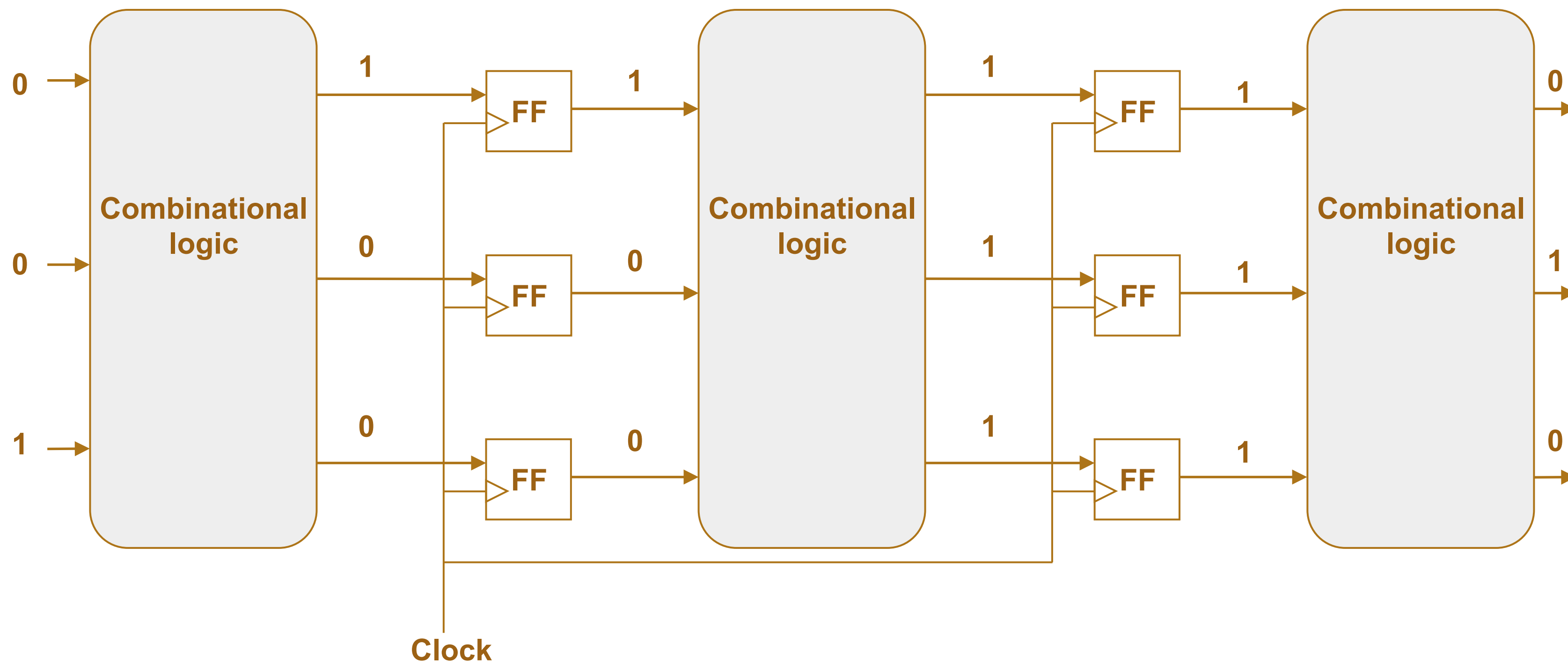
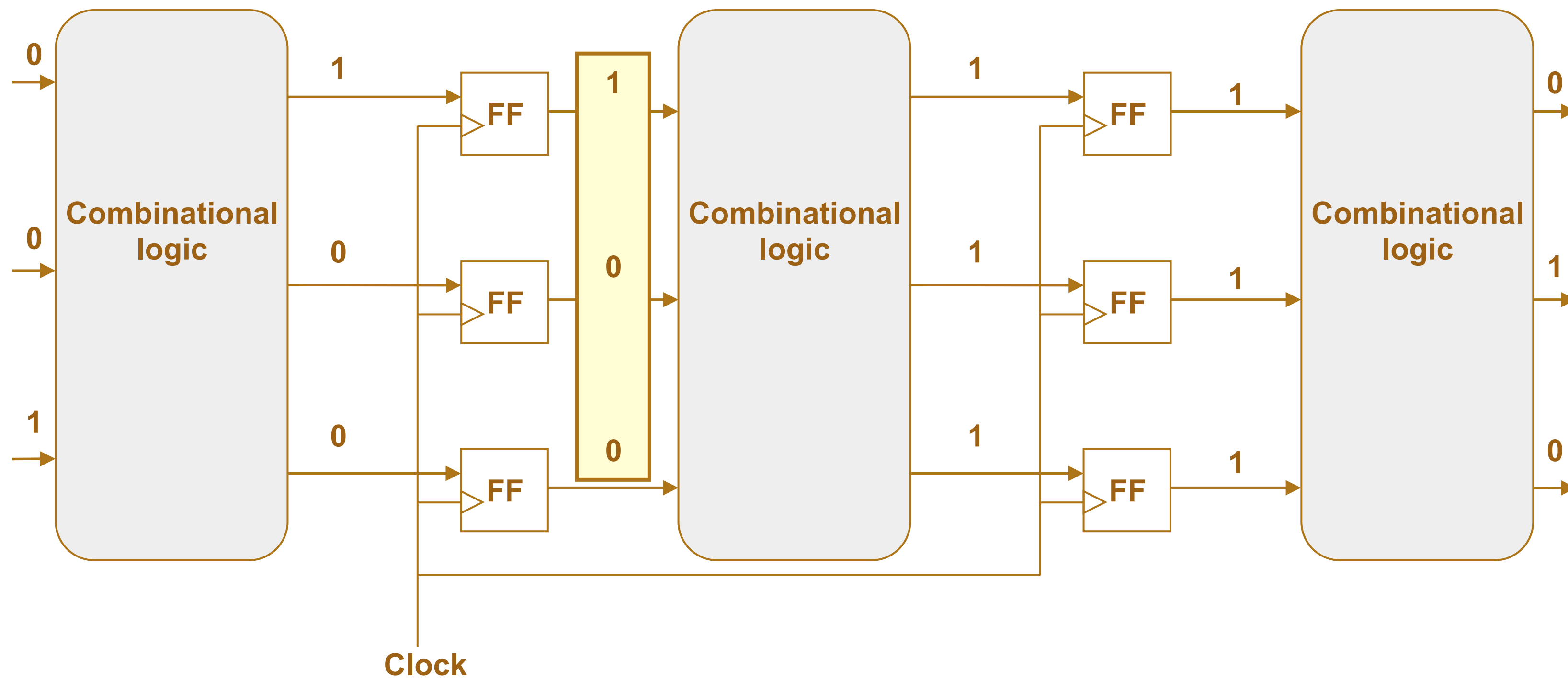
Scan



Scan



Scan

Scan enable

Combinational logic

MUX

MUX

MUX

FF

FF

FF

Combinational logic

MUX

MUX

MUX

FF

FF

FF

Combinational logic

Scan Input

Clock

Scan Output

Scan

Scan enable

Combinational logic

MUX

MUX

MUX

FF

FF

FF

1 0 0

1 0 0

MUX

MUX

MUX

1 1 1

FF

FF

FF

Combinational logic

1

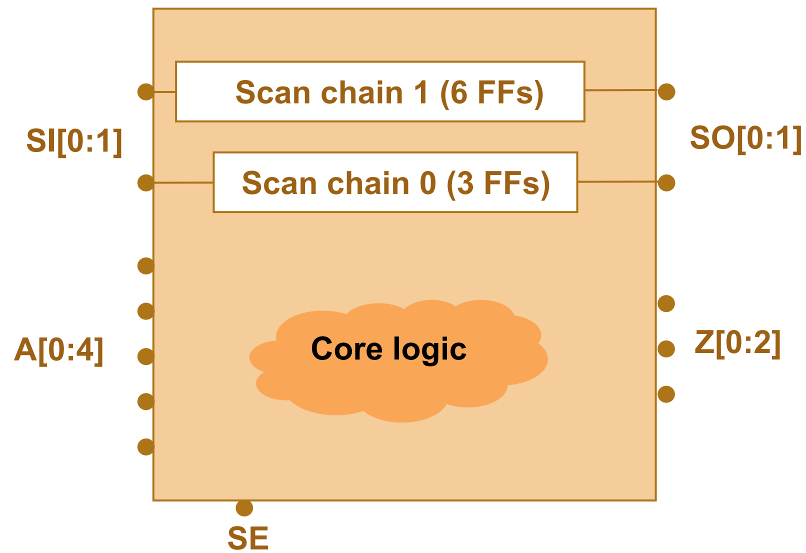
Scan Input

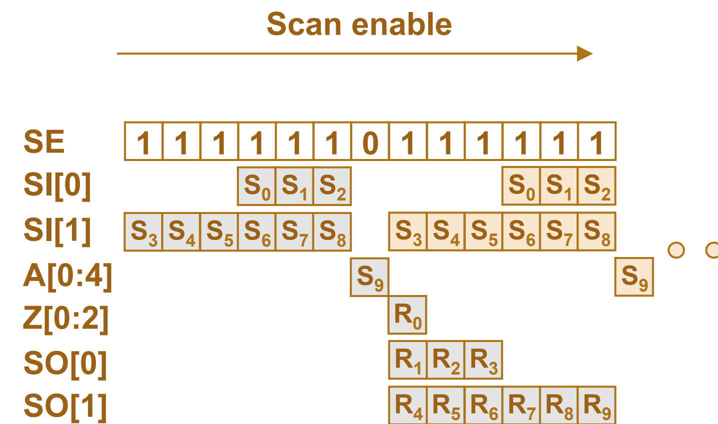
Clock

Scan Output

LUNDS UNIVERSITET

Scan application





Scan

- Scan Benefits
  - Automatic scan insertion
  - ATPG
  - High fault coverage
  - Short test development time
- EDA tools
  - For scan insertion
  - Partial scan selection
  - Scan stiching
- Scan Costs
  - Silicon area
    - » Mux, scan chain, scan enable
  - Performance reduction
    - » Multiplexer in time-critical path
  - IC pins
    - » Scan-in (SI), scan-out (SO), scan_enable (SE)
  - Test time
    - » Serial shifting is slow

Outline

- Electronics
- Test generation
  - Creation of tests
- Design-for-test
  - Design modifications to ease test
    - » Test points
    - » Scan
    - » Built-In Self-Test
    - » IEEE 1149.1 (Boundary scan (JTAG))

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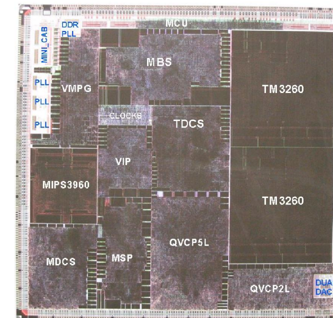
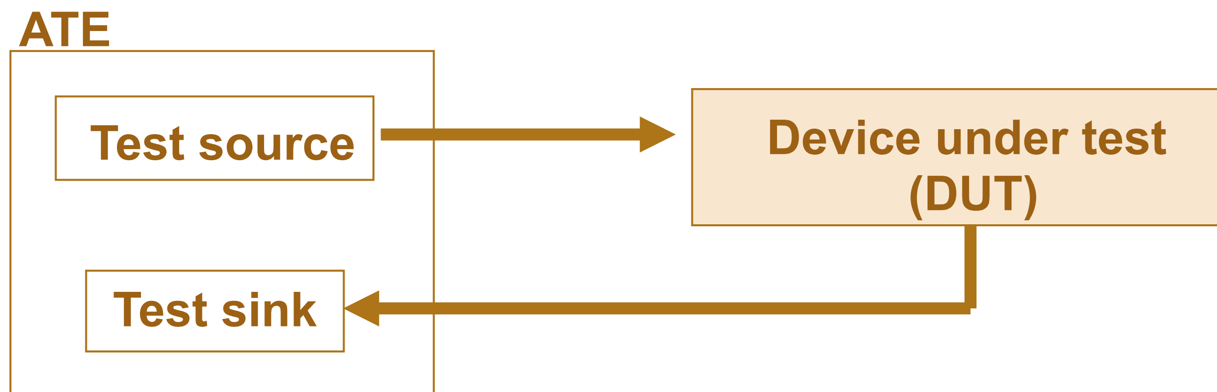
Built-In Self-Test

- Test source – where test stimuli are generated/stored
- Test sink – where test responses are stored/analyzed





Built-In Self-Test

Off-chip

Test source → Device under test (DUT)

Test sink ← Device under test (DUT)

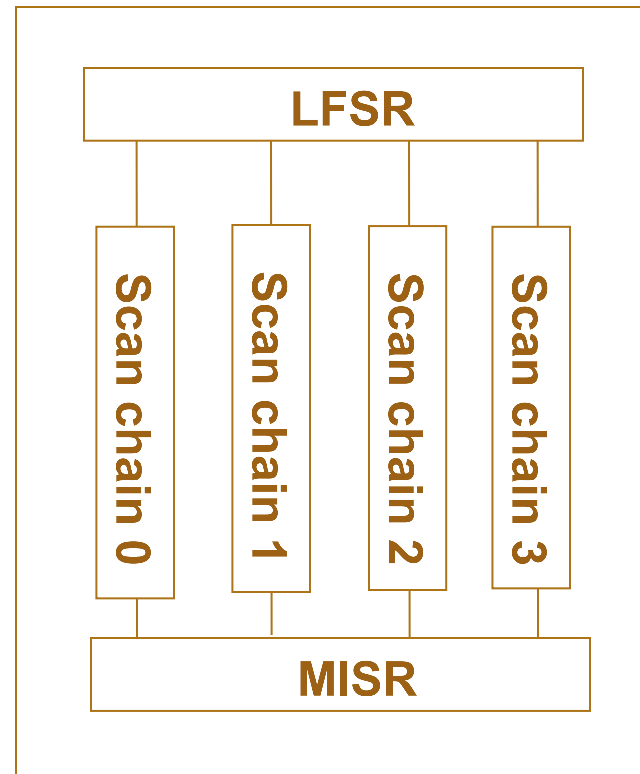
On-chip

Test source → Device under test (DUT)

Test sink ← Device under test (DUT)

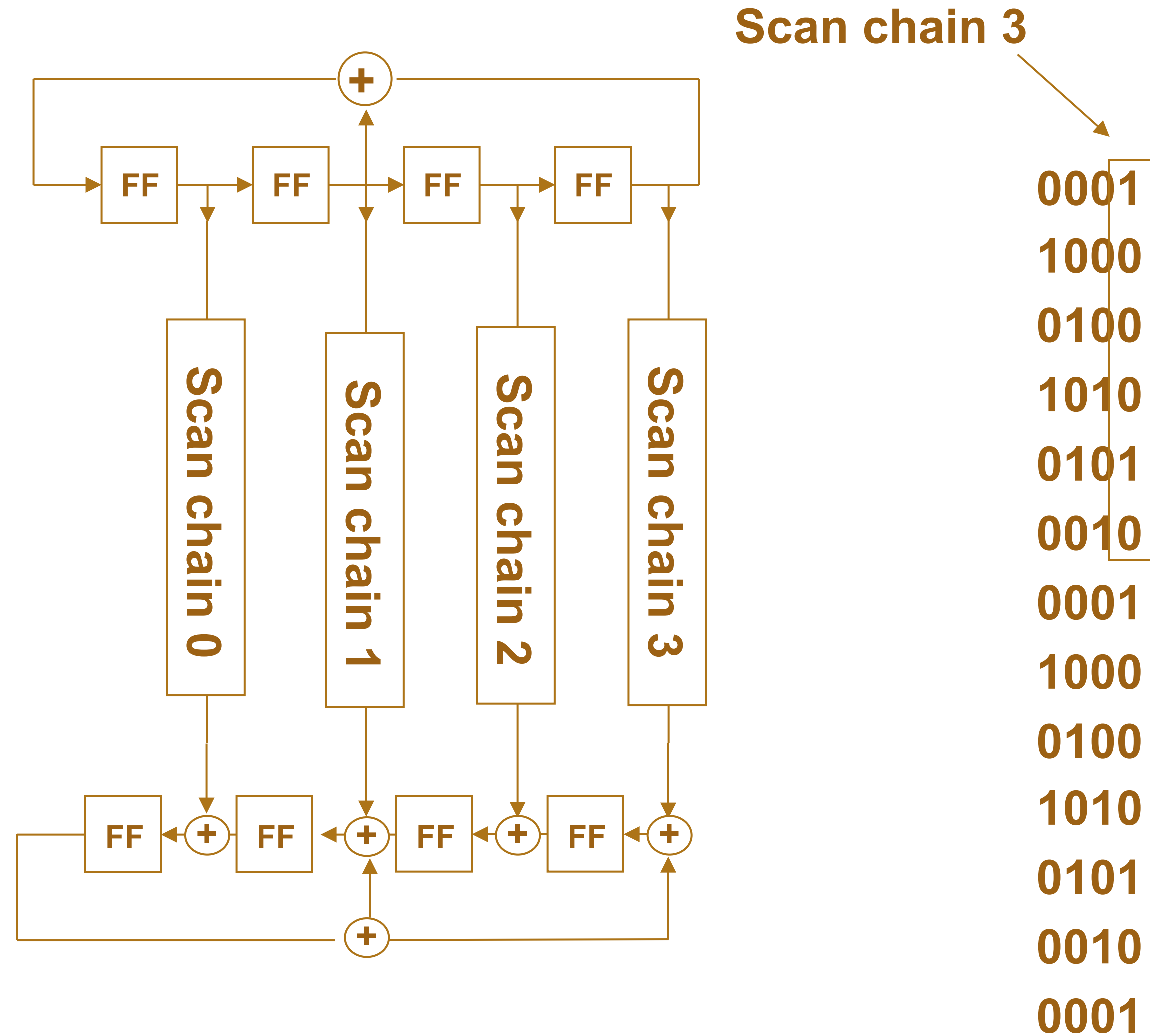
LUNDS UNIVERSITET

STUMPS: Self-testing using MISR and parallel shift register sequence generator



Test source: Linear Feedback Shift Register (LFSR)
Test sink: Multiple Input Signature Register (MISR)

STUMPS: Self-testing using MISR and parallel shift register sequence generator



Random pattern resistant faults

- The effectivness of a test is given based on the test's fault coverage, length, and hardware/data storage requirement.
- Probabilty to create a 1 at the output; $1/2^n$ where n is the number of inputs. n=2; P=0.25, n=4; P=0.0625

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Built-In Self-Test

- Difficult to reach high test coverage
- Diagnostic resolution is low
  - Only a MISR signature

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Outline

- Electronics
- Test generation
  - Creation of tests
- Design-for-test
  - Design modifications to ease test
    - » Test points
    - » Scan
    - » Built-In Self-Test
    - » IEEE 1149.1 (Boundary scan (JTAG))

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Objective

- Given a Printed Circuit Board (PCB) composed of a set of components (ICs) where each component is tested good.
- The main objectives are to ensure that all components are:
  - correct (the desired ICs are selected)
  - mounted correctly at the right place on the board and
  - ensuring that interconnections are functioning according to specification
- Problems that may occur:
  - A component is not placed where it should be,
  - A component is at its place but turned wrongly,
  - A component is correct but the interconnection is not correct, for example due to bad soldering.

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Boundary Scan (IEEE std. 1149.1)

- The Joint European Test Action Group (JETAG), formed in mid-80, became Joint Test Action Group (JTAG) in 1988 and formed the IEEE std. 1149.1.
- The IEEE std. 1149.1 consists of:
  - Test Access Port (TAP)
  - TAP Controller (TAPC),
  - Instruction Register (IR), and
  - Data Registers (DR)

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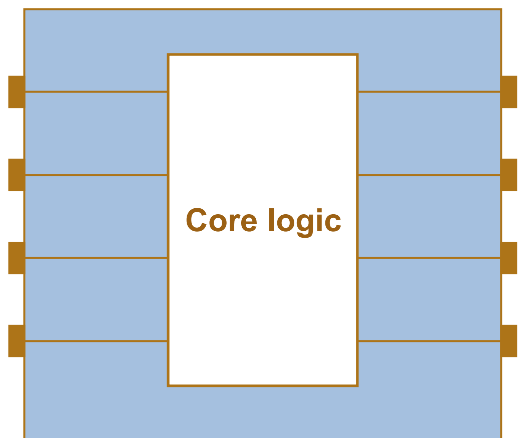
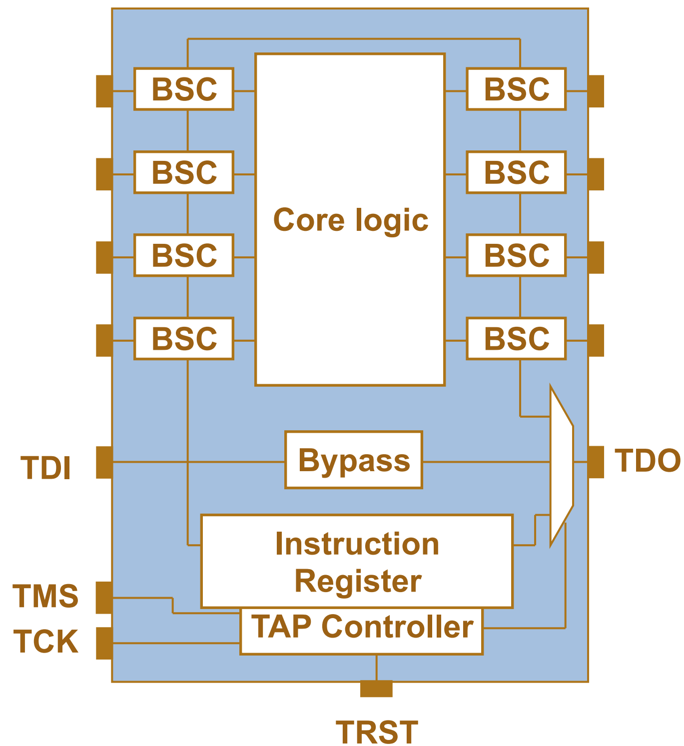
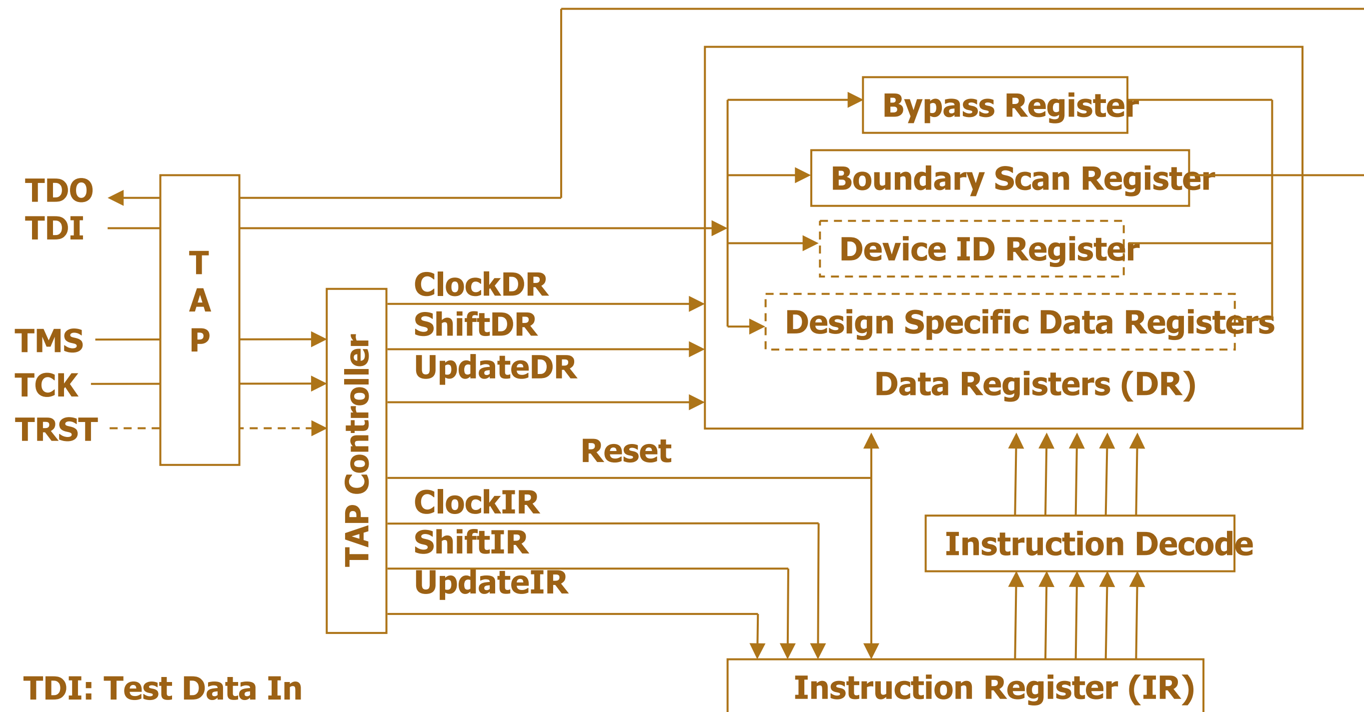
Boundary Scan (IEEE std. 1149.1)





Boundary Scan (IEEE std. 1149.1)



TDI: Test Data In
TDO: Test DataOut
TMS: Test Mode Select
TCK: Test Clock

Optional registers and signals are shown in dotted lines

Boundary Scan (IEEE std. 1149.1)

TMS

Control of data registers

Control of instruction register

Test-Logic-Reset

1 0

Run-Test/Idle

0

1

Select-DR-Scan

1

Select-DR-Scan

1

0

Capture-DR

1

0

Shift-DR

0

1

Exit1-DR

1

0

Pause-DR

1

0

Exit2-DR

1

Update-DR

1 0

0

Capture-DR

1

0

Shift-DR

0

1

Exit1-DR

1

0

Pause-DR

1

0

Exit2-DR

1

Update-DR

1 0

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Boundary Scan (IEEE std. 1149.1)

- Mandatory
  - Bypass; used to bypassing an IC
  - Extest; tests interconnection between ICs
  - Sample/Preload; used to sample (snapshot) and preload boundary scan during operation
- Optional
  - Intest, Runbist, Clamp, Idcode, Usercode, Highz

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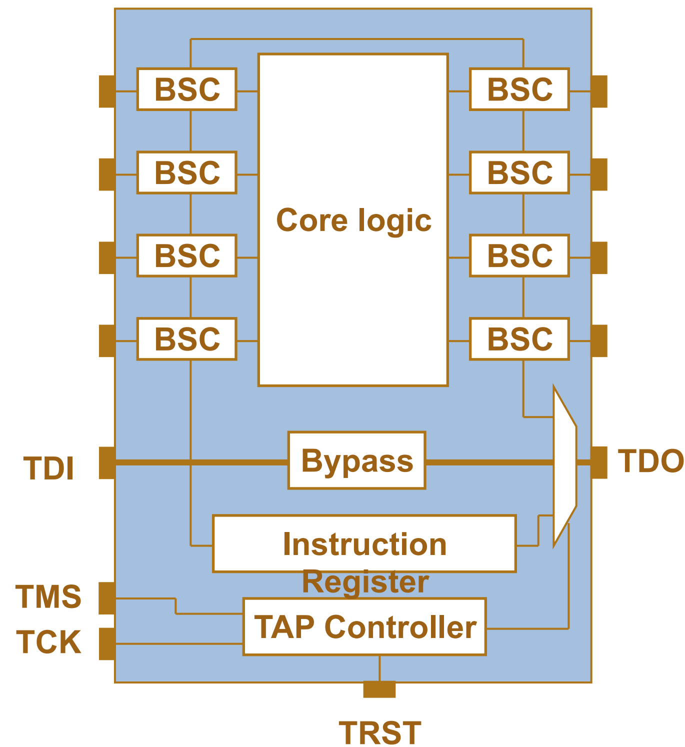
Boundary Scan (IEEE std. 1149.1)



Scan and MBIST support with Boundary Scan

Scan path
Scan_in
Scan_en
Logic
Scan_out
BIST controller
Memory
Compressor
Bist_sel
BIST decoder
Mbist
Bist_so
Scan decoder
Int_scan
Decoder
Instruction register
TDI
TCK
TMS
TAP Controller
MUX
TDO

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