EITF35: Introduction to Structured VLSI Design

Introduction to FPGA design

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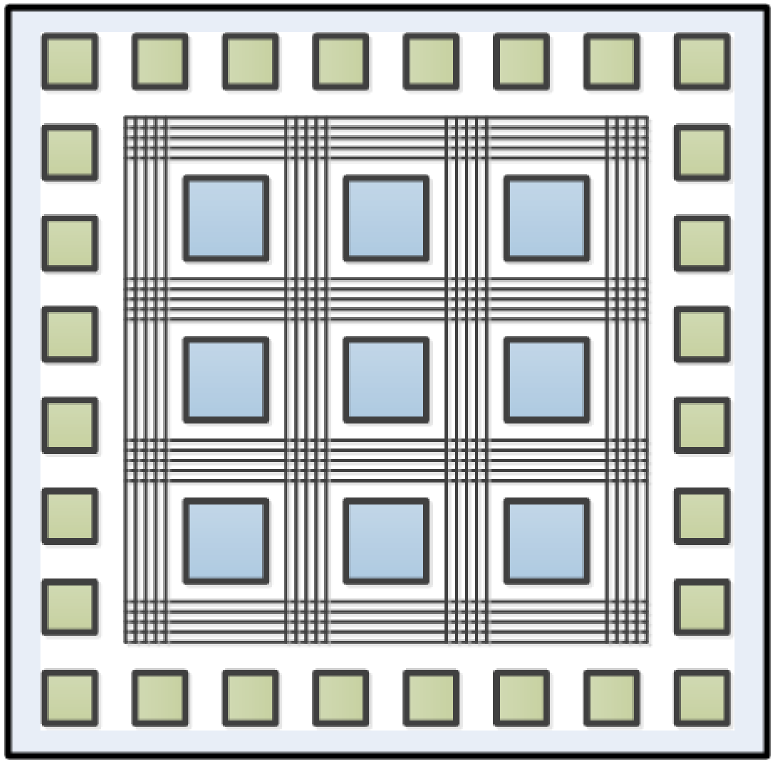
Slides from Chenxin Zhang

WWW.FPGA

- What is FPGA?
  - Field Programmable Gate Array

Configurable logic blocks

Configuration memory



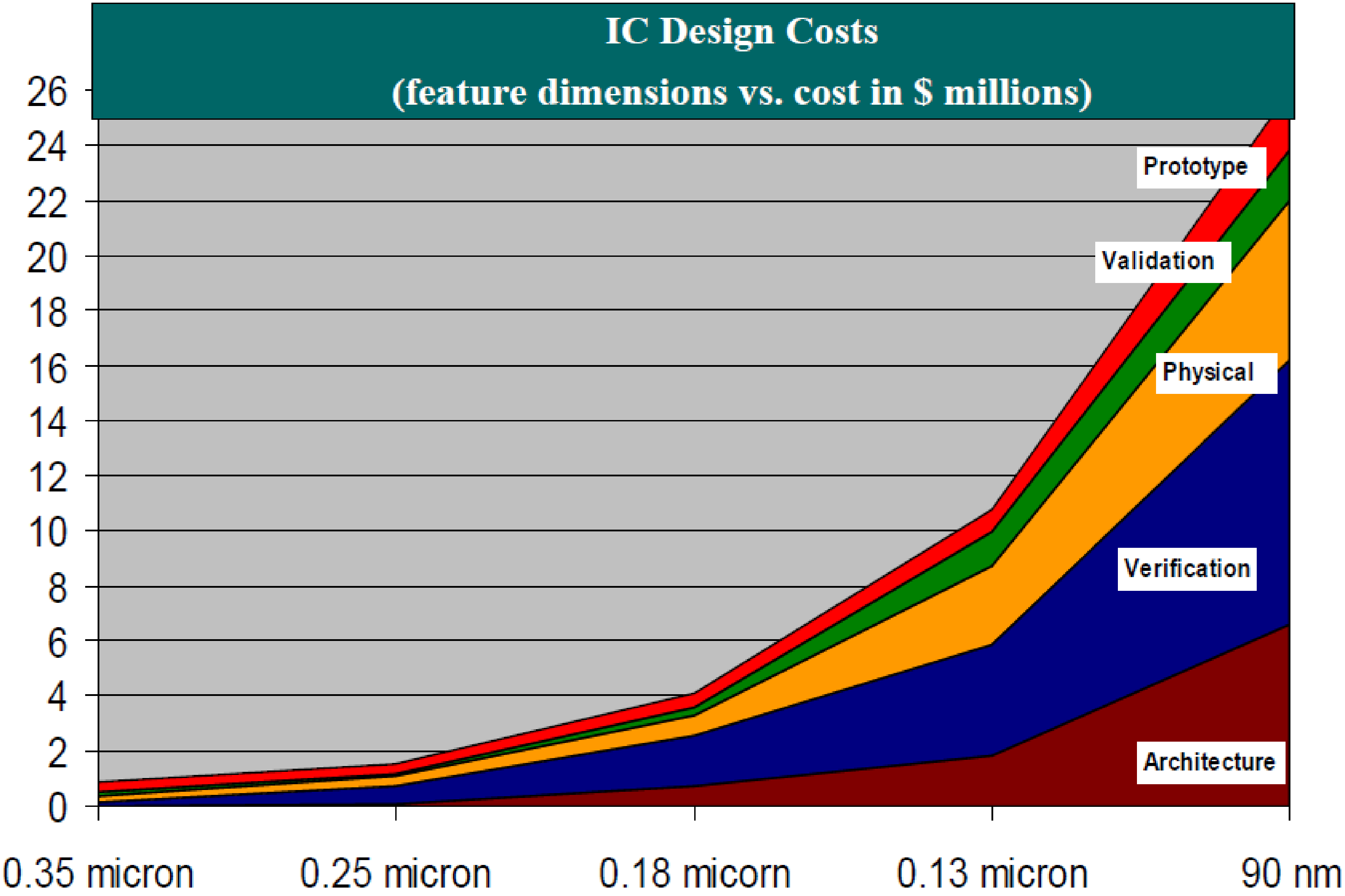
Interconnects

IO blocks

WWW.FPGA

- What is FPGA?
  - Field Programmable Gate Array
  - Configurable logic blocks + interconnects + IOs + memory
- Why do we use it?
  - High performance & Flexible
  - Shorter time to market

WWW.FPGA


IC Design Costs
(feature dimensions vs. cost in $ millions)
26
24
22
20
18
16
14
12
10
8
6
4
2
0
Prototype
Validation
Physical
Verification
Architecture
0.35 micron
0.25 micron
0.18 micorn
0.13 micron
90 nm

WWW.FPGA

- What is FPGA?
  - Field Programmable Gate Array
  - Configurable logic blocks + interconnects + IOs + memory
- Why do we use it?
  - High performance & Flexible
  - Shorter time to market
- Where do we use it?
  - Prototyping
  - Computer vision
  - Medical imaging
  - Software-defined radio
  - …

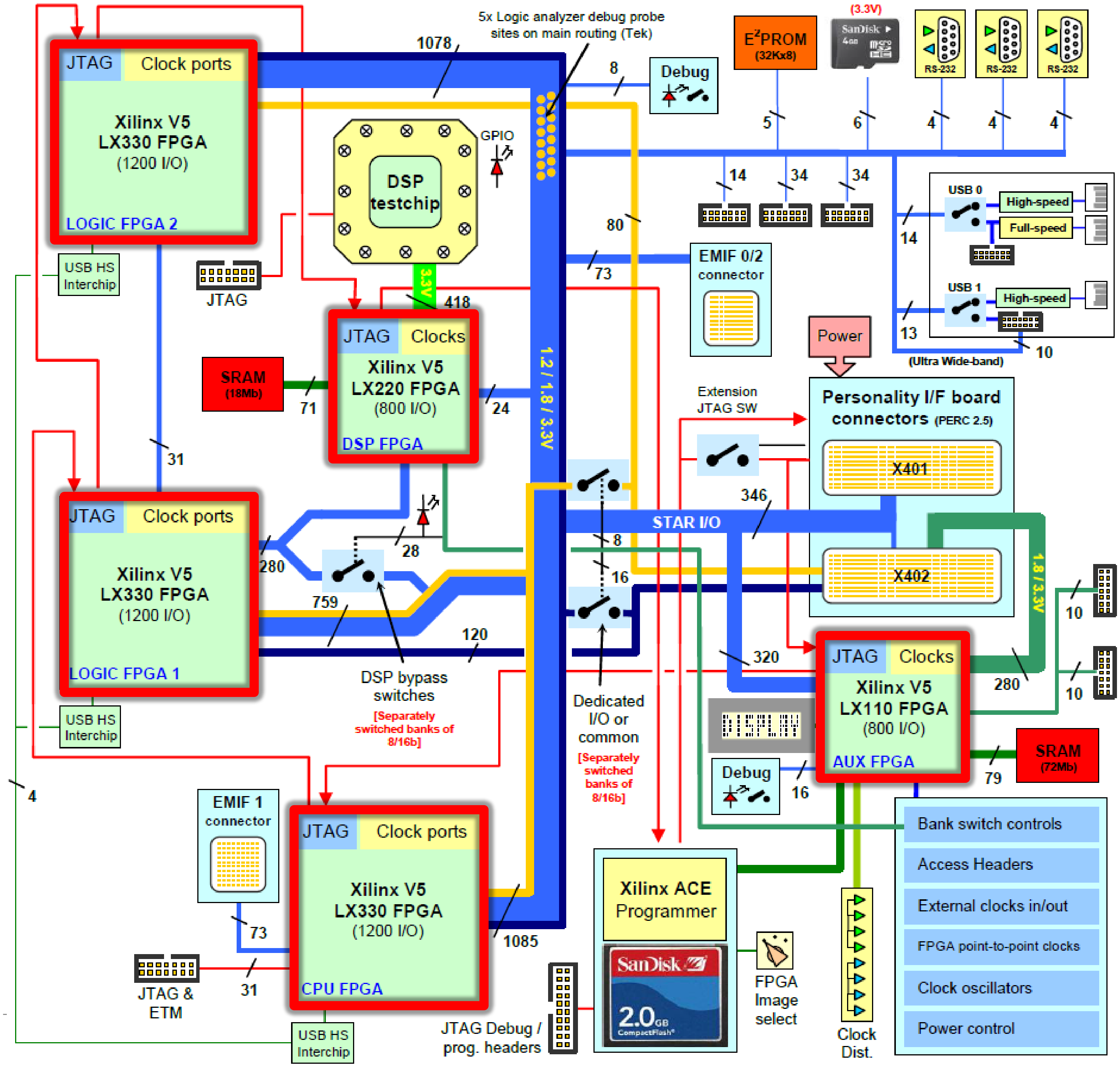
FPGA vs. Microprocessor

	Intel Itanium 2	Xilinx Virtex-II Pro (XC2VP100)
Technology	0.13 µm	0.13 µm
Clock speed	1.6 GHz	180 MHz
Internal memory bandwidth	102 GBytes/S	7.5 TBytes/S
# Processing units	5 FPU (2 MACs+1 FPU) 6 MMU 6 Integer units	212 FPU or 300+Integer units or …
Power consumption	130 W	15 W
Peak performance	8 GFLOPs	38 GFLOPs
Sustained performance	~2GFLOPs	~19 GFLOPs
IO/External memory bandwidth	6.4 GBytes/S	67 GBytes/S

(Courtesy: Nallatech)

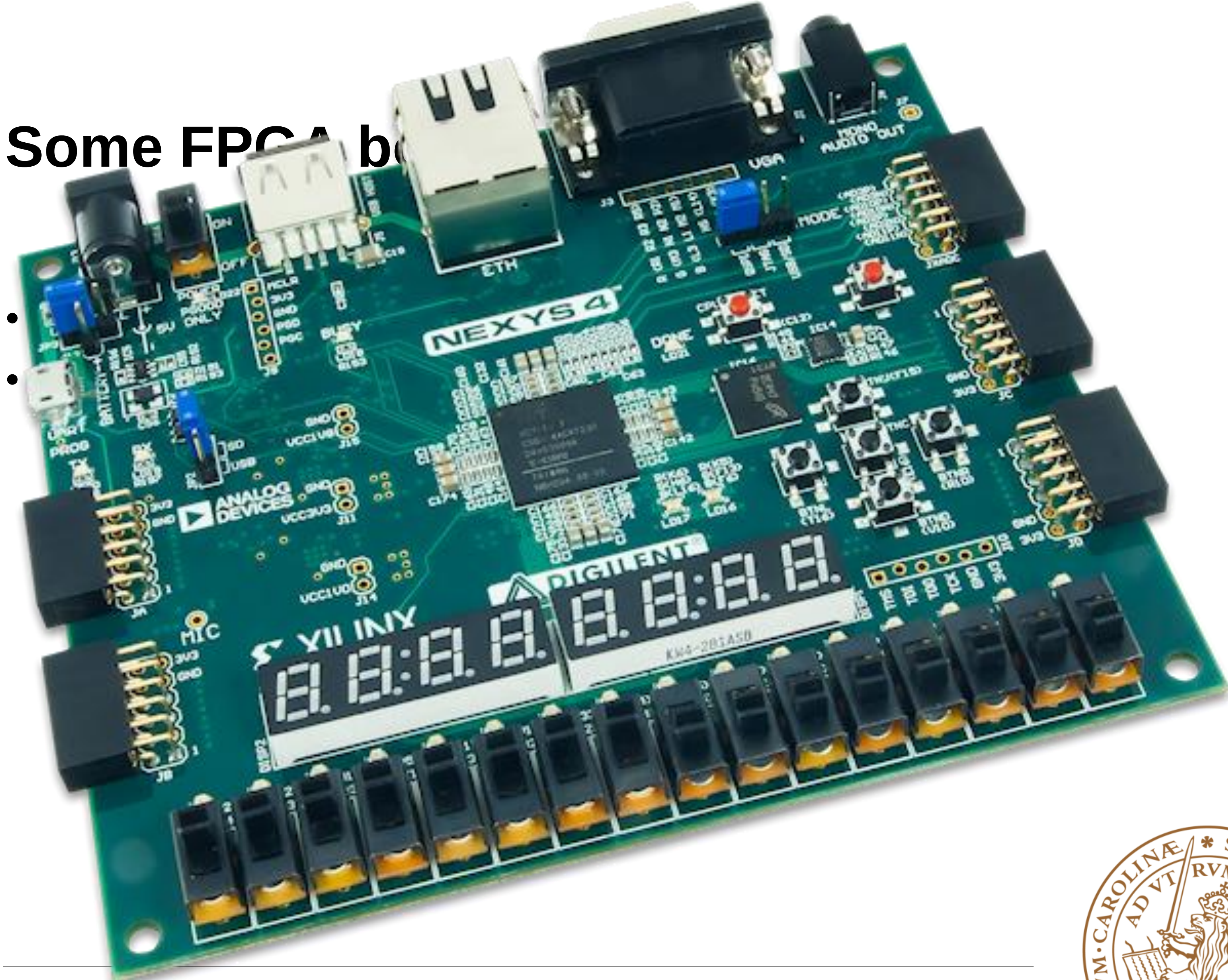
FPGA devices

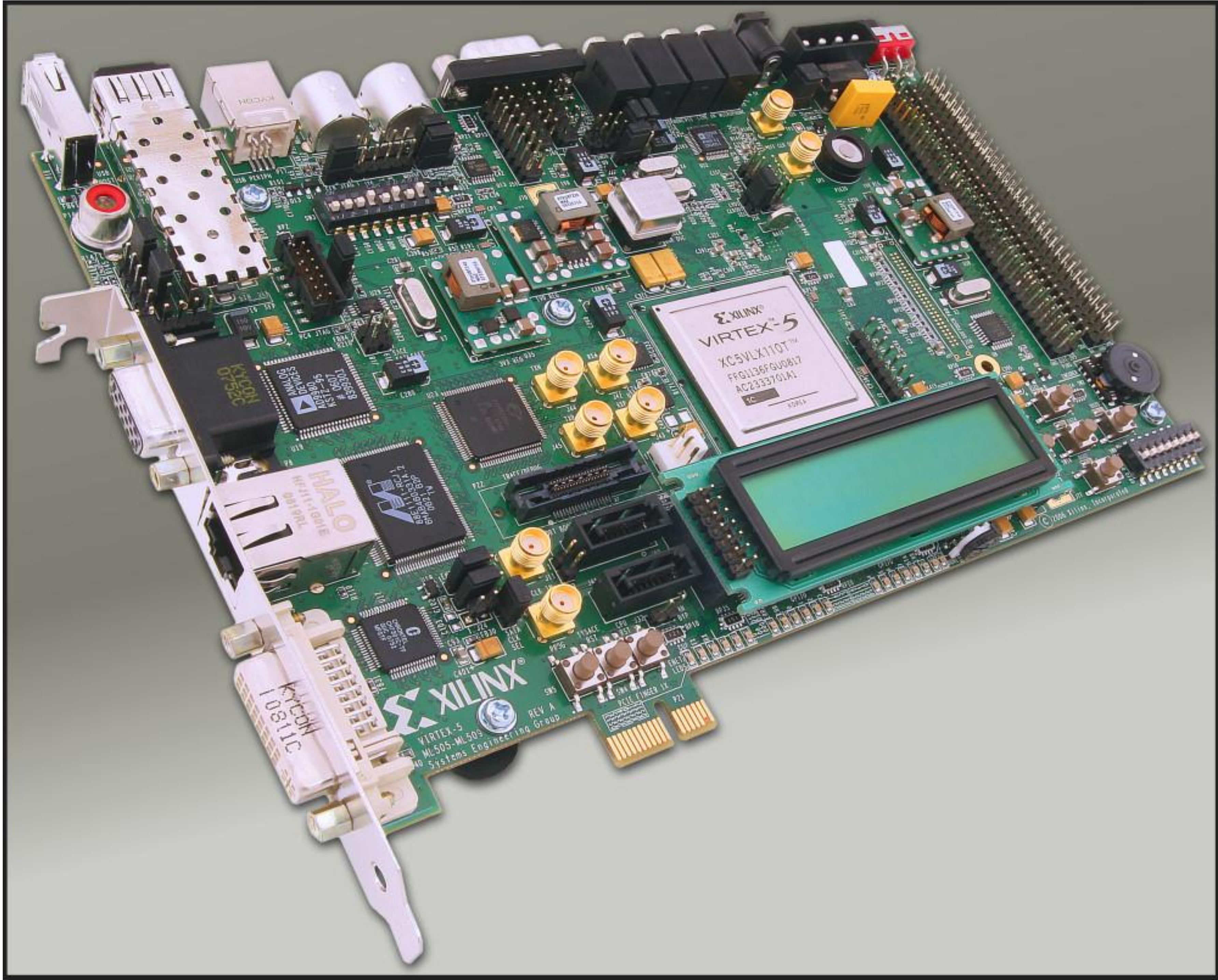
- Manufactures:
  - **Xilinx**: Virtex, Kintex, Artix, Spartan
  - **Altera**: Cyclone, Arria, Stratix
  - Lattice Semiconductor: flash, low power
  - Microsemi (Actel): antifuse, mix-signal
  - Achronix: high speed
  - QuickLogic: application-specific (handheld)



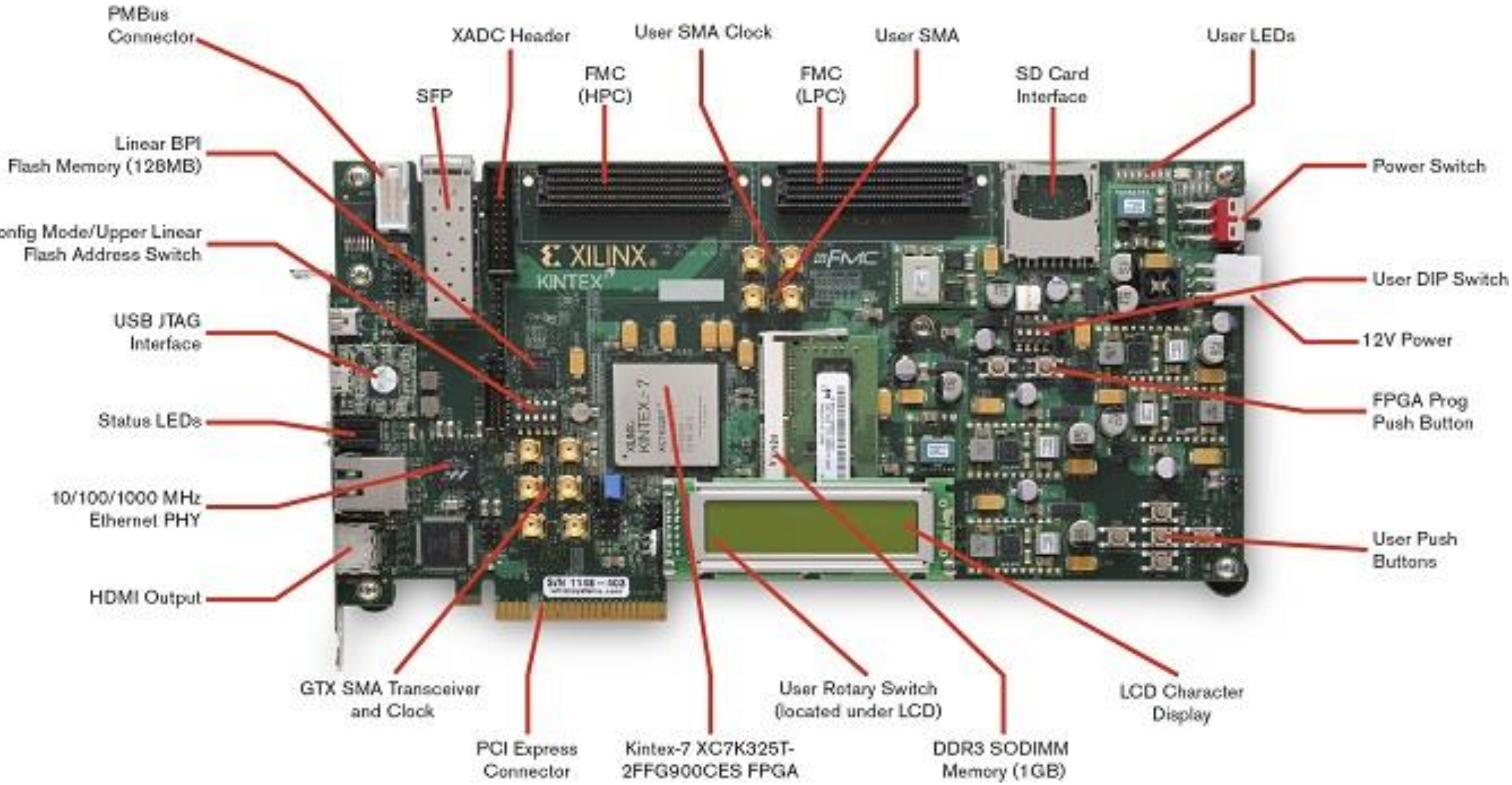
JTAG
Clock ports
Xilinx V5
LX330 FPGA
(1200 I/O)
LOGIC FPGA 2
5x Logic analyzer debug probe sites on main routing (Tek)
1078
8
Debug
E2PROM
(32Kx8)
(3.3V)
SanDisk
RS-232
RS-232
RS-232
5
6
4
4
4
GPIO
DSP
testchip
14
34
34
USB 0
High-speed
Full-speed
USB 1
High-speed
14
13
10
(Ultra Wide-band)
80
73
EMIF 0/2
connector
USB HS
Interchip
JTAG
3.3V
418
JTAG
Clocks
Xilinx V5
LX220 FPGA
(800 I/O)
DSP FPGA
SRAM
(18Mb)
71
24
1.2 / 1.8 / 3.3V
Power
Personality I/F board
connectors (PERC 2.5)
Extension
JTAG SW
X401
346
X402
STAR I/O
31
JTAG
Clock ports
Xilinx V5
LX330 FPGA
(1200 I/O)
LOGIC FPGA 1
280
28
759
8
16
120
1.8 / 3.3V
10
10
320
280
DSP bypass
switches
[Separately
switched banks of
8/16b]
Dedicated
I/O or
common
[Separately
switched
banks of
8/16b]
JTAG
Clocks
Xilinx V5
LX110 FPGA
(800 I/O)
AUX FPGA
SRAM
(72Mb)
79
DISPLAY
Debug
16
USB HS
Interchip
4
EMIF 1
connector
73
JTAG
Clock ports
Xilinx V5
LX330 FPGA
(1200 I/O)
CPU FPGA
1085
JTAG &
ETM
31
USB HS
Interchip
JTAG Debug /
prog. headers
Xilinx ACE
Programmer
SanDisk
2.0GB
FPGA
Image
select
Clock
Dist.
Bank switch controls
Access Headers
External clocks in/out
FPGA point-to-point clocks
Clock oscillators
Power control

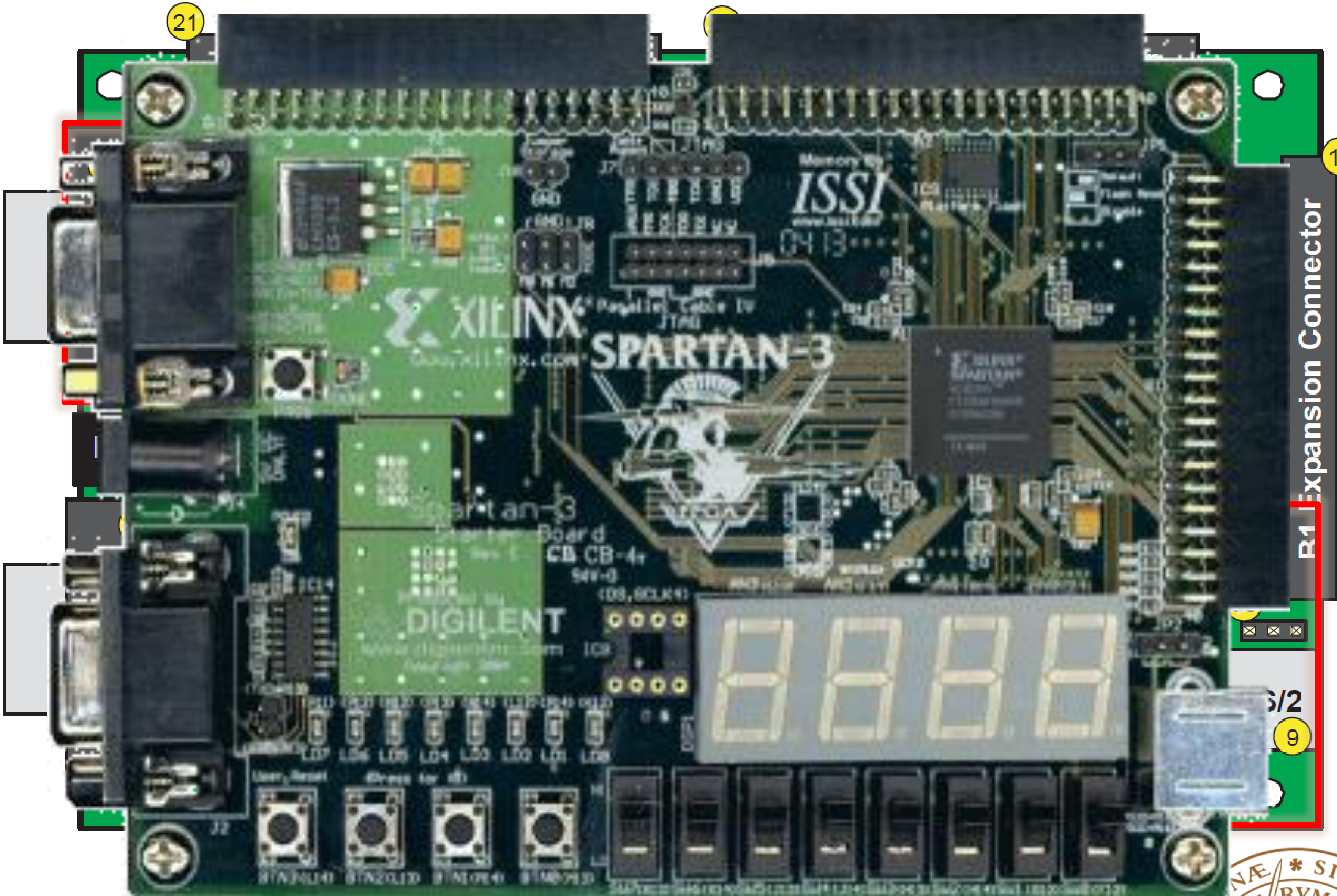
Some FPGA b…


NEXYS 4
DIGILENT
ANALOG DEVICES
VGA
ETH
MONO AUDIO OUT
MODE
DONE
BUSY
MIC
UART PROG
3V3
GND
VCC1V0
VCC3V3
TMS
TDI
TDO
TCK
GND
3V3



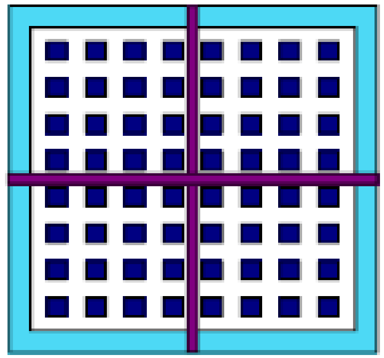
XILINX
VIRTEX-5
XC5VLX110T
XILINX
VIRTEX-5
ML505-ML509
Systems Engineering Group
REV A
HALO
KYCON
PCIE FINGER 1X

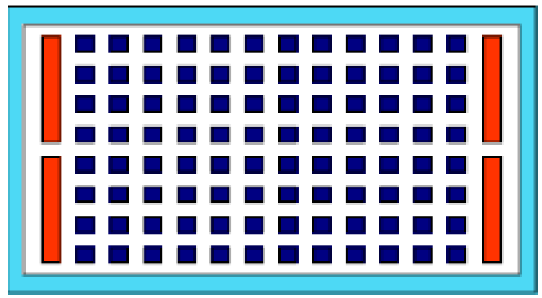

PMBus Connector
XADC Header
User SMA Clock
User SMA
User LEDs
SFP
FMC (HPC)
FMC (LPC)
SD Card Interface
Linear BPI Flash Memory (128MB)
Power Switch
onfig Mode/Upper Linear Flash Address Switch
User DIP Switch
USB JTAG Interface
12V Power
FPGA Prog Push Button
Status LEDs
10/100/1000 MHz Ethernet PHY
User Push Buttons
HDMI Output
GTX SMA Transceiver and Clock
User Rotary Switch (located under LCD)
LCD Character Display
PCI Express Connector
Kintex-7 XC7K325T-2FFG900CES FPGA
DDR3 SODIMM Memory (1GB)
XILINX
KINTEX

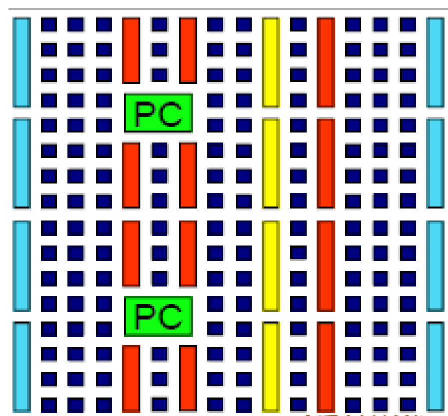

21
19
Expansion Connector
9
XILINX
SPARTAN-3
ISSI
DIGILENT

FPGA architectures

- Early FPGAs
  - N x N array of unit cells (CLB + routing)
  - Special routing along center axis
- Next Generation FPGAs
  - M x N unit cells
  - Small block RAMs around edges
- More recent FPGAs
  - Added block RAM arrays
  - Added multiplier cores
  - Added processor cores







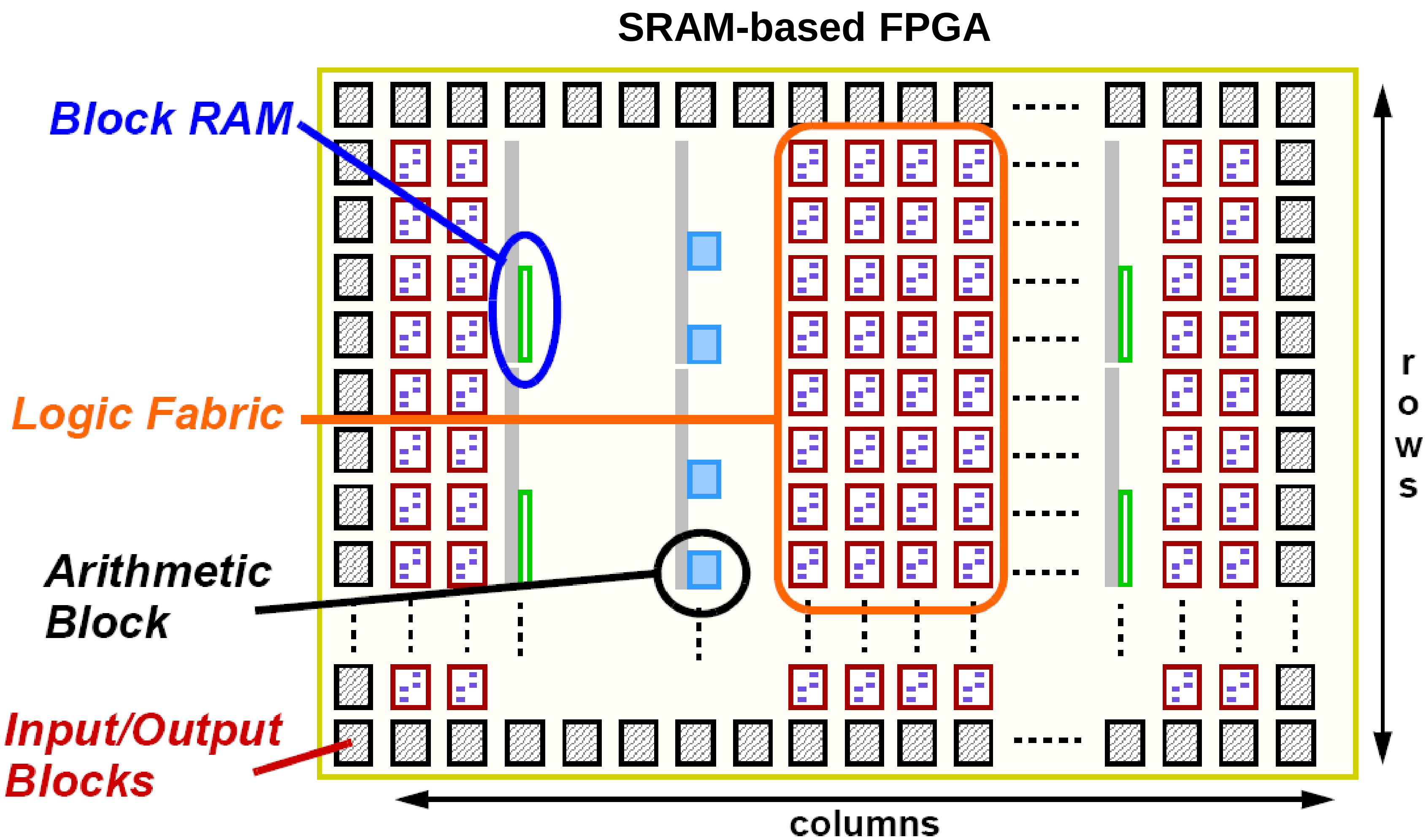
FPGA architecture trends

- Memories
  - Single & Dual-port RAMs
- Digital Signal Processor Engines
- Embedded Processors
  - Hardcore (dedicated processors)
  - Soft core (synthesized from a HDL)
- High speed/performance I/O connectivity
  - PCIe interface block
  - I/O transceiver
- Clock management blocks

Programming technology

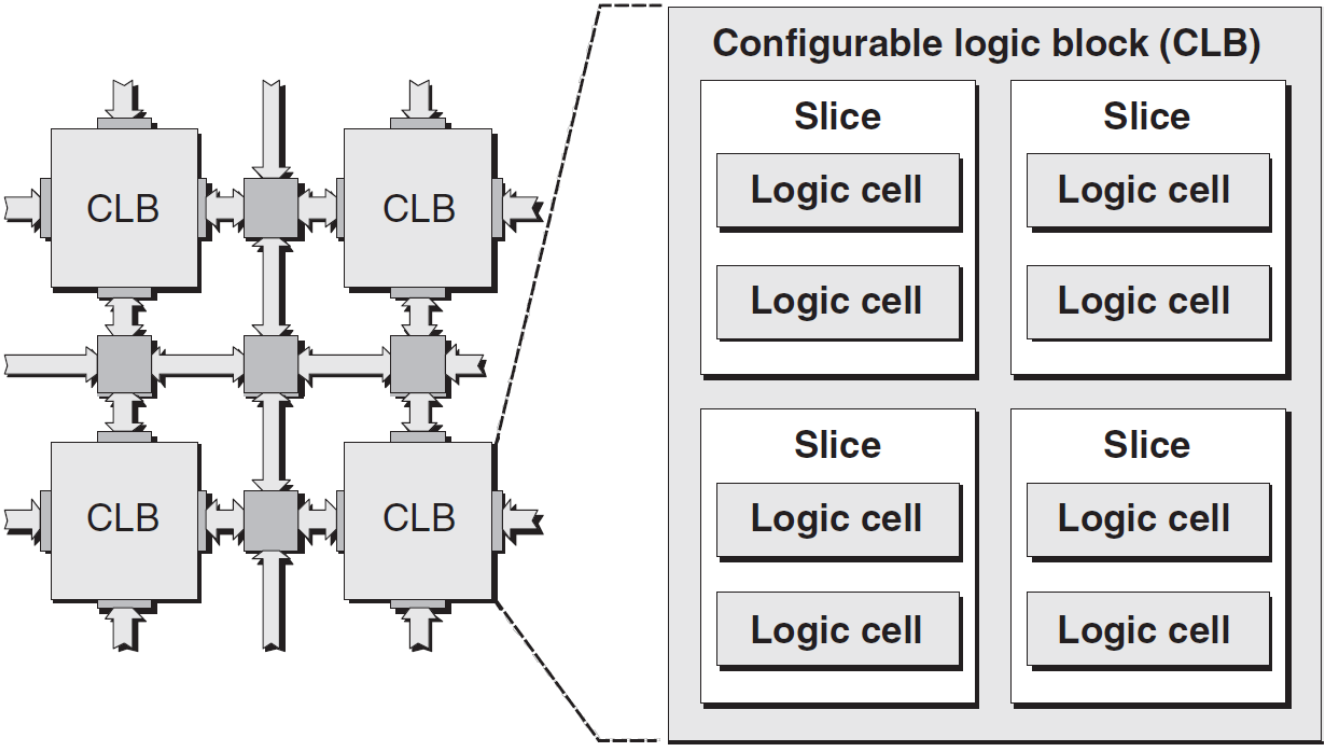
Feature	SRAM	Antifuse	Flash/E2PROM
Technology	State-of-the-art	One or more generations behind	One or more generations behind
Reprogrammable	Yes (in system)	No	Yes (in system or offline)
Reprogramming speed	Fast	---	3x slower than SRAM
Volatile	Yes	No	No
Instant-on	No	Yes	Yes
Security	Acceptable	Very Good	Very Good
Size of Config. Cell	Large (Six transistors)	Very small	Medium-small (Two transistors)
Power consumption	Medium	Low	Medium

Xilinx FPGA architecture



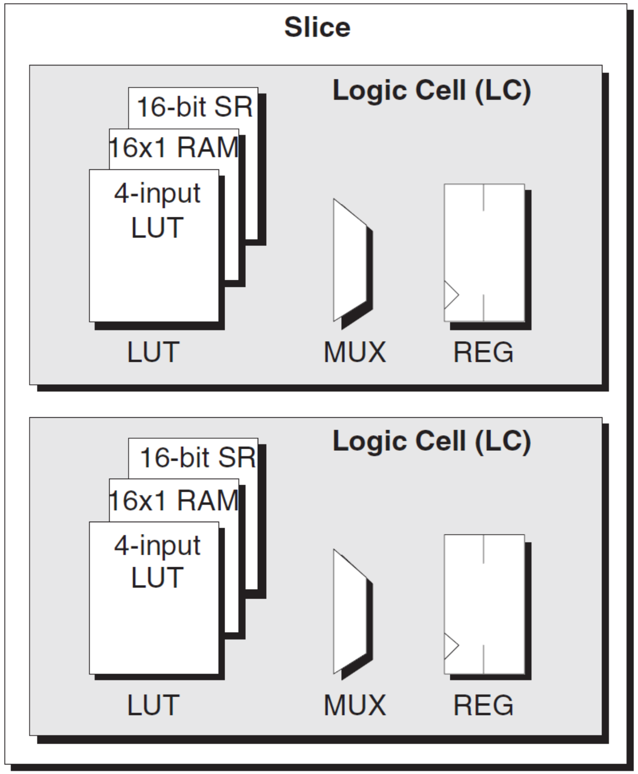
Configurable logic block (CLB) (I)

- One CLB contains four slices

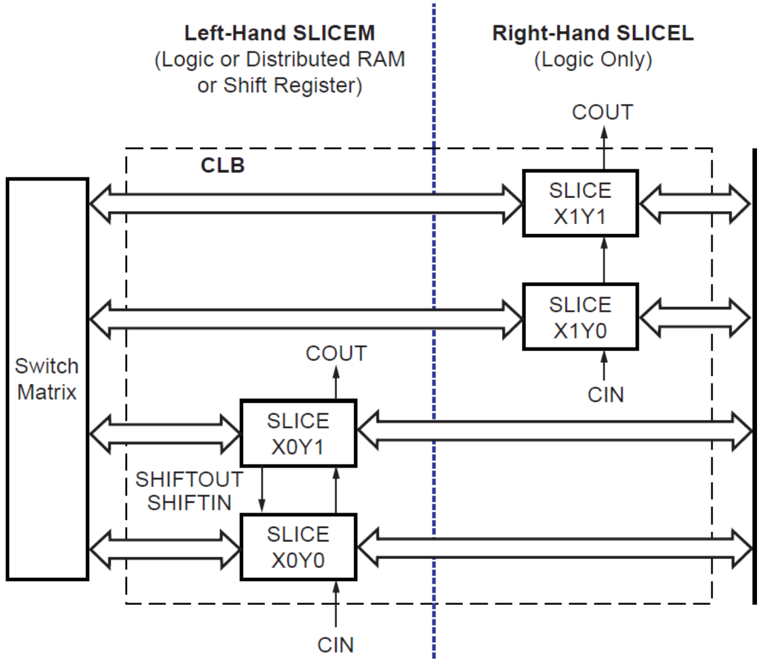


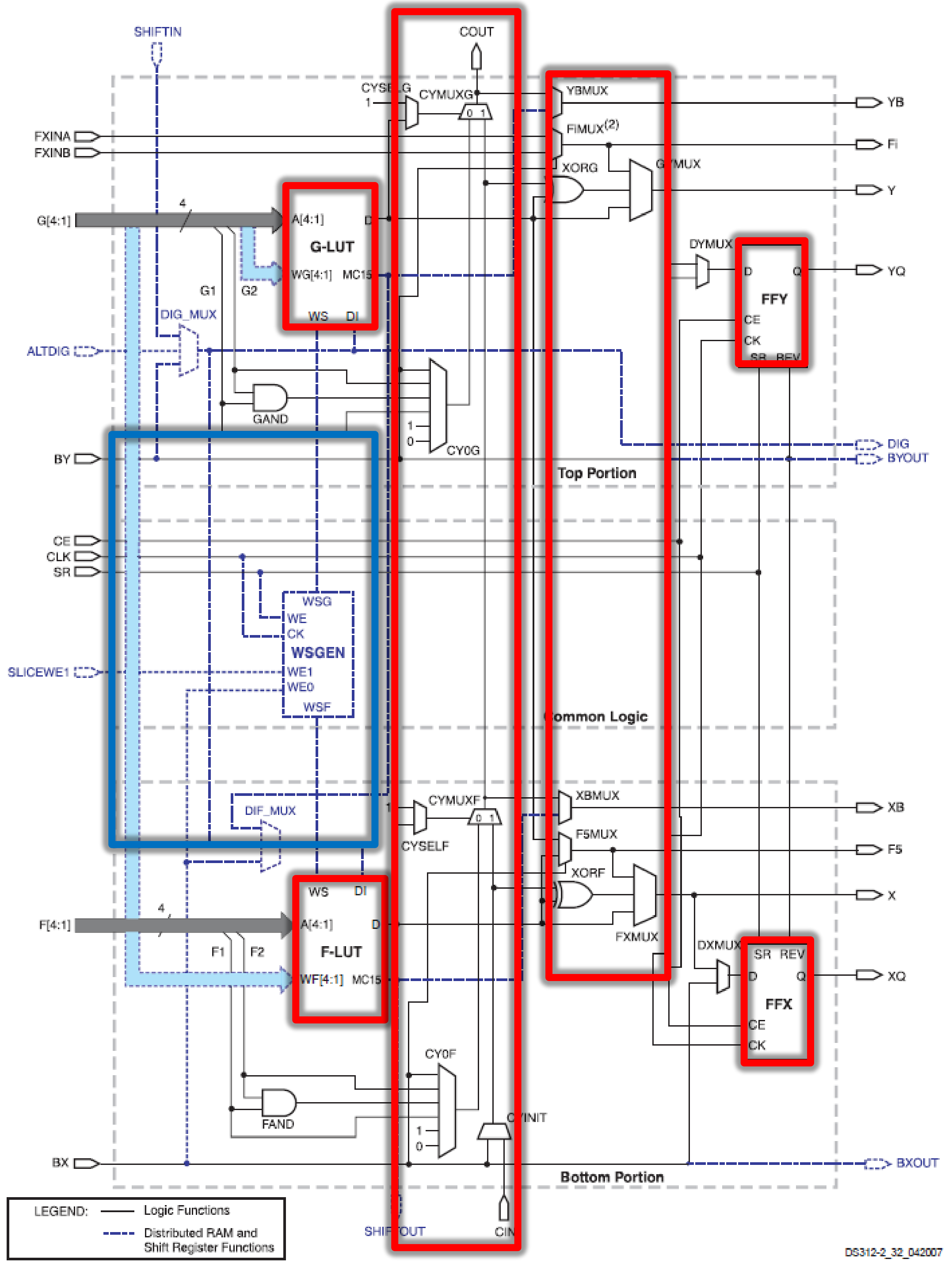
Configurable logic block (CLB) (II)

- One CLB contains four slices
- Each slice:
  - Two Look-up tables (LUTs)
  - Two D Flip-Flops (DFFs)
  - Multiplexers and arithmetic gates
  - Carry logic
- Left-hand slice (SLICEM)
  - Distributed RAM
  - Shift register

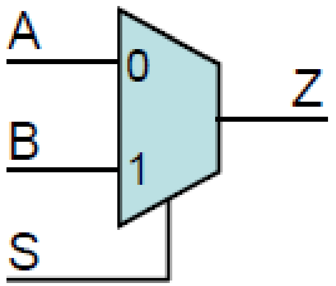


Configurable logic

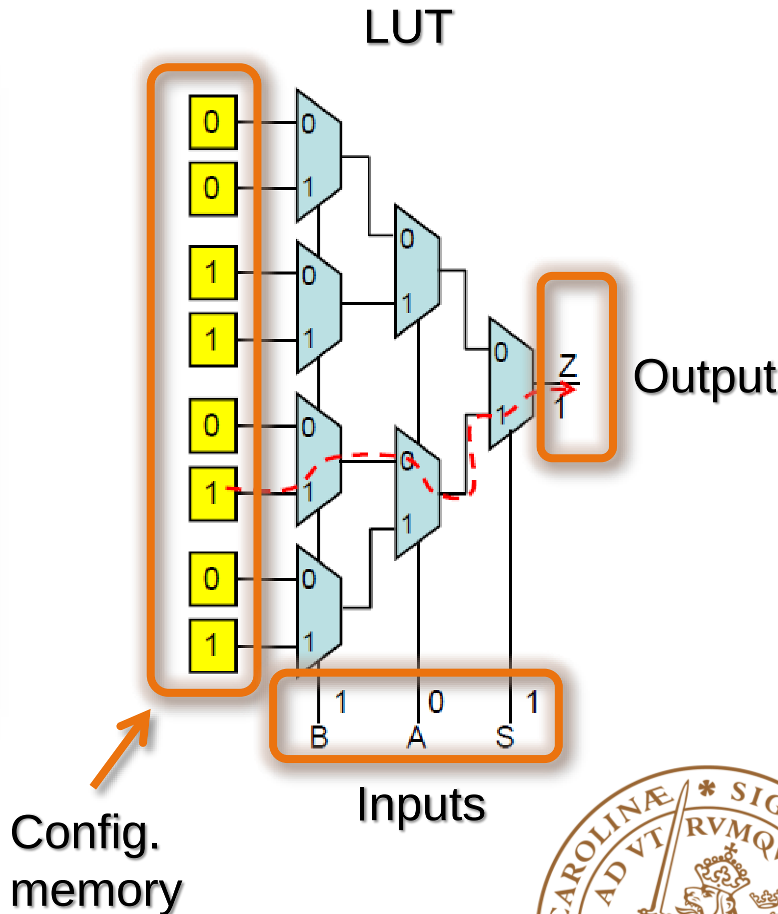




Look-up table (LUT) (I)

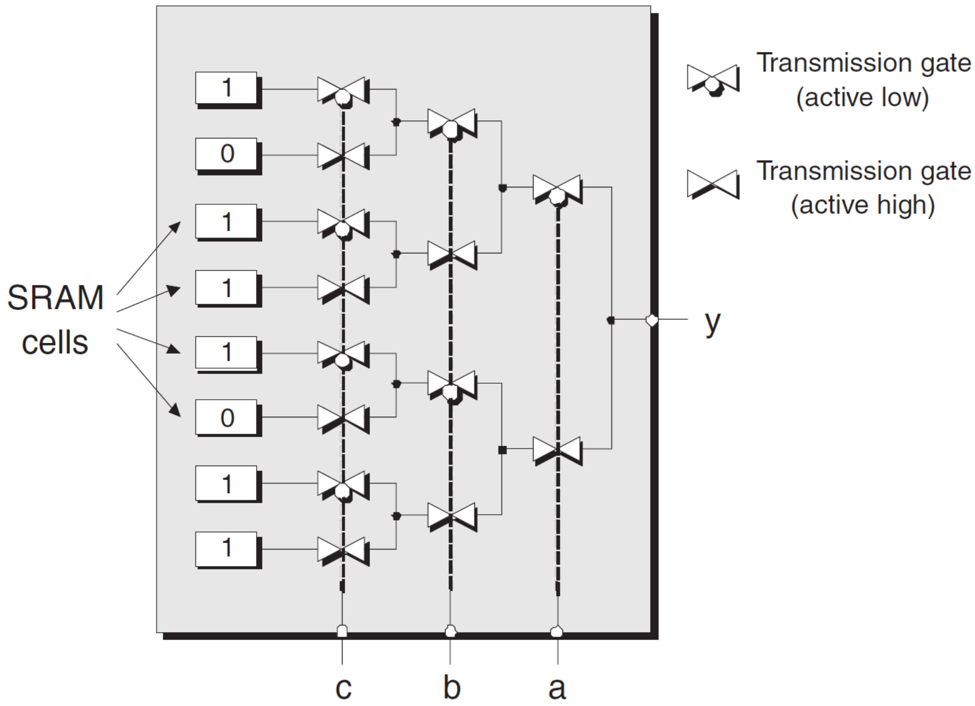


S	A	B	Z
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	0
1	1	1	1



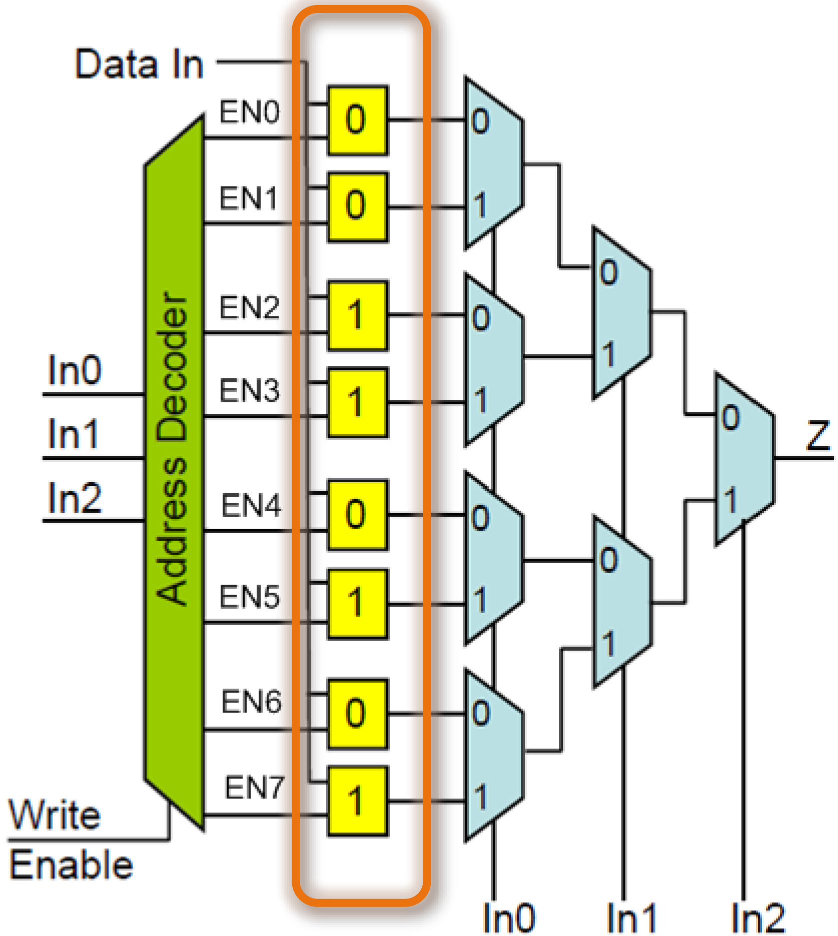
Look-up table (LUT) (II)

- Inputs are used as a pointer into a LUT.
- Decoded using a hierarchy of transmission-gate MUXs.
- Transmission-gate: “pass” or “high-impedance”.



LUT based RAM (Distributed RAM)

- Normal LUT performs “read” operation.
- For “write” operation, address decoders + write enable.
- Can be concatenated to created larger RAMs.
- Can also be used as shift registers (some of the LUTs).



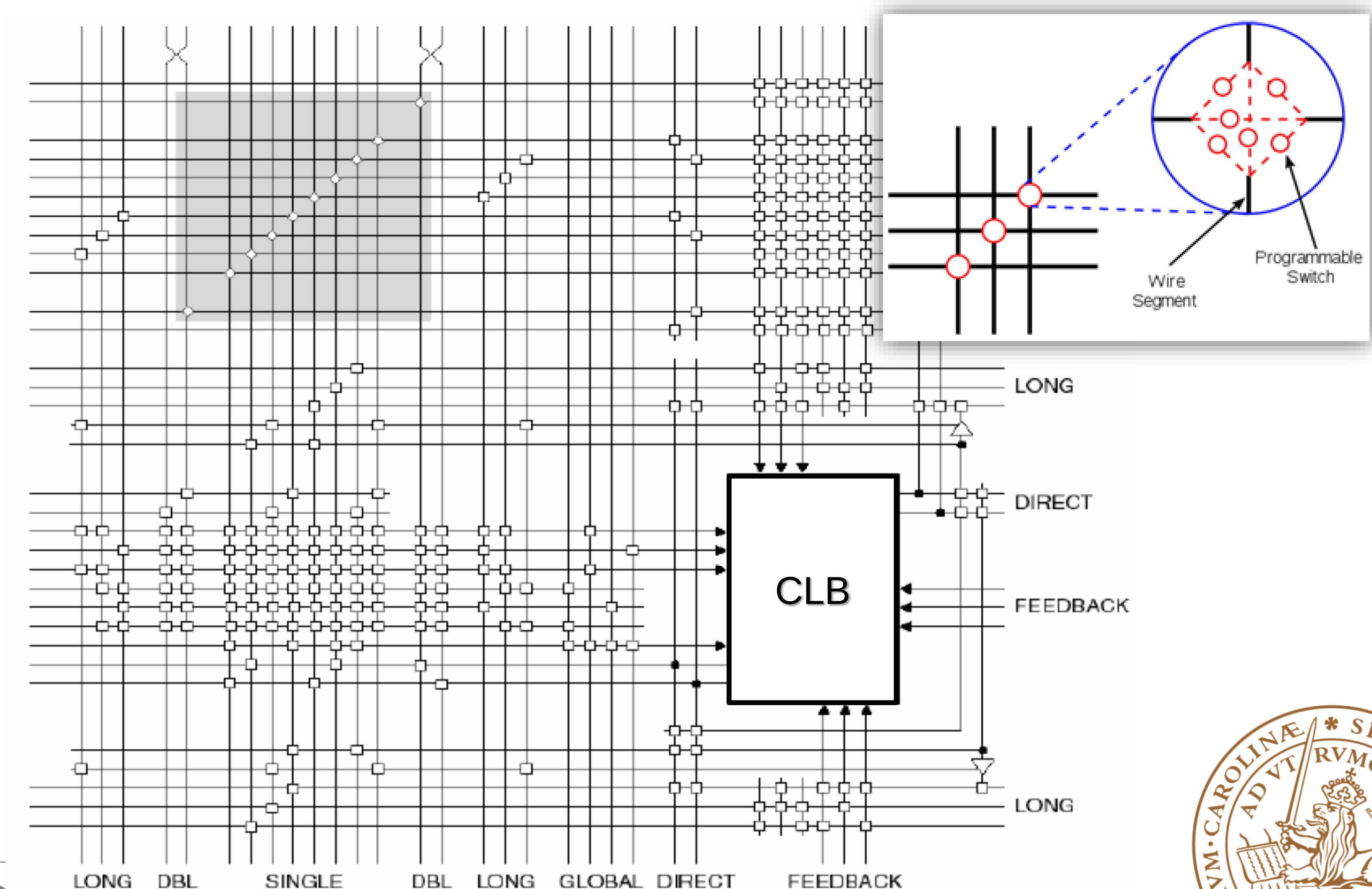
Xilinx Spartan-3 FPGAs

- XC3S200:
  - 480 CLBs = 480*4 Slices = 480*4*2*(4-input LUTs + registers)
  - 12 18-kbit dual-port BRAMs = 12*18 Kb = 216 Kbits
  - Distributed RAM: 480*2*2*2^4 = 30,720b = 20Kb (only 2 LUTs per slice)

Device	System Gates	Equivalent Logic Cells[1]	CLB Array (One CLB = Four Slices)			Distributed RAM Bits (K=1024)	Block RAM Bits (K=1024)	Dedicated Multipliers	DCMs	Maximum User I/O	Maximum Differential I/O Pairs
			Rows	Columns	Total CLBs						
XC3S50[2]	50K	1,728	16	12	192	12K	72K	4	2	124	56
XC3S200[2]	200K	4,320	24	20	480	30K	216K	12	4	173	76
XC3S400[2]	400K	8,064	32	28	896	56K	288K	16	4	264	116
XC3S1000[2]	1M	17,280	48	40	1,920	120K	432K	24	4	391	175
XC3S1500	1.5M	29,952	64	52	3,328	208K	576K	32	4	487	221
XC3S2000	2M	46,080	80	64	5,120	320K	720K	40	4	565	270
XC3S4000	4M	62,208	96	72	6,912	432K	1,728K	96	4	633	300
XC3S5000	5M	74,880	104	80	8,320	520K	1,872K	104	4	633	300

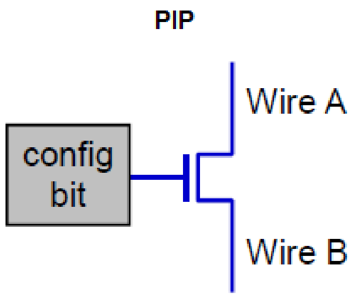
Notes:
1. Logic Cell = 4-input Look-Up Table (LUT) plus a 'D' flip-flop. "Equivalent Logic Cells" equals "Total CLBs" x 8 Logic Cells/CLB x 1.125 effectiveness.
2. These devices are available in Xilinx Automotive versions as described in DS314: Spartan-3 Automotive XA FPGA Family.

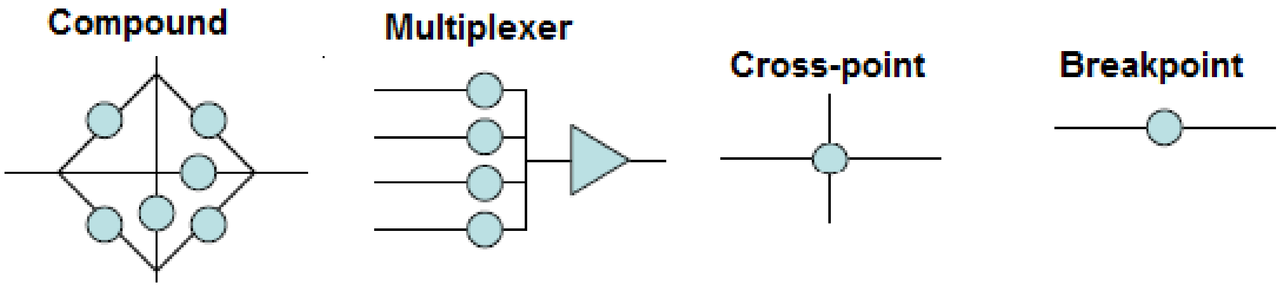
Programmable Interconnects (I)



Programmable Interconnects (II)

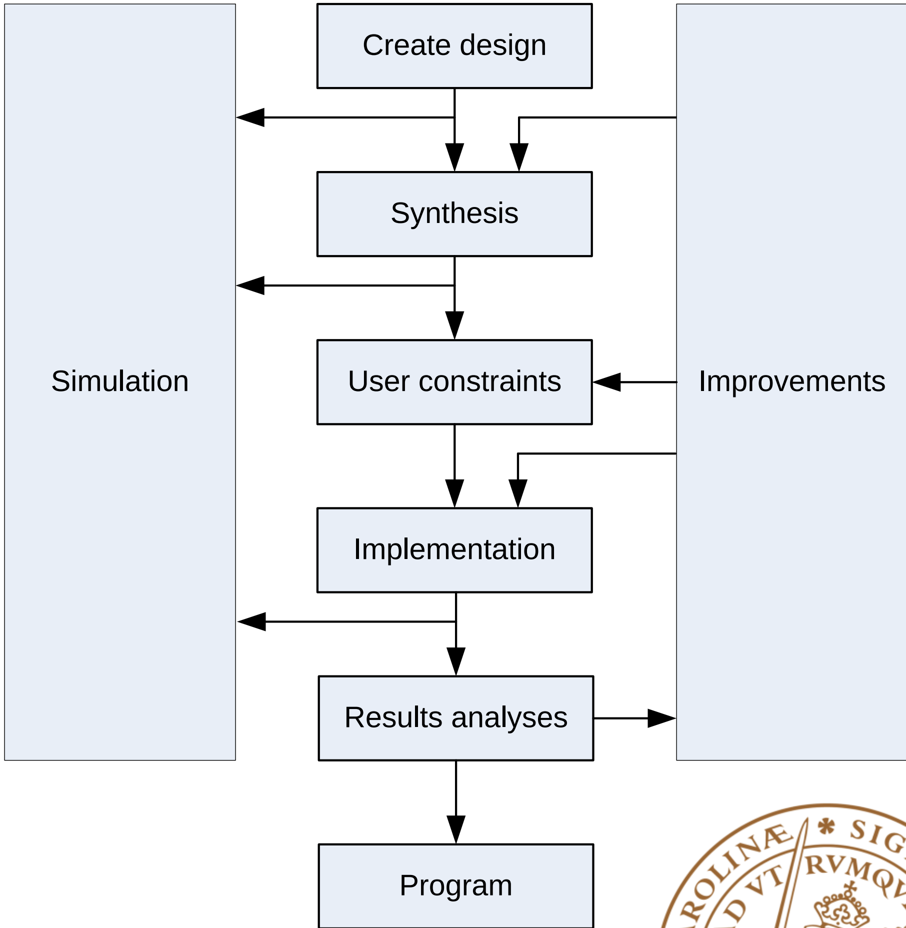
- Programmable swich, also called programmable interconnect points (PIP).
- Implemented using transmission gates.
- Several types of PIPs:



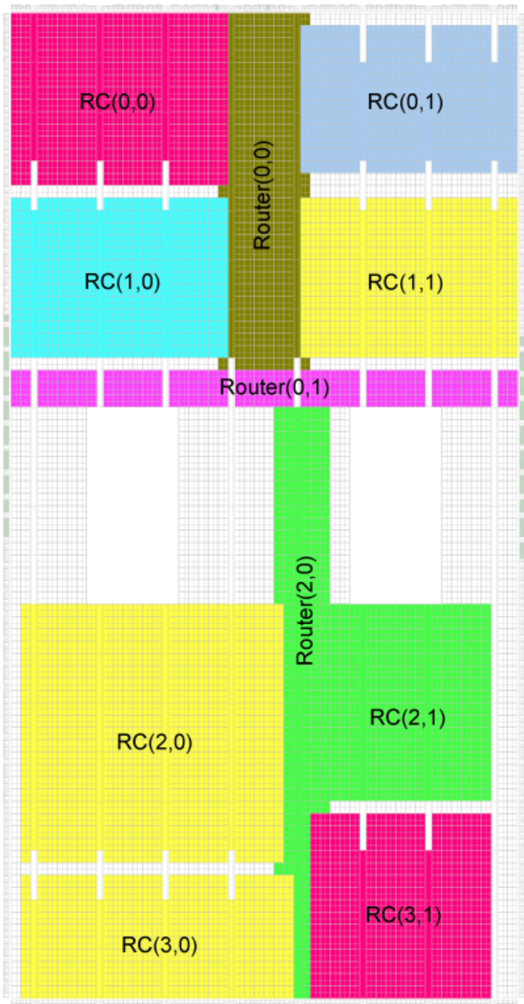


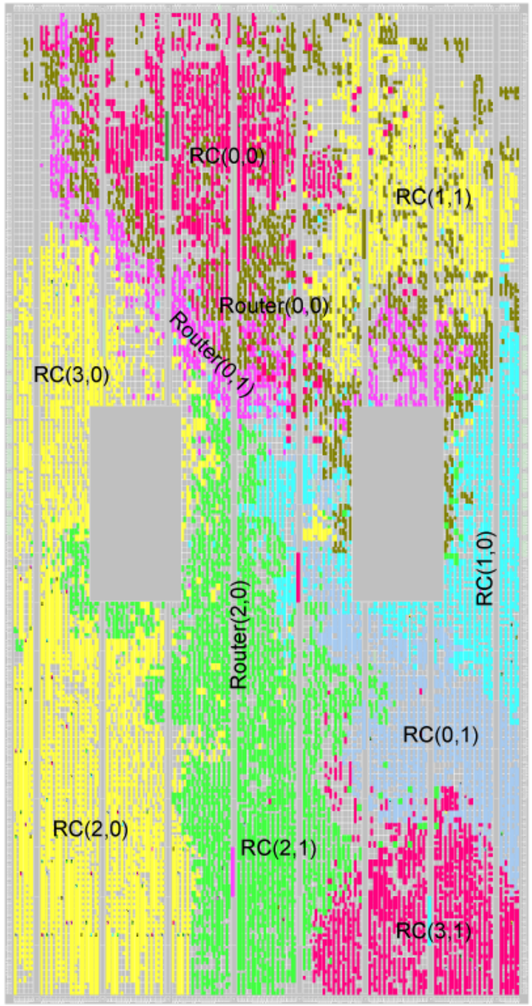
FPGA Design flow

- Synthesis
  - Parses HDL design
  - Infers Xilinx primitives
  - Generates design netlist
- Translate
  - Merges incoming netlists and constraints into a design file
- Map
  - Maps (places) design into the available resources on the target device
- Place and Route
  - Places and routes design

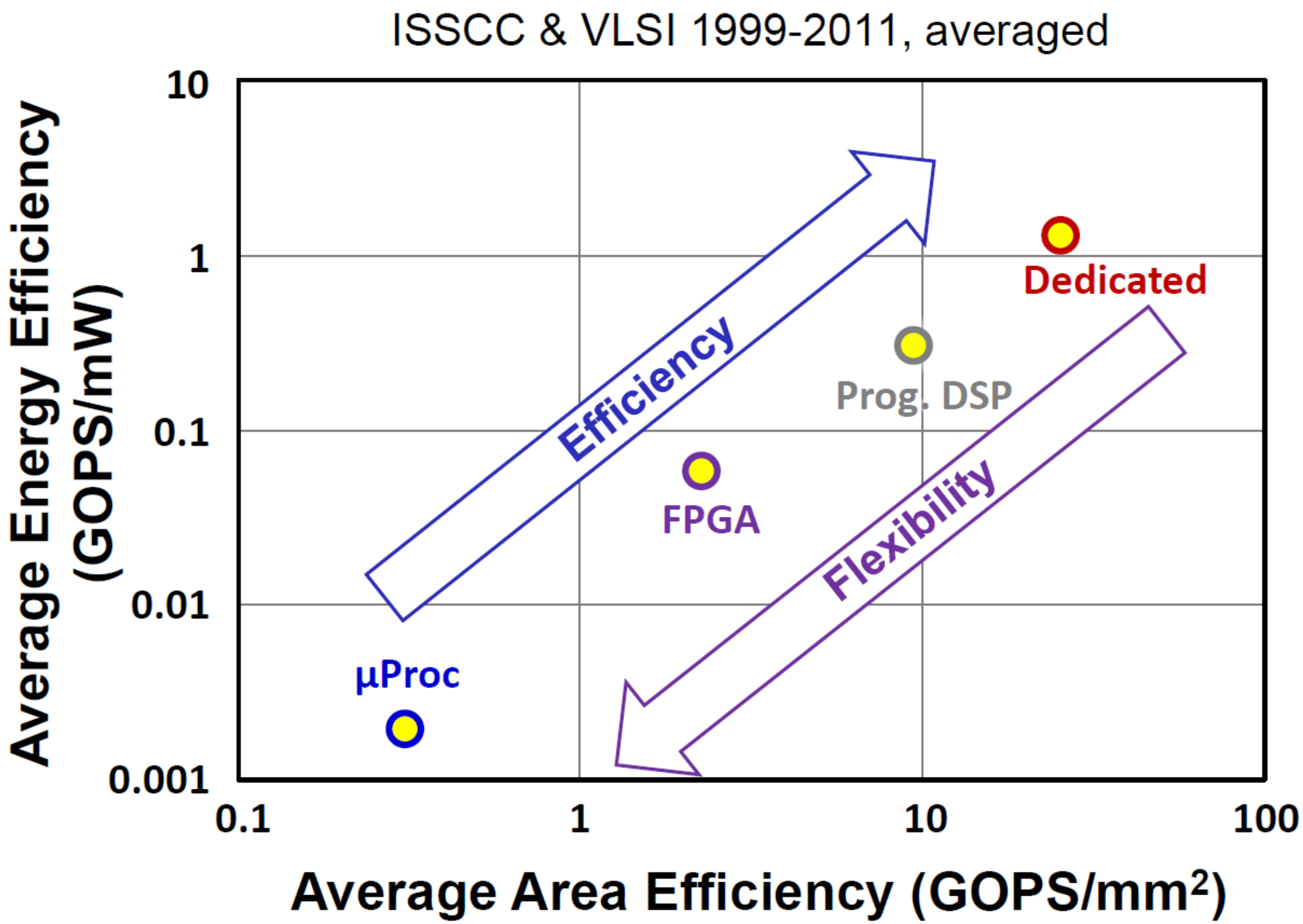


Synthesis constraints



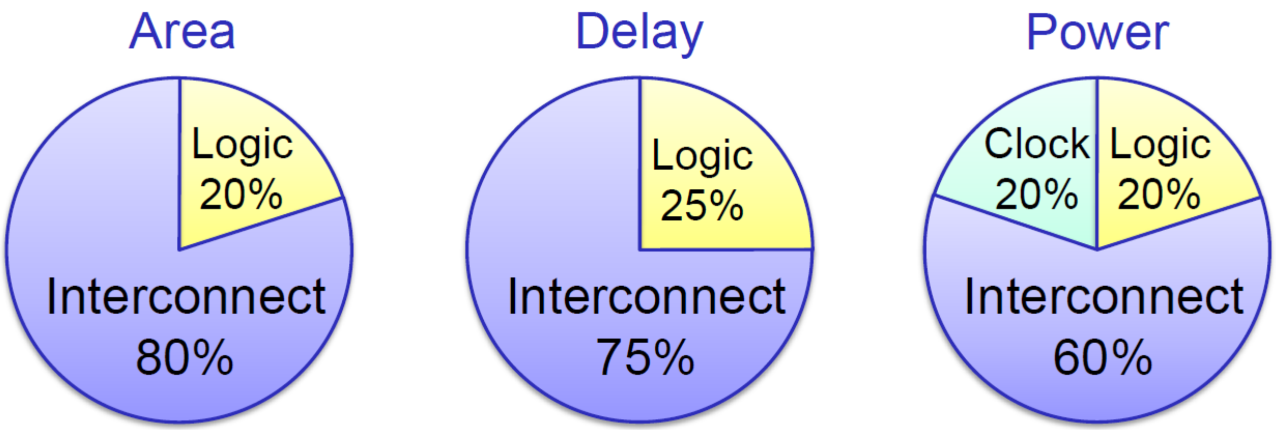


Are FPGAs perfect?



FPGAs are inefficient

- Compared to ASICs, penalties in FPGAs:
  - Area: 17 – 54x
  - Speed: 3 – 7x
  - Power: 6 – 62x
- Main culprit: **INTERCONNECT!**

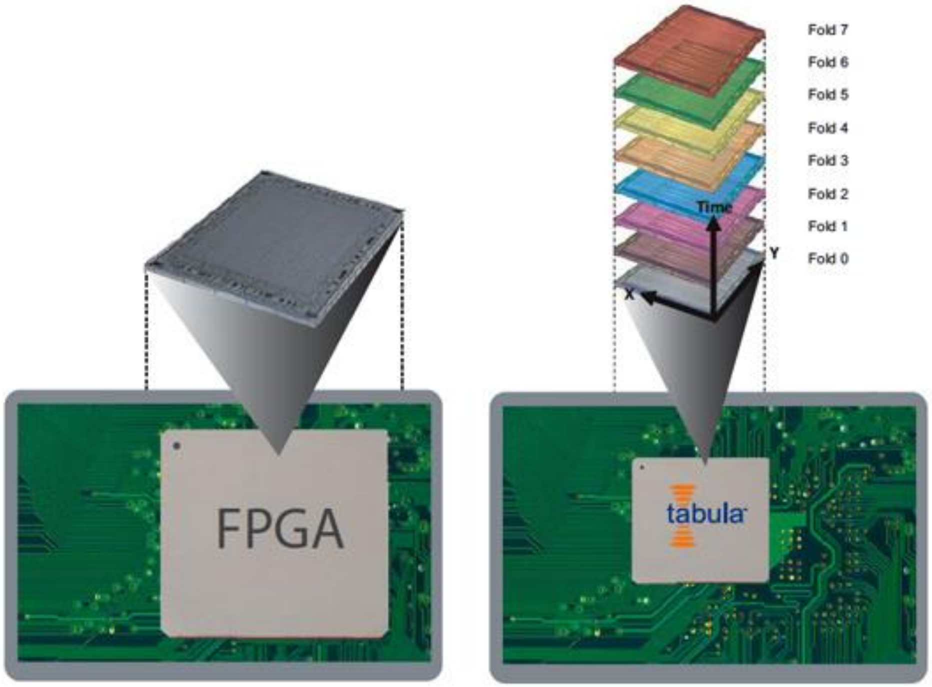


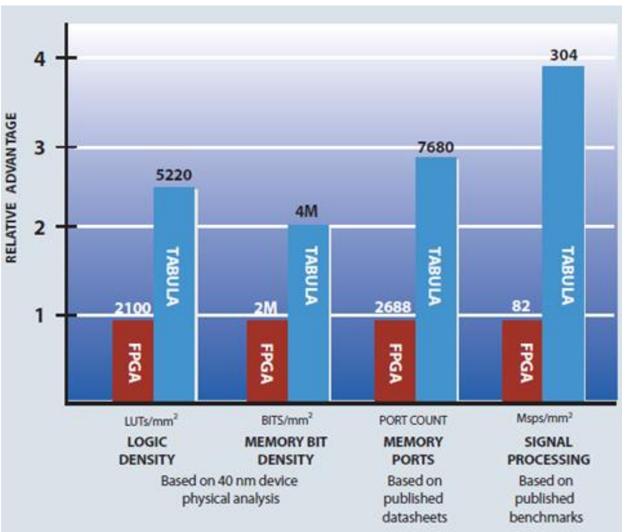
Tabula Spacetime

- Ultra-rapid full/partial reconfiguration with makes it possible to fold more functions onto the same hardware:

  multi-GHz rates
- Their claim:
  - 2.5x logic density
  - 3.7x DSP performance

www.tabula.com





Coarse-grained reconfigurable architecture

- Currently in FPGA
  - Dedicated building blocks: multiplier, DSP core, processor
  - Partial configuration
- Moving torwards coarse-grained architecture:
  - Block-level instead of bit manipulations
  - Lower area and power consumption
  - High-level programming: e.g. xilinx vivado
  - Run-time configuration

References

- Clive "Max" Maxfield, "The Design Warrior's Guide to FPGAs – Devices, Tools and Flows", ELSEVIER, 2004.
- Bill Jason P. Tomas, "Introduction to Field Programmable Gate Arrays (FPGAs)".
- Xilinx, "Spartan-3 FPGA Family Data Sheet".