EITF35: Introduction to Structured VLSI Design

Part 1.1.2: Introduction (Digital VLSI Systems)

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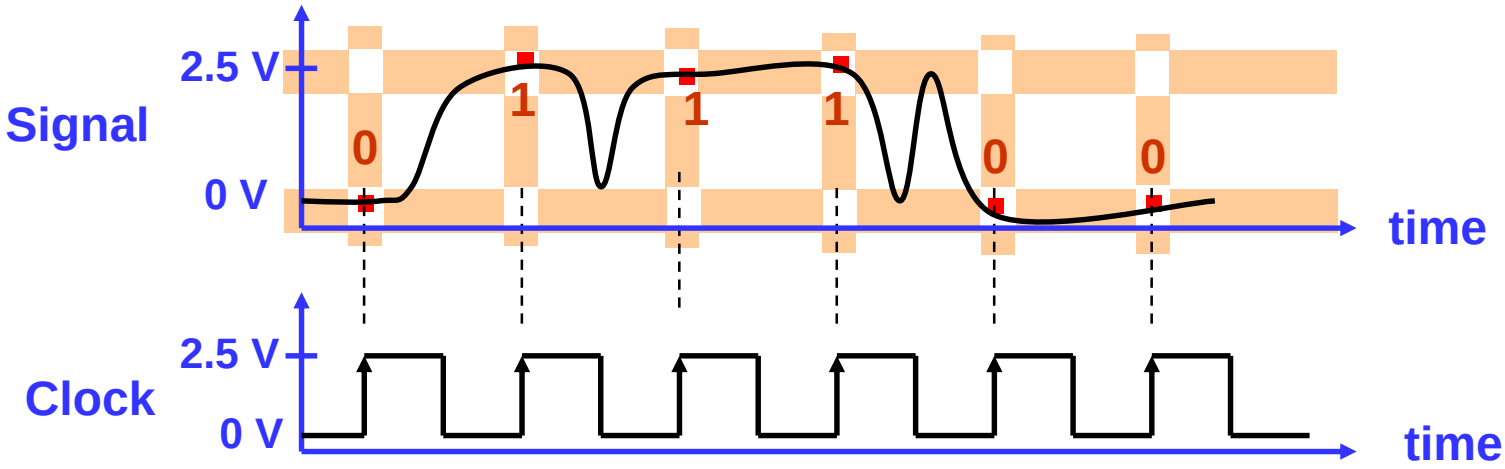
Outline

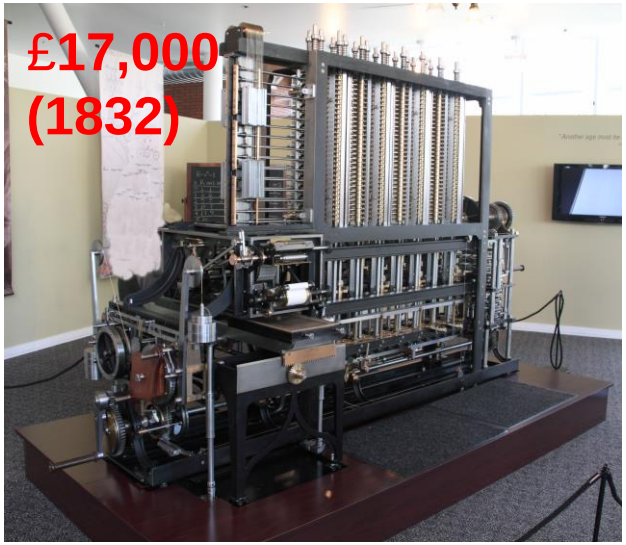
- **Why Digital?**
  - Advantages
  - Some applications
- **History & Roadmap**
- **Device Technology & Platforms**
- **System Representation**
- **Design Flow**
- **RTL Basics**

Digitalization

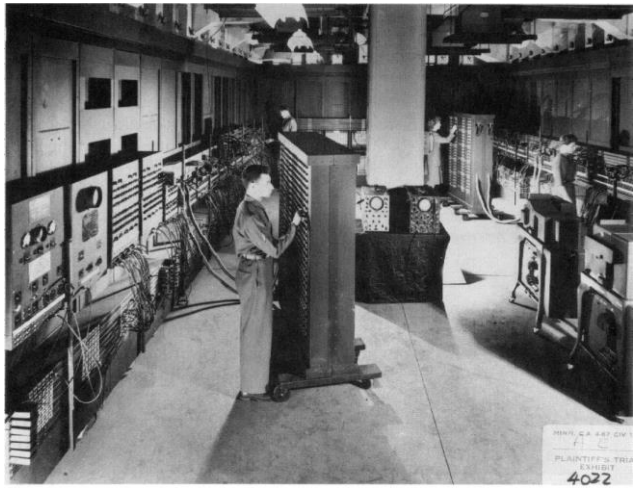


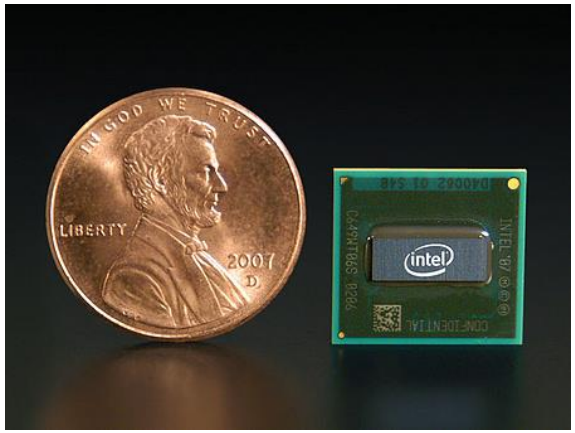
- **Digital is an abstraction**
  - Discrete in time: Sampling
  - Discrete in value: Quantization
- **Digital vs. Analog**
  - Flexibility & functionality: easier to store and manipulate information
  - Reliability: tolerant to noise, mismatch, variations, etc.
  - Economic: easy to design, and friendly to technology evolvement
  - Analog interface is needed

Applications 4C:CCCC



Computation





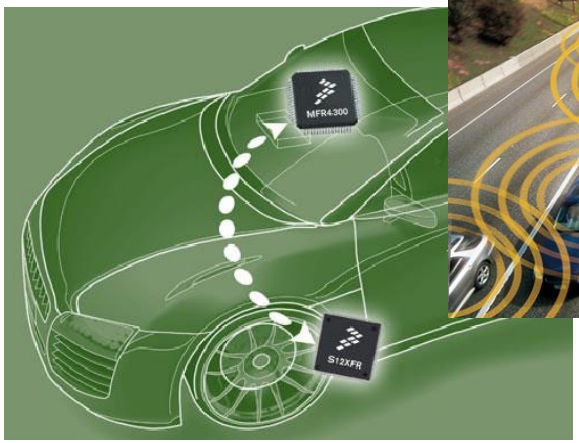
$1,000

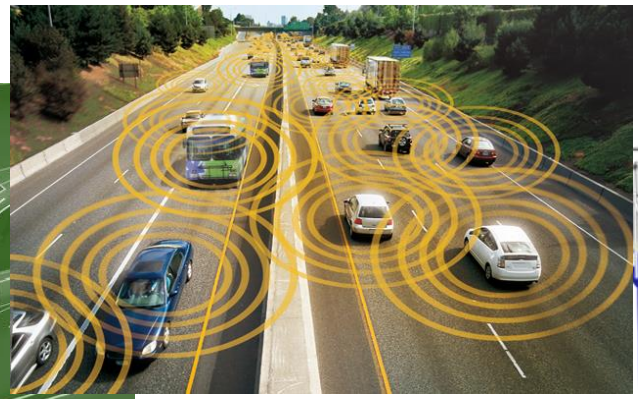
Applications: CCCC

Communication

Applications: CCCC

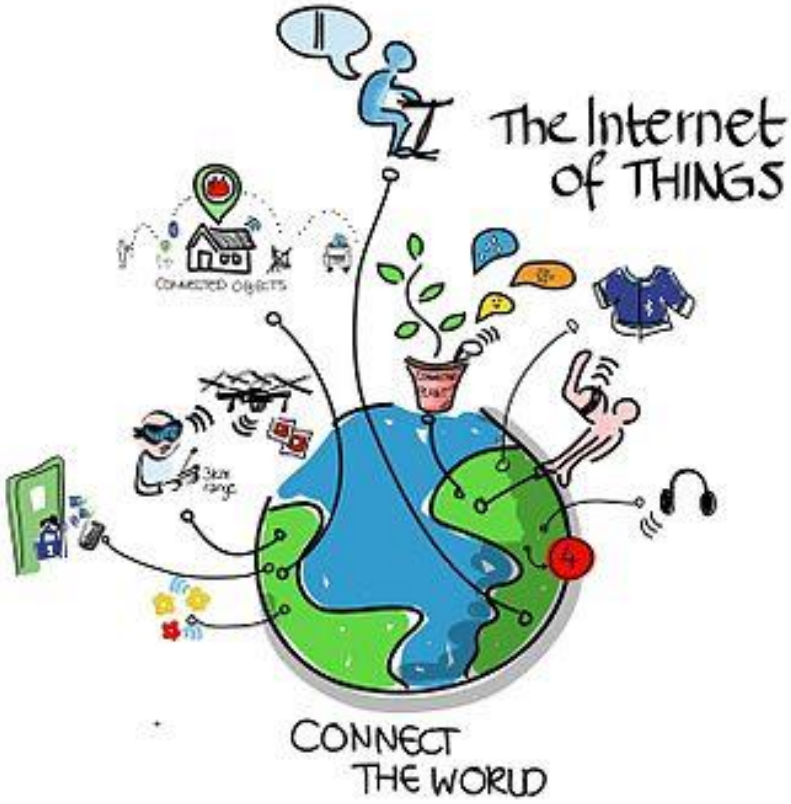
Consumer





Control

Trends



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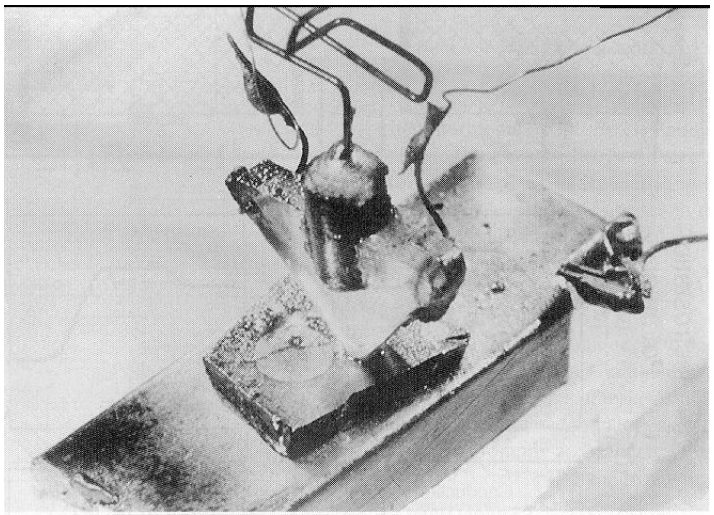
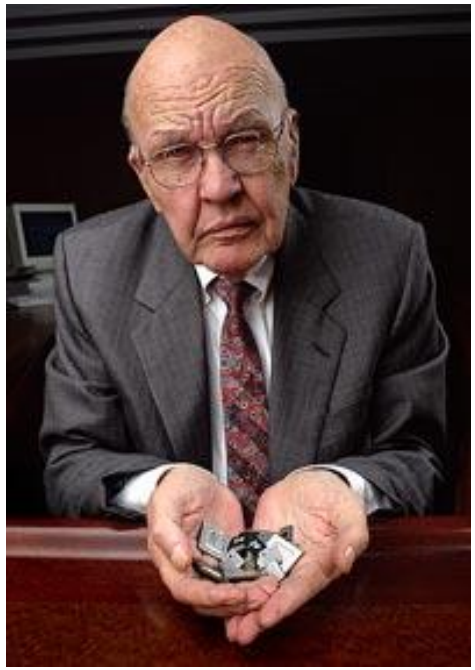
Brief History

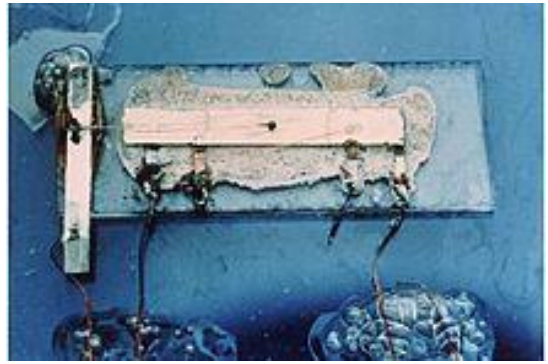
- **Transistor Evolution**
  - First Transistor
    - ***Bell Labs (1947)***
    - ***Bardeen, Brattain, Shockley***
    - ***Nobel Prize (1956)***



Brief History

- **Integration Evolution**
  - First Integrated circuit
    - ***Jack Kilby***
    - ***TI (1960)***
    - ***Nobel Prize (2000)***





"a body of semiconductor material ... wherein all the components of the electronic circuit are completely integrated."

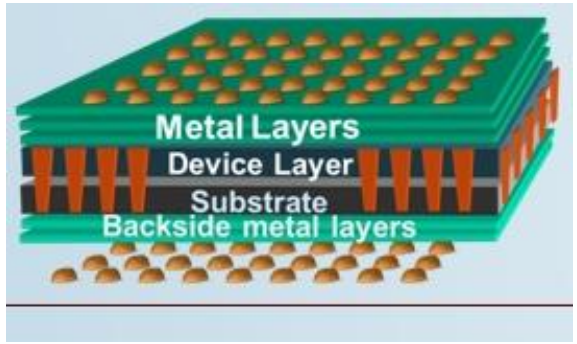
Technology Evolution

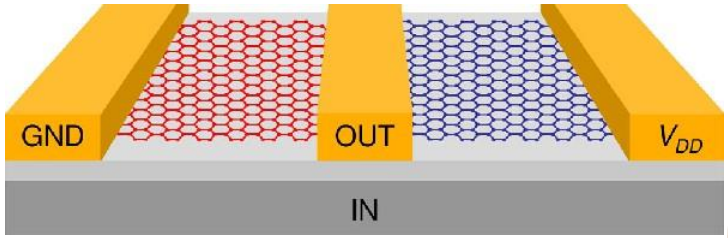
- **Bipolar**
  - Transistor
    - ***1947, Bardeen/Bell Lab***
  - Bipolar junction transistor
    - ***1949, William Shockley***
  - Logic gate
    - ***1956, Harris***
  - Integrated circuit
    - ***1958, Kilby/Noyes***
  - Transistor–transistor logic (TTL)
    - ***1962, James L. Buie***
  - High-speed Emitter-coupled logic (ECL)
    - ***1974, Masaki***

- **MOSFET (metal-oxide-semiconductor field-effect transistor)**
  - Bipolar faces power and size limitation
  - **CMOS logic gate**
    - ***1963, Wanlass***
  - PMOSFET
    - ***1970, first practical MOS IC, Calculator***
  - NMOSFET
    - ***1970, high-density storay(4K)***
    - ***1972, first microprocessor(4004)***
    - ***1974, 8080 microprocessor***

Technology Evolution (cont.)

- **Main trend today**
  - Since early 80's until today, ***CMOS*** became dominant.
  - Again, ***power consumption*** is now becoming a problem.
- **For higher performance, other technologies are used**
  - Bi-CMOS (bipolar-CMOS): High speed memory and gate arrays.
  - ECL (Emitter-coupled logic): Even higher performance.
  - SOI (Silicon on insulator): high-performance radio frequency (RF) and radiation-sensitive applications
- **What's Next?**
  - ***3D-IC, FinFET***
  - Integrated photonics circuit
  - Superconducting electronics
  - Quantum circuit
  - ***Graphene circuit***





Moore's Law

The experts look ahead

Cramming more components onto integrated circuits

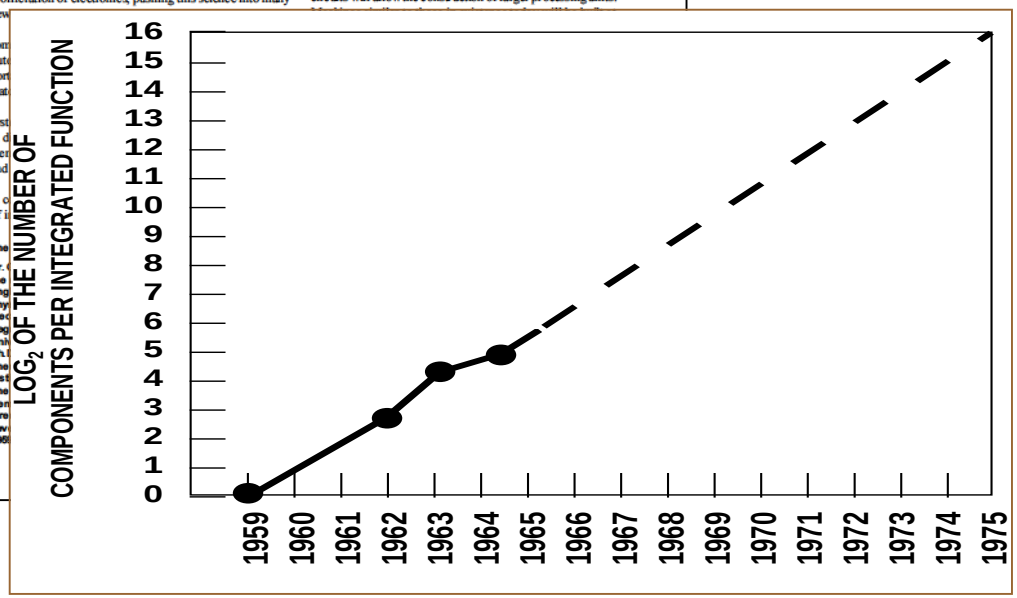
With unit cost falling as the number of components per circuit rises, by 1975 economics may dictate squeezing as many as 65,000 components on a single silicon chip

By Gordon E. Moore

Director, Research and Development Laboratories, Fairchild Semiconductor division of Fairchild Camera and Instrument Corp.

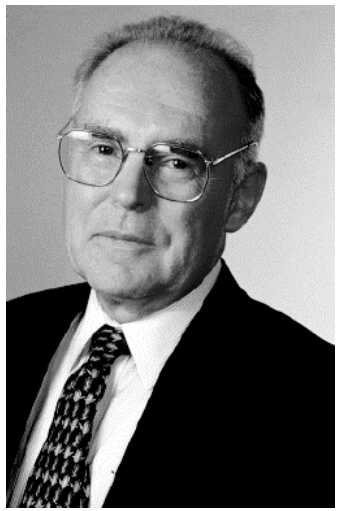
The future of integrated electronics is the future of electronics itself. The advantages of integration will bring about a proliferation of electronics, pushing this science into many

machine instead of being concentrated in a central unit. In addition, the improved reliability made possible by integrated circuits will allow the construction of larger processing units.

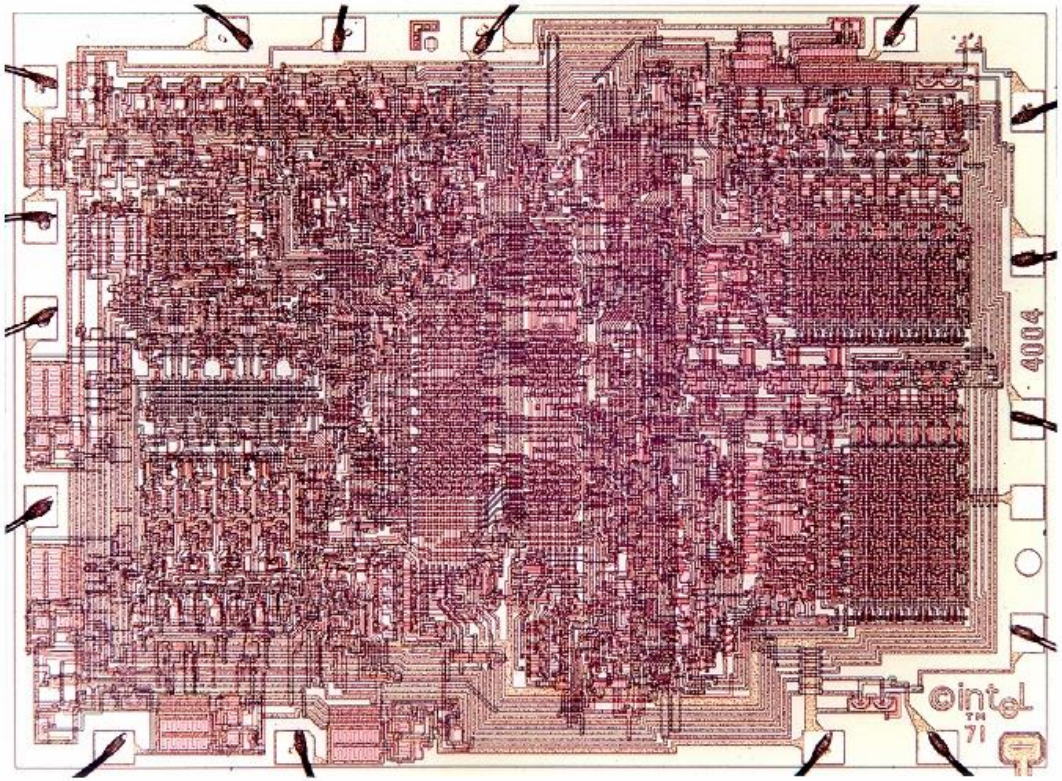


- **Electronics, Apr. 19, 1965**

Gordon Moore (co-founder of Intel) made a prediction that semiconductor technology will double its effectiveness every 18 months



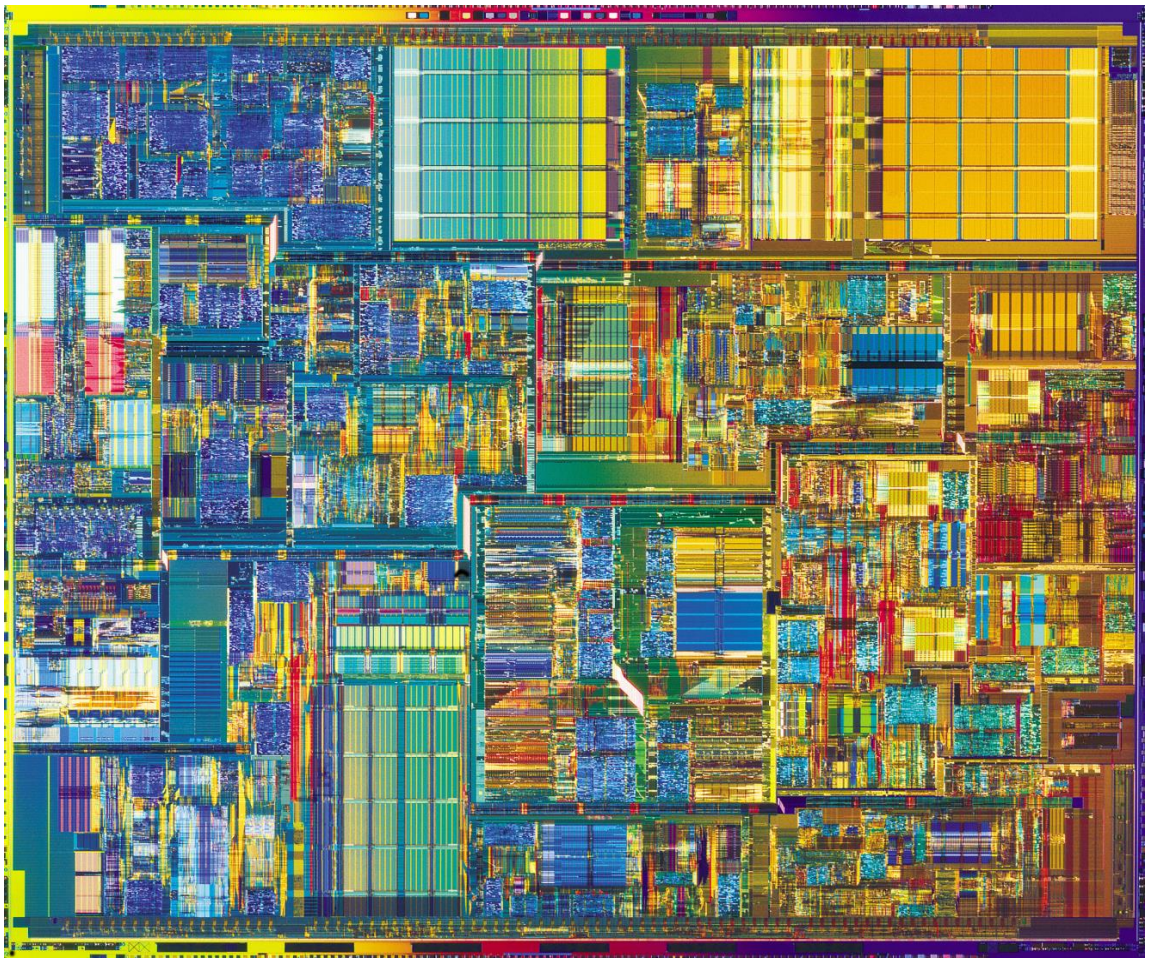
Intel 4004:1972



- First micro-processor on a single chip
- 2 300 transistors
- 0.3 mm x 0.4 mm
- 4 bit words
- Clock: 0.108 MHz

You will have the possibility to design a more powerful processor in one of our courses

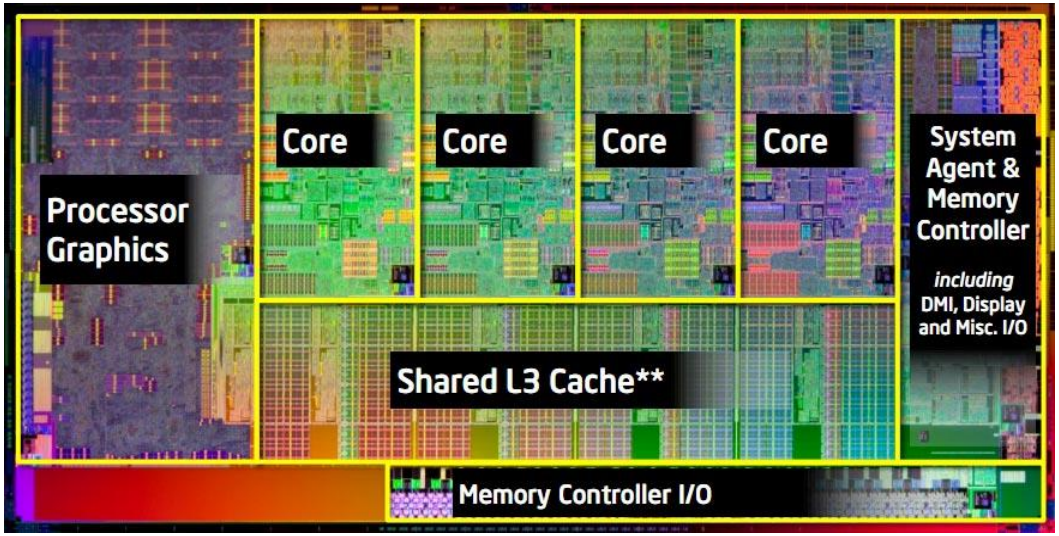
Intel Pentium 4 (2000)



- 42 000 000 transistors
- 0.18 micron CMOS
- Clock: 1.5 GHz
- Die: 20 mm^2

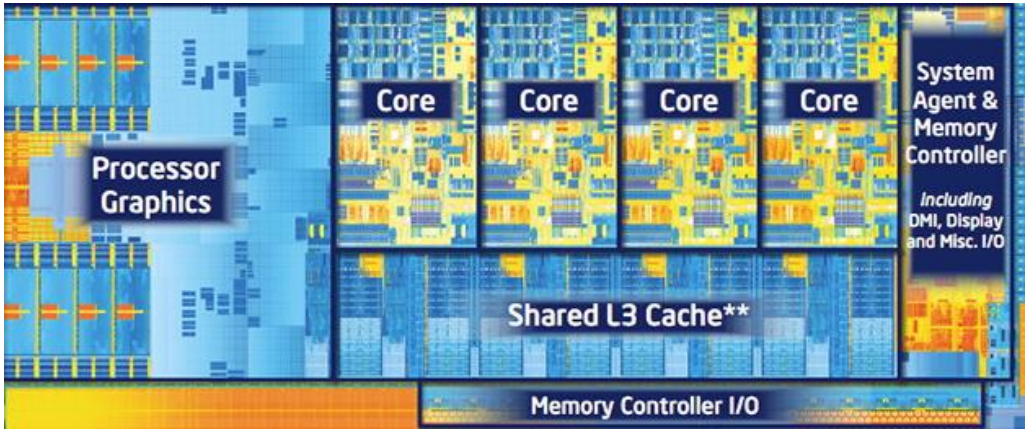
Baseband ASIC of a modern mobile phone has easily 10 times more transistors.

SandyBridge (2009)



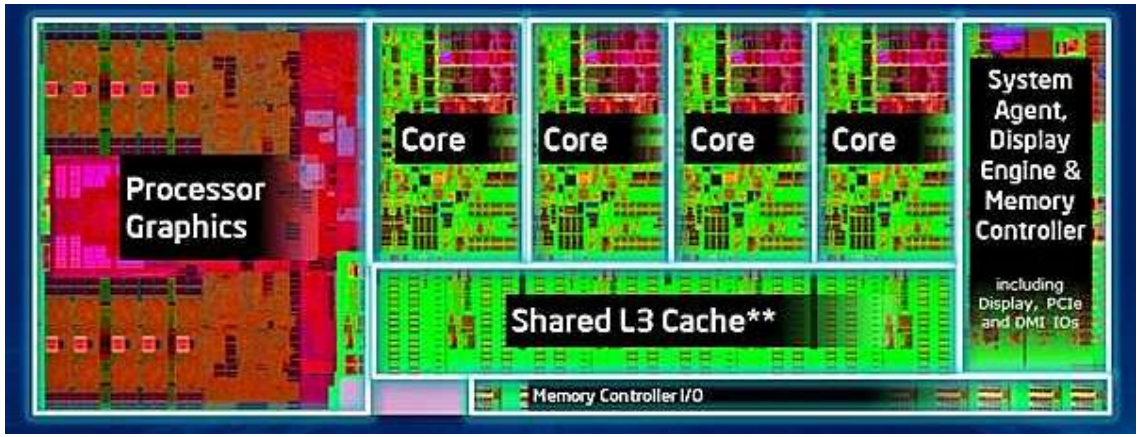
- 32 nm-64 bit
- 995 000 000 Transistors (23 × P4)
- ~3.5 GHz
- 216 mm²

IvyBridge (2011)

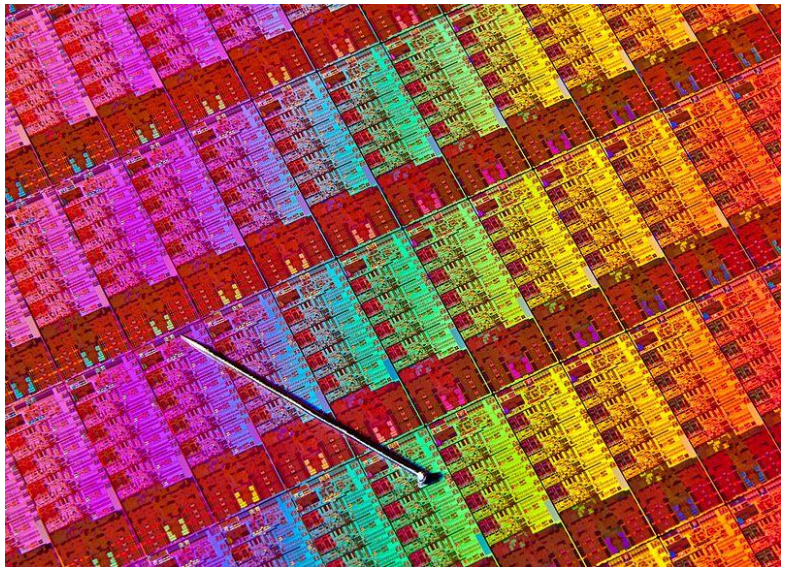


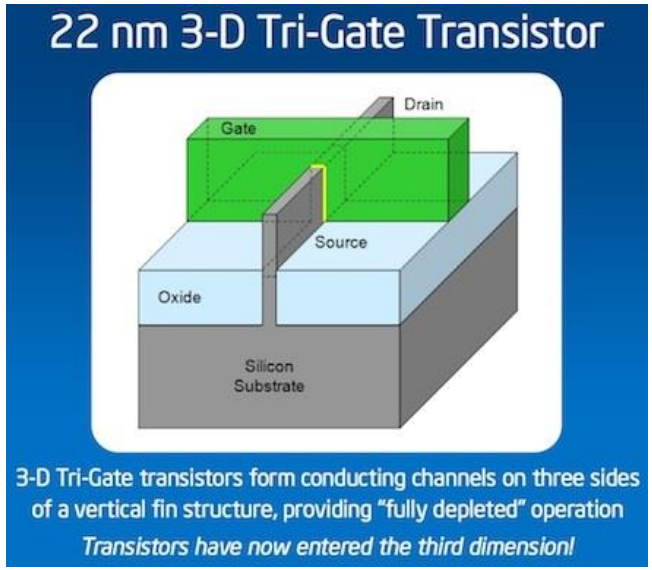
- 22 nm-64 bit
- 1 400 000 000 Transistors
- ~3.5 GHz
- 160 mm²

Haswell (2013)

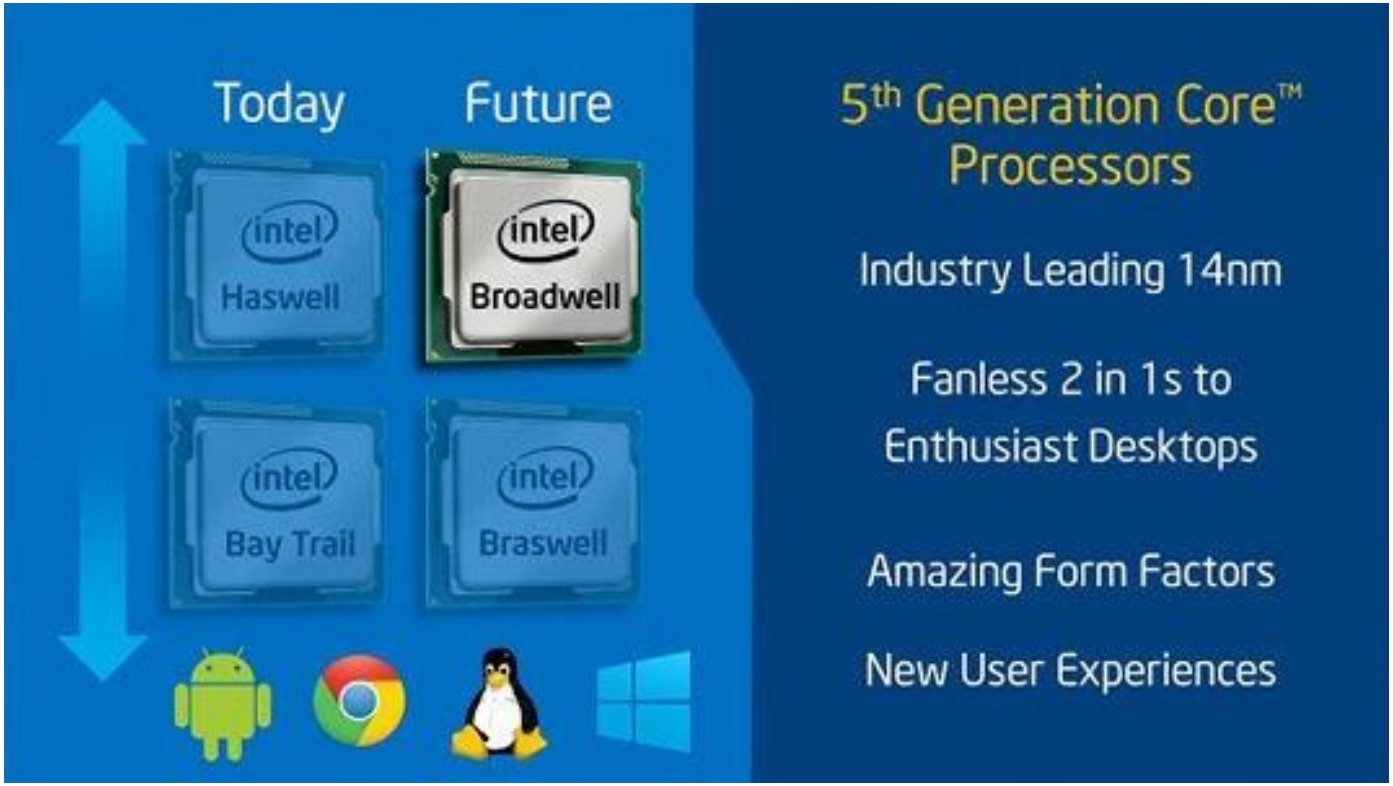


- 22 nm
- Tri-gate 3D transistor
- 1.4b Transistors
- ~3.5 GHz
- 177 mm^2

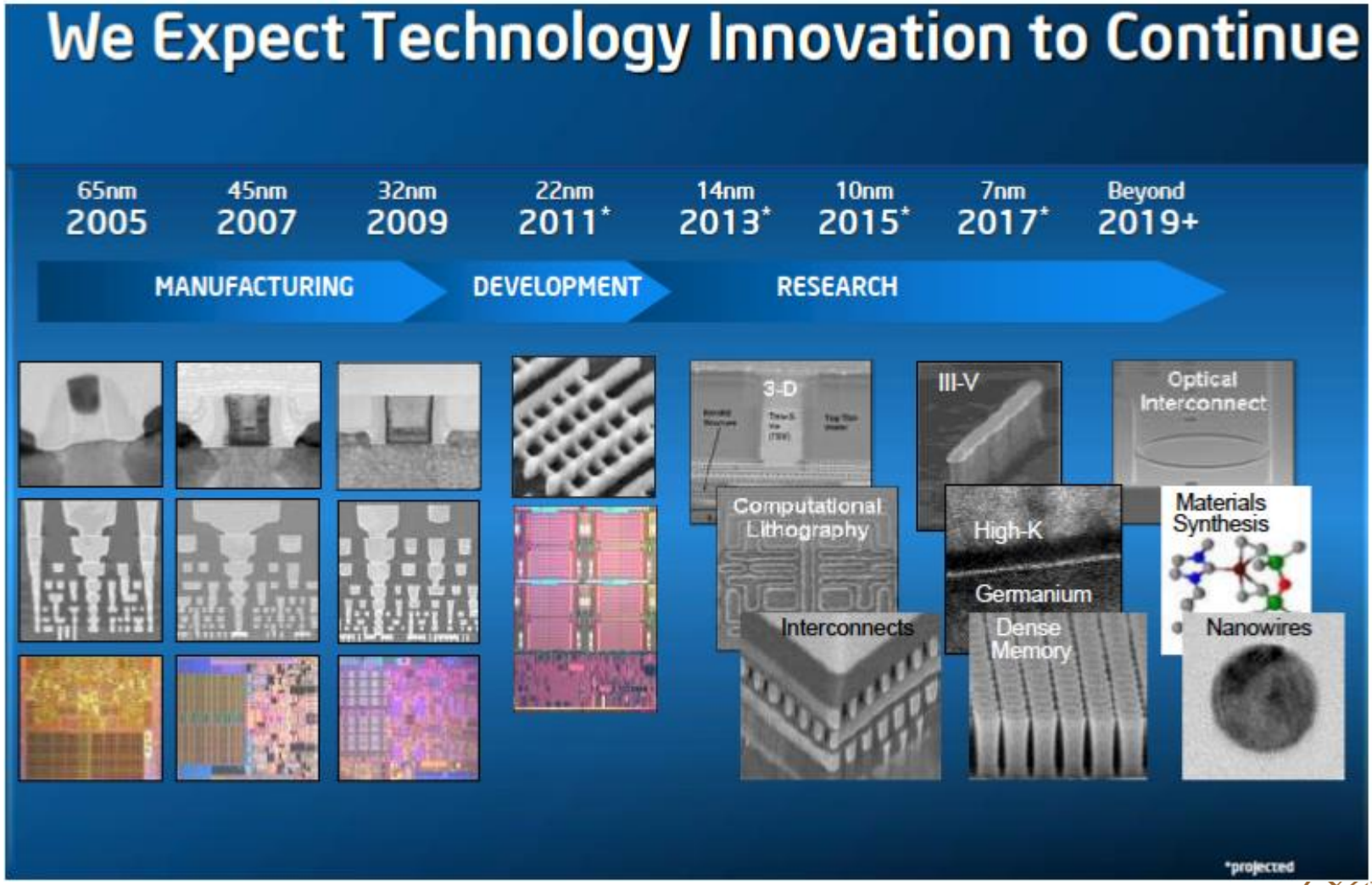




Braswell (coming 2015)

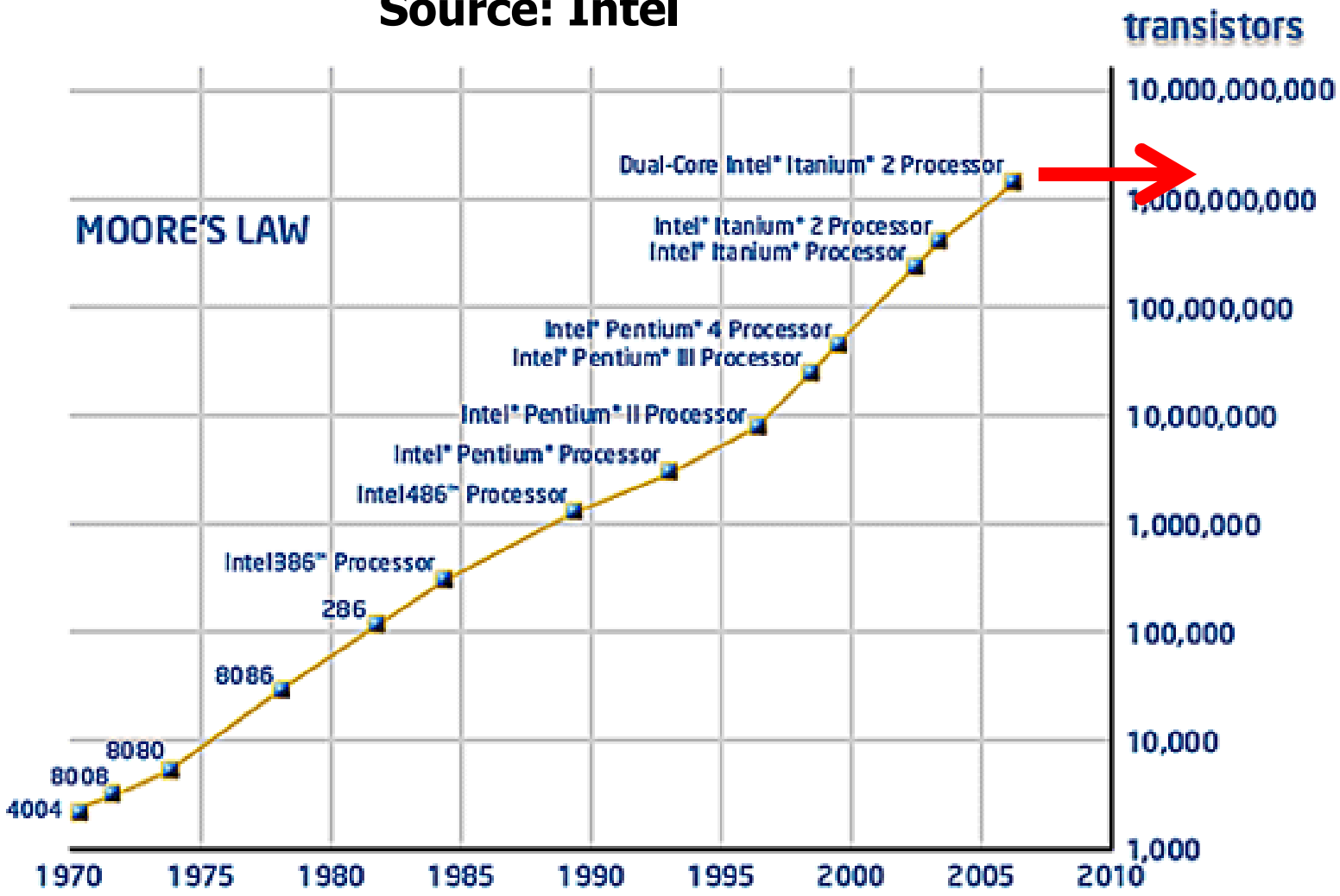


On-Time 2 Year Cycles



Moore's Law: number of transistors

Source: Intel

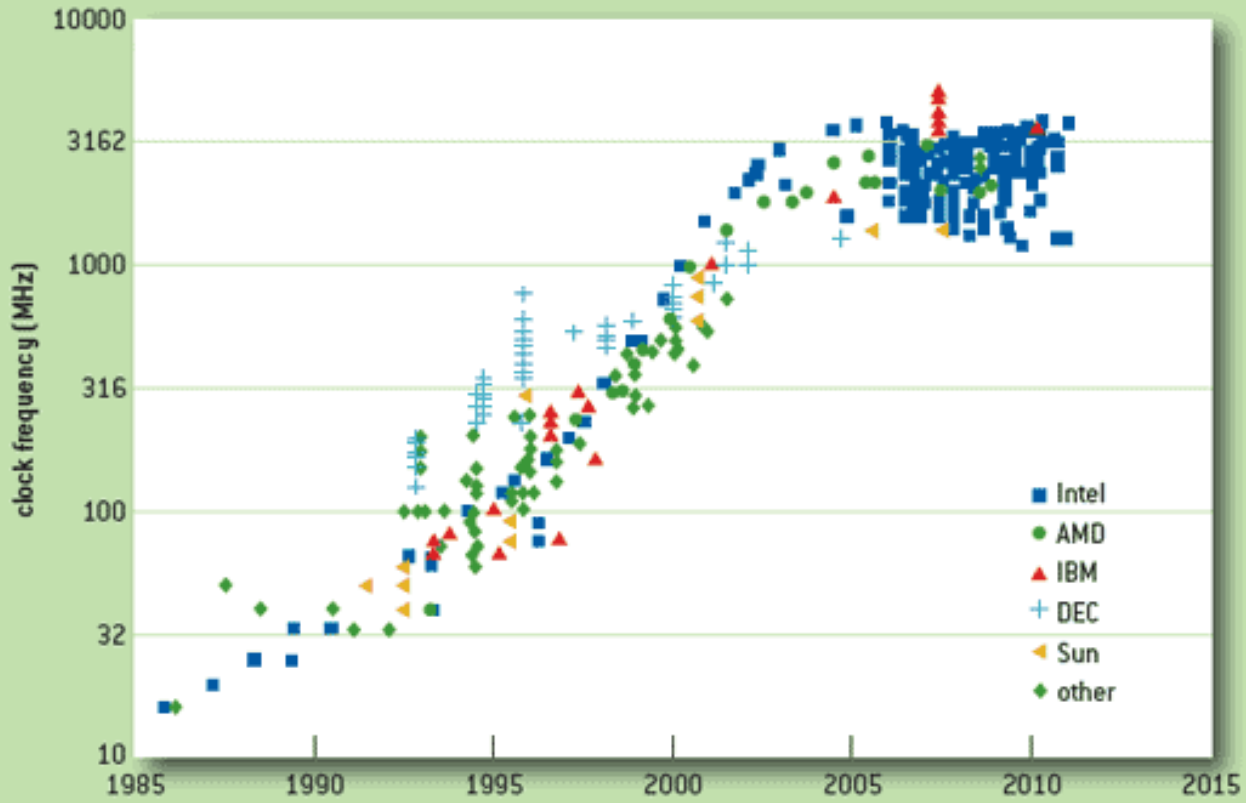


Moore's Law: frequency

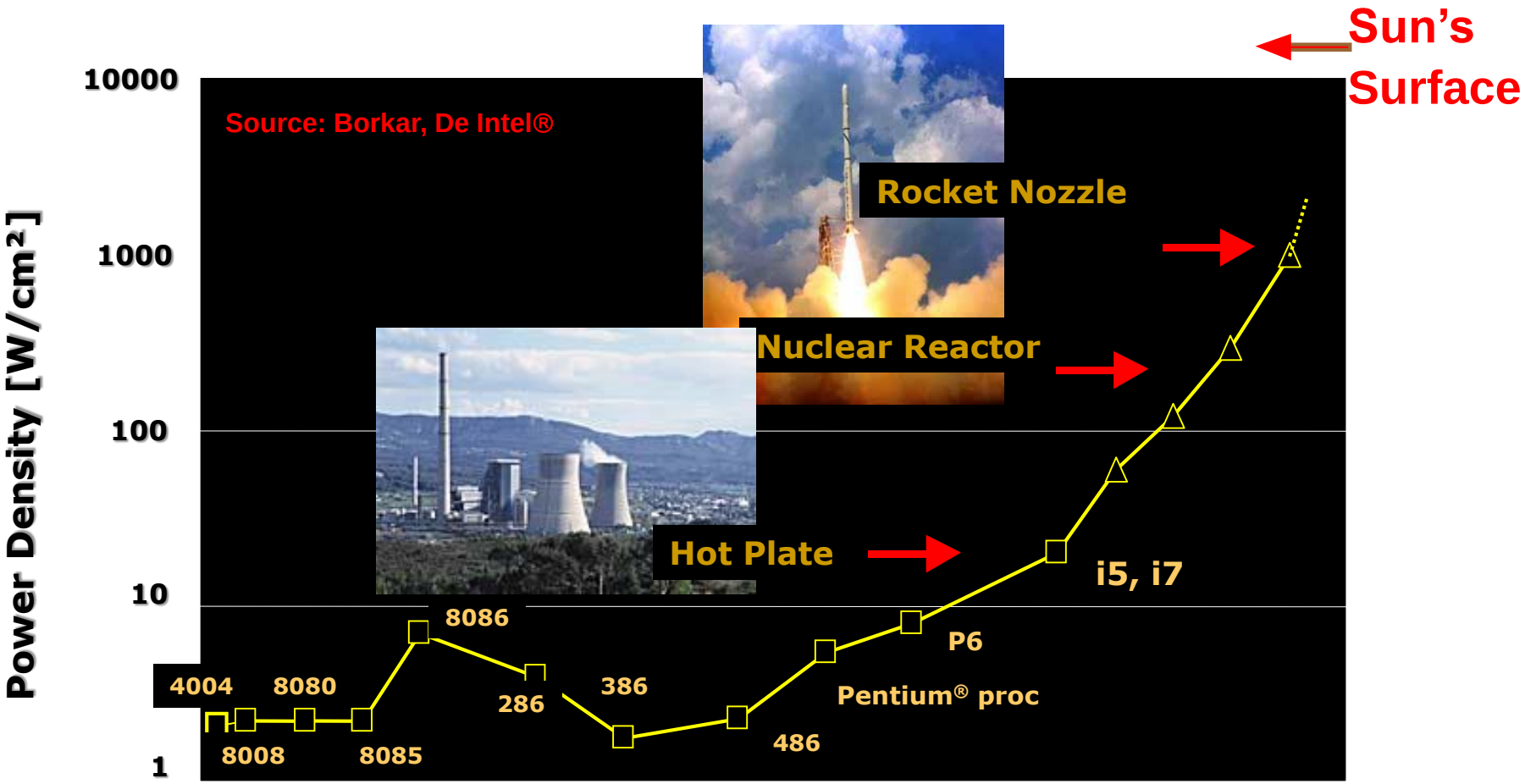
FIGURE 7

Source: CPU DB: Recording Microprocessor History

Processor Frequency Scaling Over Time



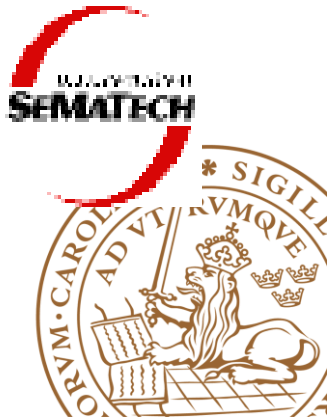
Moore's Law: power density



ITRS: The International Technology Roadmap for Semiconductors

- Published every two years (current 2013)
- Wide range: material, fabs, equipment, EDA, design, testing, modeling, simulation……
- Closely followed by industry: Not an empty prediction, but an actual planning

http://public.itrs.net/



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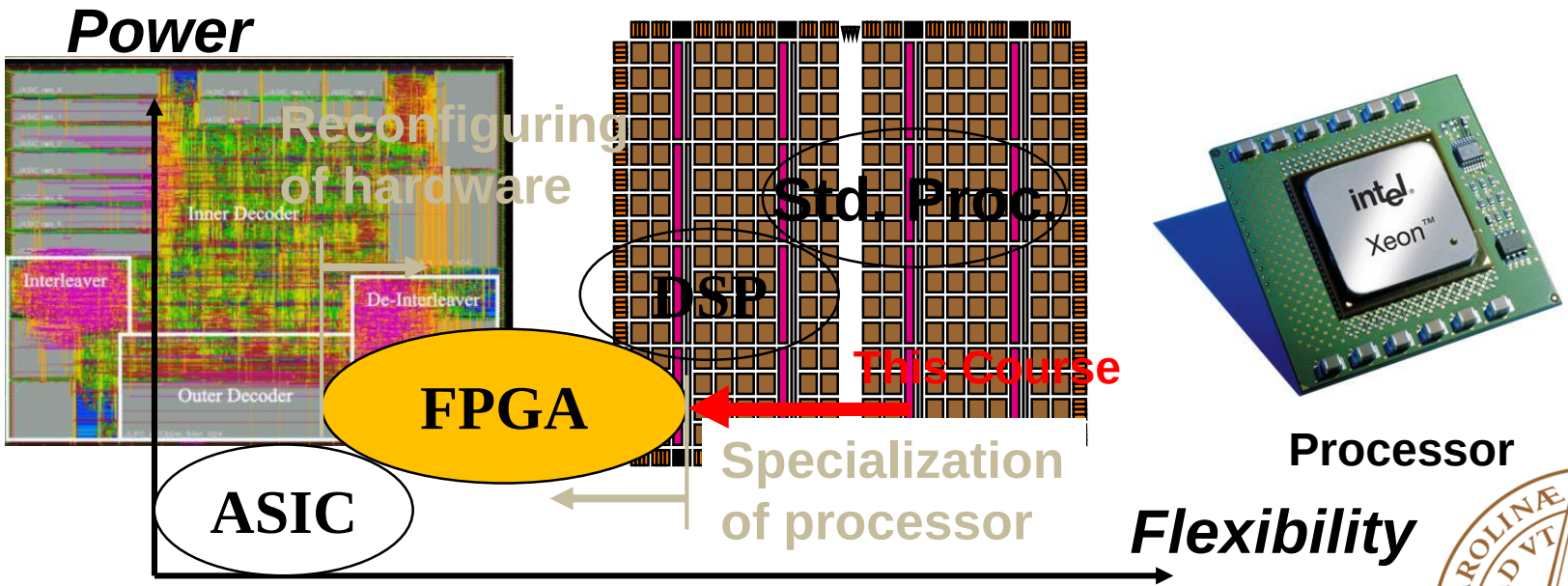
- System Representation
- Design Flow
- RTL Basics

Devices

- **General-purpose integrated circuits**
  - Microprocessors, digital signal processors, ***FPGA*** and memories
- **Application-specific integrated circuits (ASIC)**
  - Designed for a narrow range of applications
  - Full-custom ASIC
  - ***Standard-cell ASIC***



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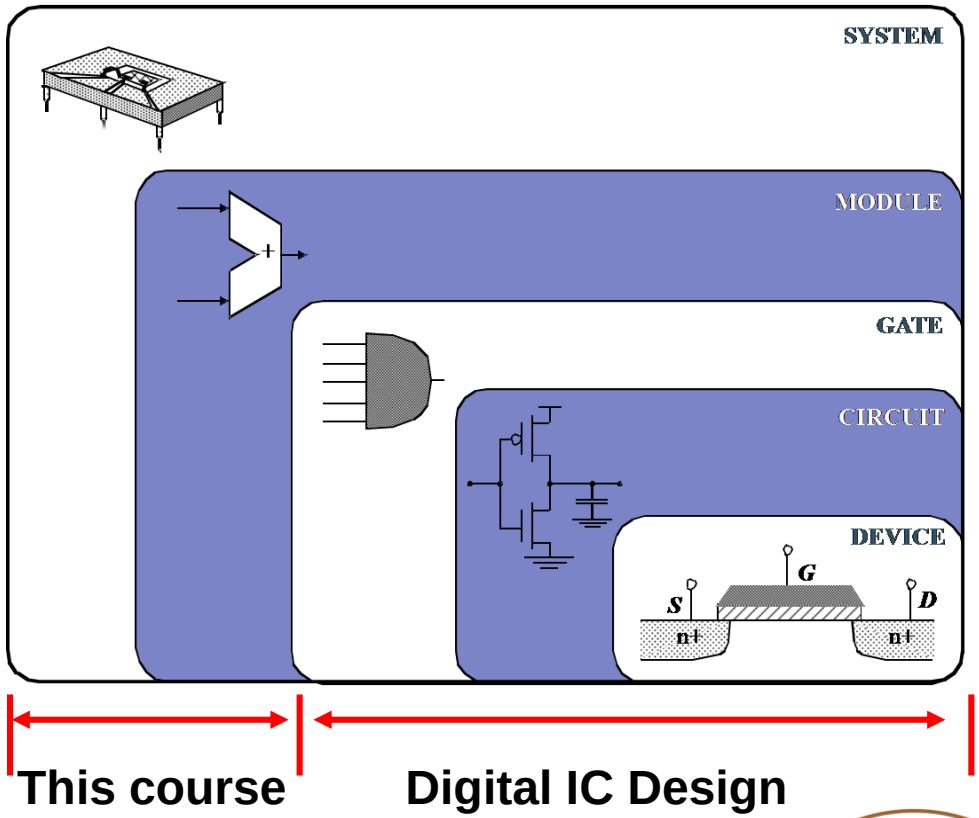
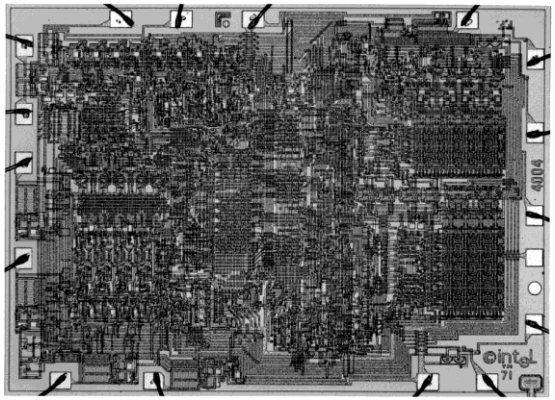
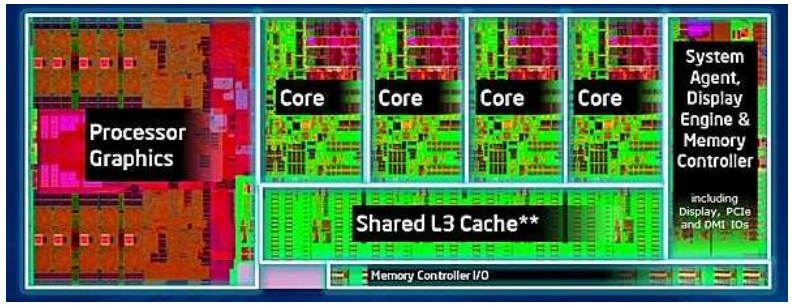
System Representation

- System
  - SoC: a CPU chip …
- Module
  - Macro cell in a chip : ALU…
- Gate
  - Basic logic block : xor, nor…
- Circuit
  - Transistors
- Device
  - Gate, source, drain



View a Design in a Proper Way





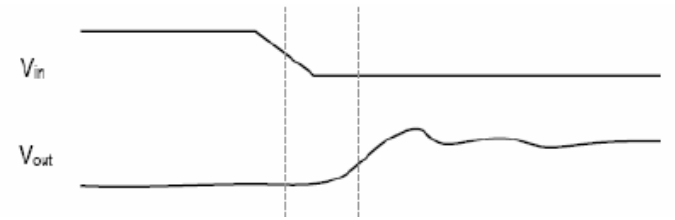
Intel 4004 (2.3K transistors)

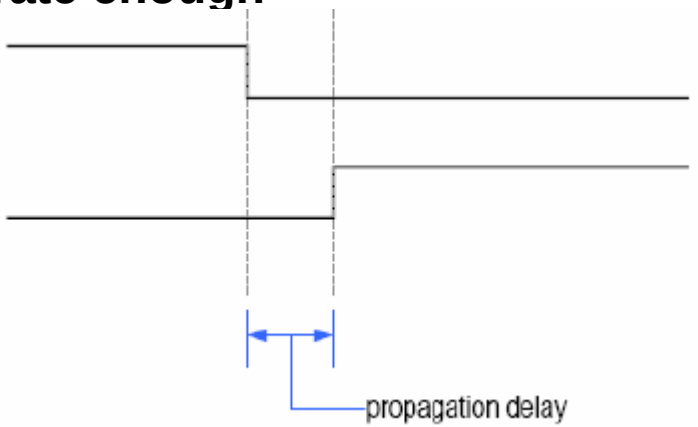
Full-custom

Intel Haswell (1.4B transistors)

?

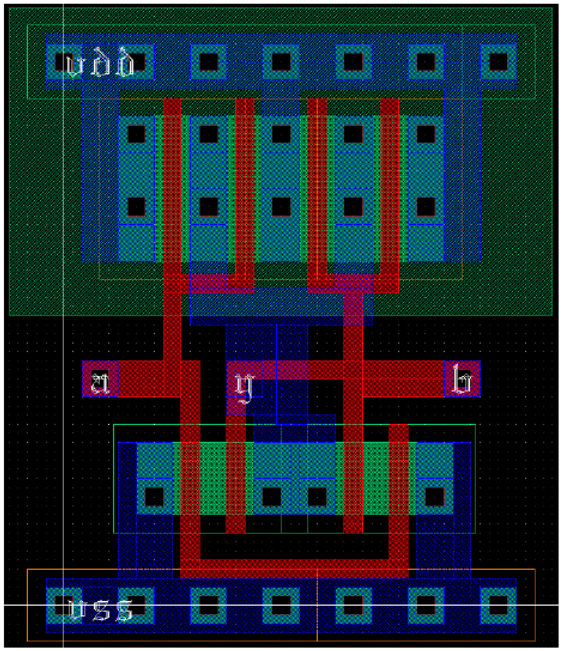
- **Abstraction: simplified model of a system**
  - **Show the selected features accurate enough**
  - **Ignore the others**





VLSI Design Flow

- **Evolution of circuit design**
  - Full-custom⇒Design-automation
    - ***Based on library cells and IPs***
    - ***Top-down methodology***
  - Design abstraction⇒“Black box” or “Model”
    - ***Parameter simplification***
    - ***Accurate enough to meet the requirement***




```
module HS65_GH_NAND2AX14 (Z, A, B);
   output Z;
   input A,B;
   not    U1 (INTERNAL1, B) ;
   or   #1 U2 (Z, A, INTERNAL1) ;
   specify
     (A +=> Z) = (0.1,0.1);
     (B -=> Z) = (0.1,0.1);
   endspecify
endmodule // HS65_GH_NAND2AX14
```

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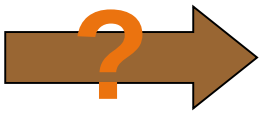
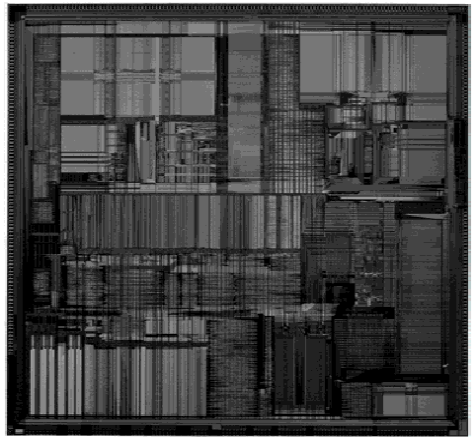
VLSI Design

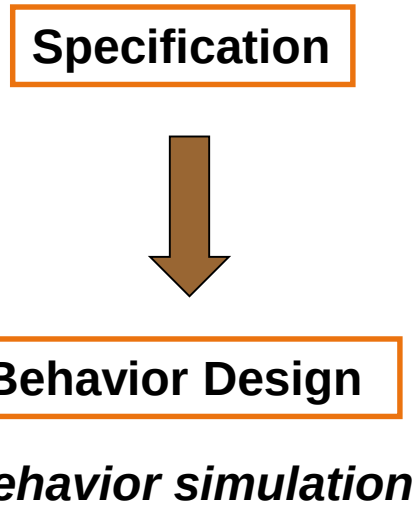
- **Set of specification:**
  - What does the chip do?
  - How fast does it run?
  - How reliable will it be?
  - How is the silicon area?
  - How much power will it consume?
  - ……





VLSI Design Flow

- An iterative process that transfer the specification to a manufacturable chip through at least five levels of design abstraction.



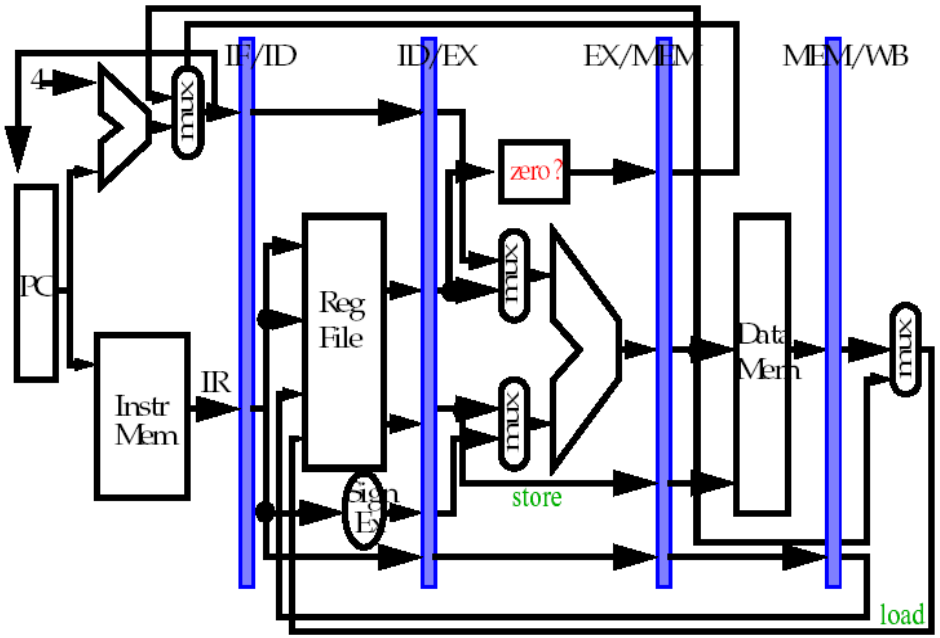
Function, performance, definition: English

Behavior, algorithm: C/C++, SystemC, Matlab …

VHDL
Verilog

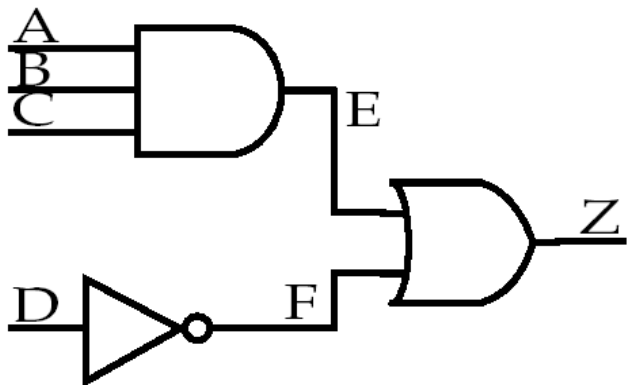
Register Transfer Level Design

RTL simulation



Synthesis

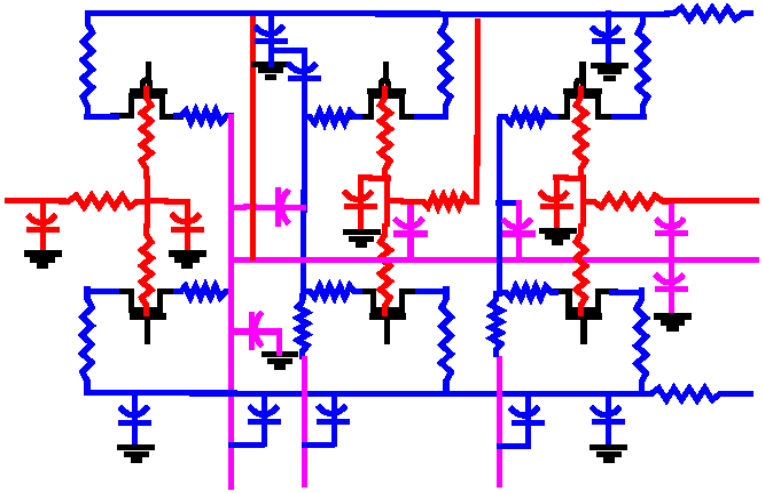
Logic Design



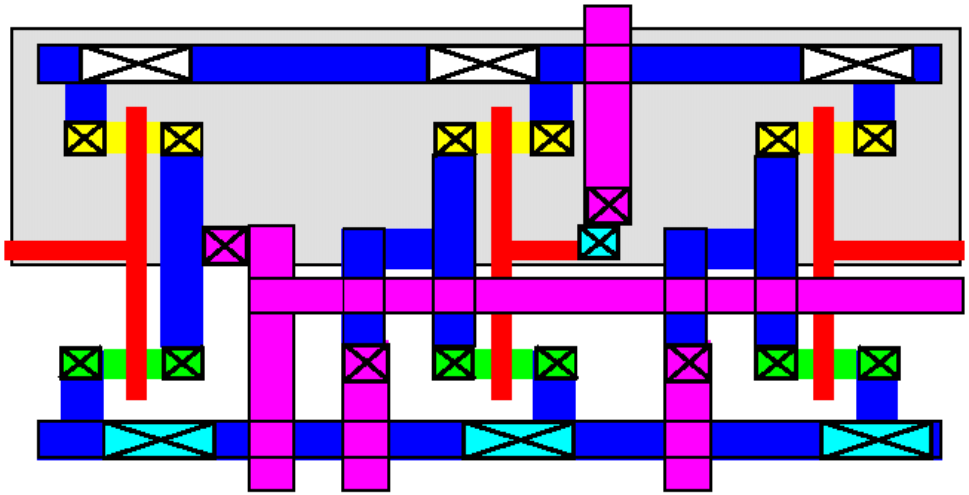
Gate-level simulation
Timing analysis
Power analysis

Custom Design

Circuit Design



Layout



Physical Design

Design rule checking
Post layout simulation

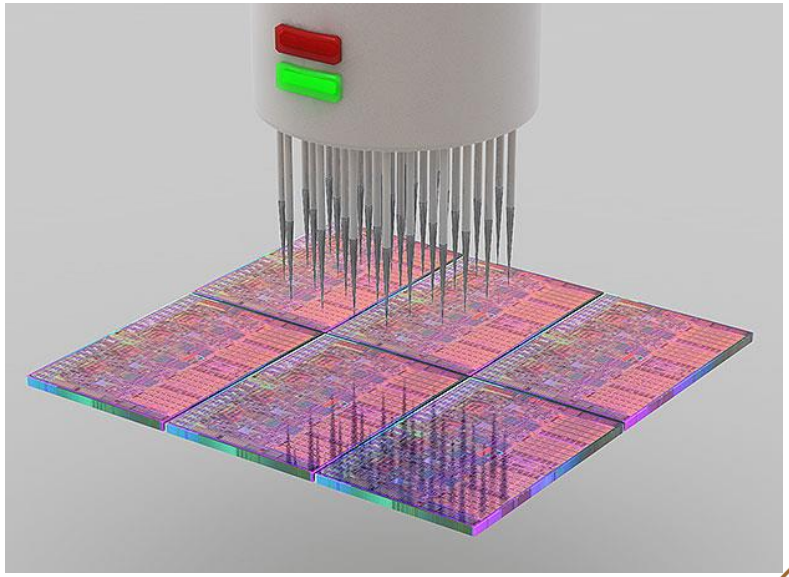
Verification

- **Verification**
  - Check whether a design meets the specification and performance goals
  - Concern the correctness of the initial design and the refinement
- **Two aspects**
  - ***Functionality***
  - ***Performance (timing)***
- **Method of Verification**
  - **Simulation**
    - ***Spot check: cannot verify the absence of errors***
    - ***Can be computation intensive***
  - **Timing analysis**
    - ***Just check delay***
  - Formal verification
    - ***Apply formal math techniques determine its property***
    - ***E.g, equivalence checking***
  - **Hardware emulation**

Fabrication

Testing

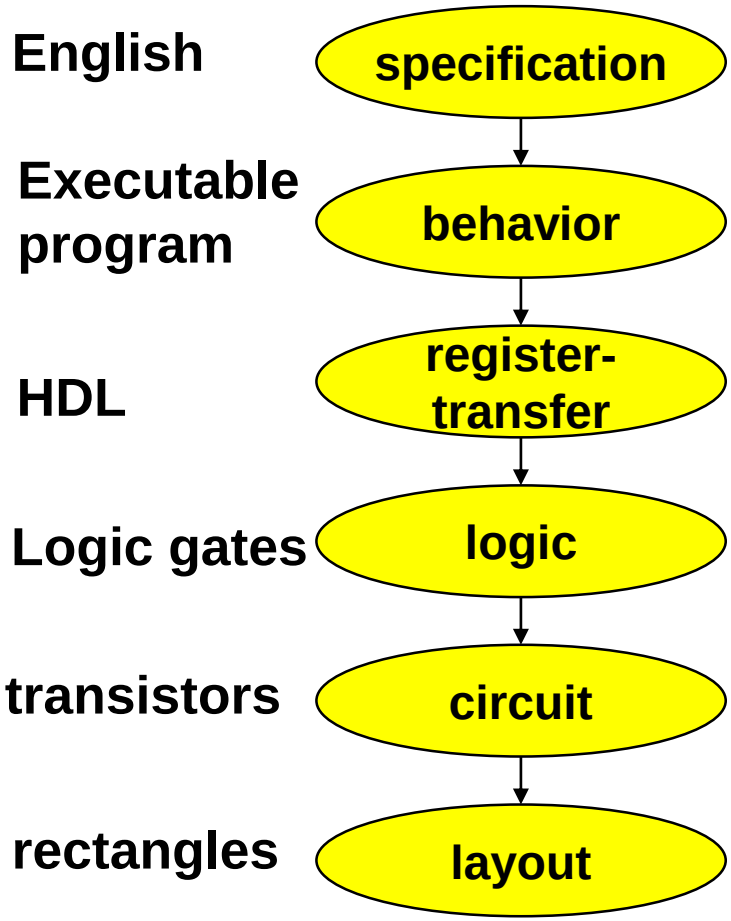
- **Testing is the process of detecting physical defects of a die or a package occurred at the time of manufacturing**
- **Testing and verification are different tasks.**
- **Difficult for large circuit**
  - Need to add auxiliary testing circuit in design
  - E.g., built-in self test (BIST), scan chain etc.



VLSI Design Flow: Tools

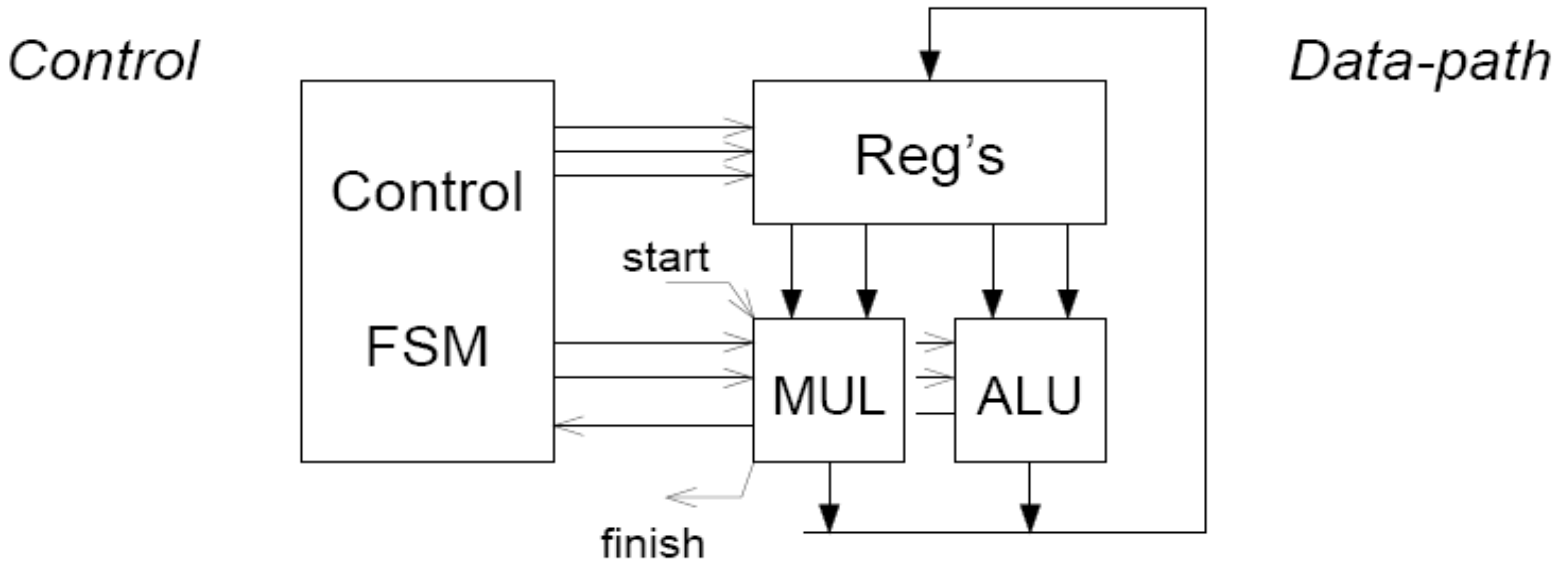
- **Algorithm**
  - **Matlab**
- **RTL Simulation**
  - ***Modelsim, Mentor***
  - VCS, Synopsys
  - VerilogXL, Cadence
- **Logic Synthesis**
  - **Design Compiler, Synopsys**
  - Blast Create, Magma
- **Transistor Simulation**
  - Hspice/Starsim, Synopsys
  - Spectra, Cadence
  - Eldo, Mentor
- **Mixed-Signal Simulation**
  - **AMS Designer, Cadence**
  - ADMS, Mentor
  - Saber, Synopsys
- **Place & Route**
  - Astro, Synopsys
  - **Silicon Encounter, Cadence**
  - Blast Fusion, Magma
- **Layout**
  - **Icfb/Dracula, Cadence**
  - ICstation/Calibre, Mentor
- **FPGA**
  - ***ISE, Xilinx***
  - Quatus, Altera

VLSI Design Flow: Summary



Following slides should fresh up your memory

Overall VLSI Structure

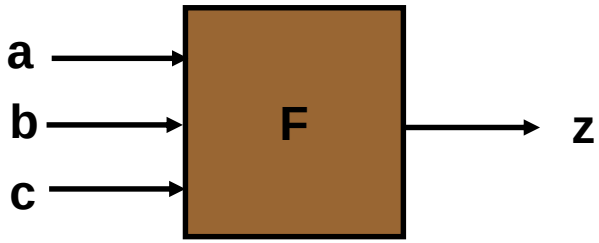


- **Scheduling / ordering / sequencing of operations**
- **Mapping / allocation:**
  - Variables -> {Reg1, ... ,RegN}
  - Operations -> {MUL, ADD, ALU, ... ,}

We will implement something similar in this course

Two Basic Digital Components

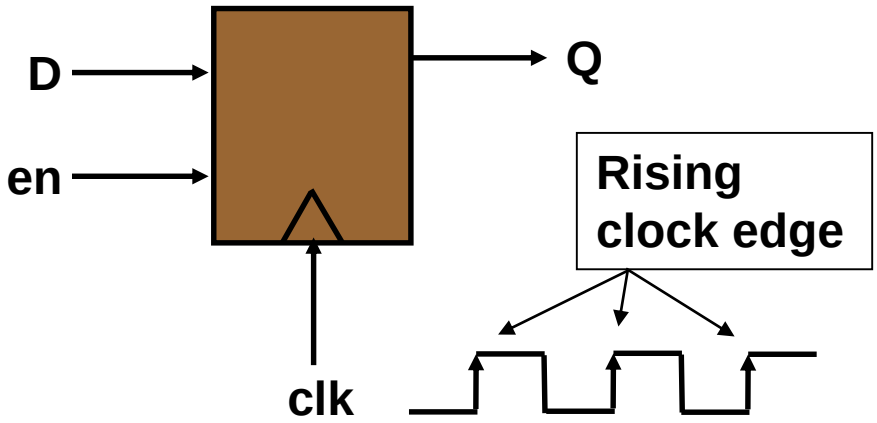
Combinational Logic



Always:
z <= F(a, b, c);

i.e. a function that is always evaluated when an input changes. Can be expressed by a truth table.

Register



if clk'event and clk='1' then
if en='1' then
Q <= D;

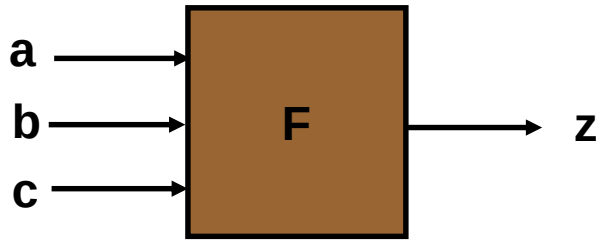
i.e. a stored variable, Edge triggered D Flip-Flop with enable.

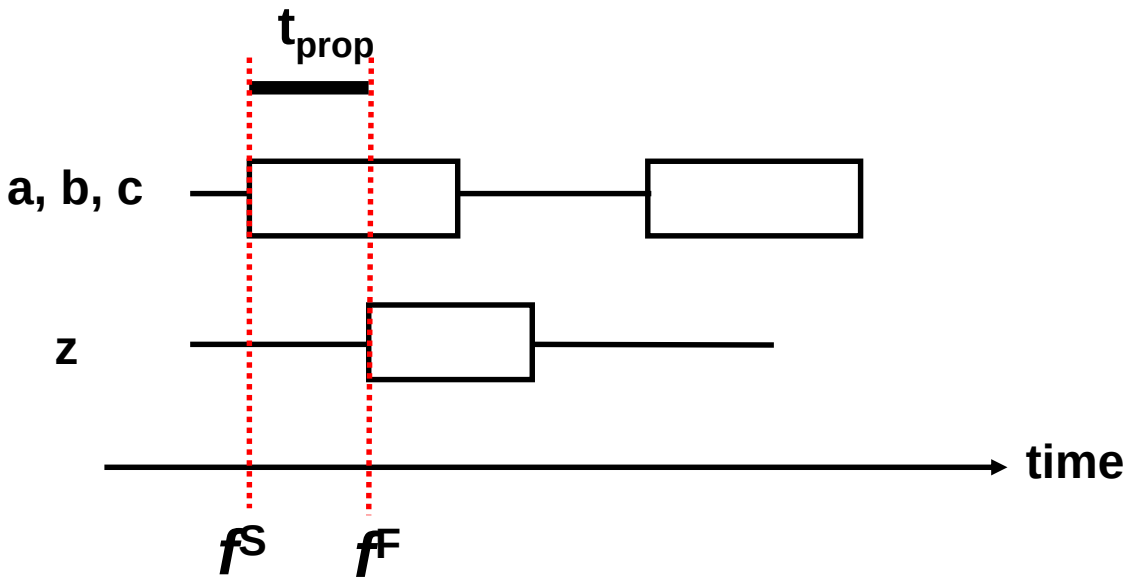
Timing

Only if we guarantee to meet the timing requirements

... do the components guarantee to behave as intended.

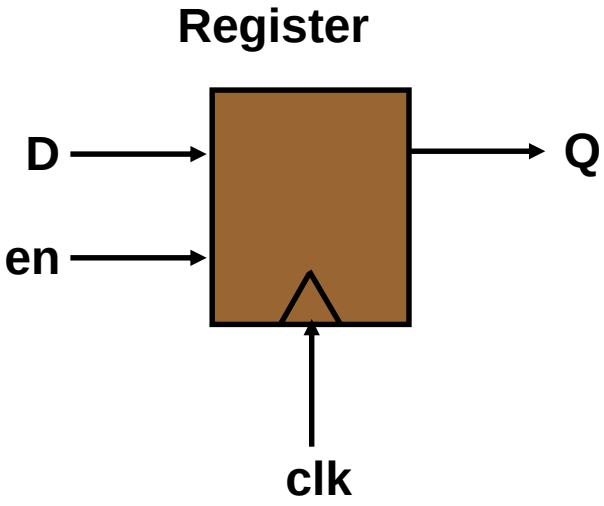
Combinational Logic Timing

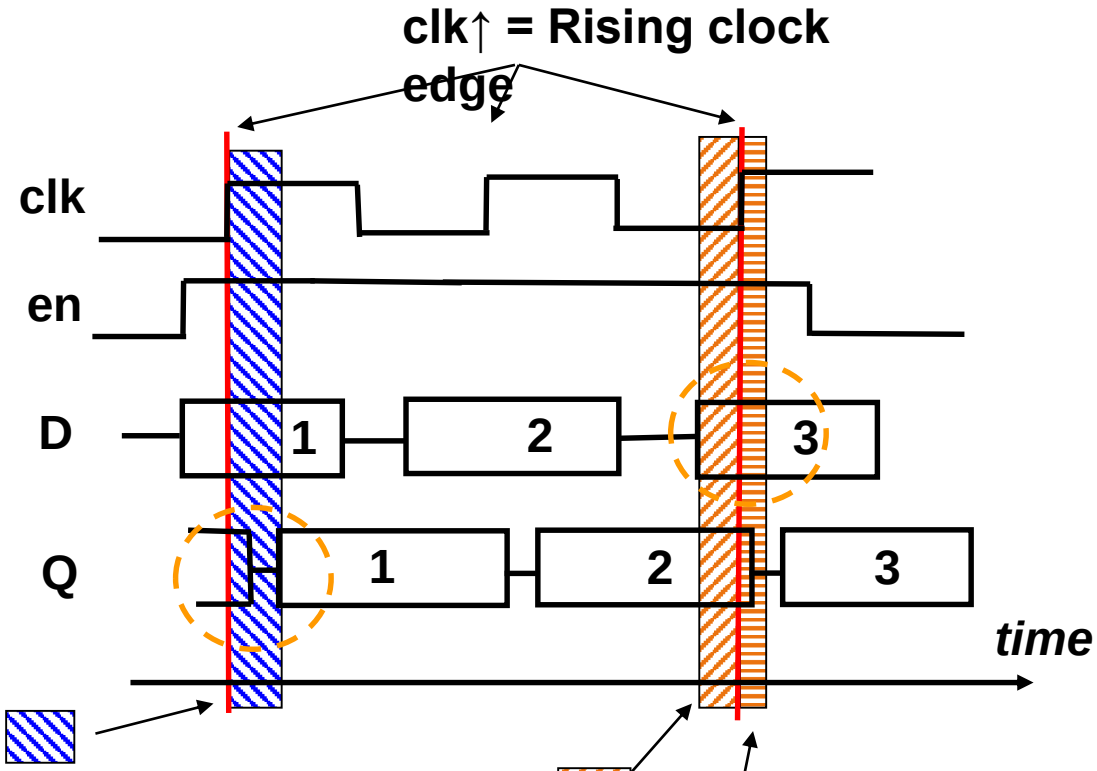




- **Propagation delay:**
  After presenting new inputs
  Worst case delay before producing correct output

Register timing





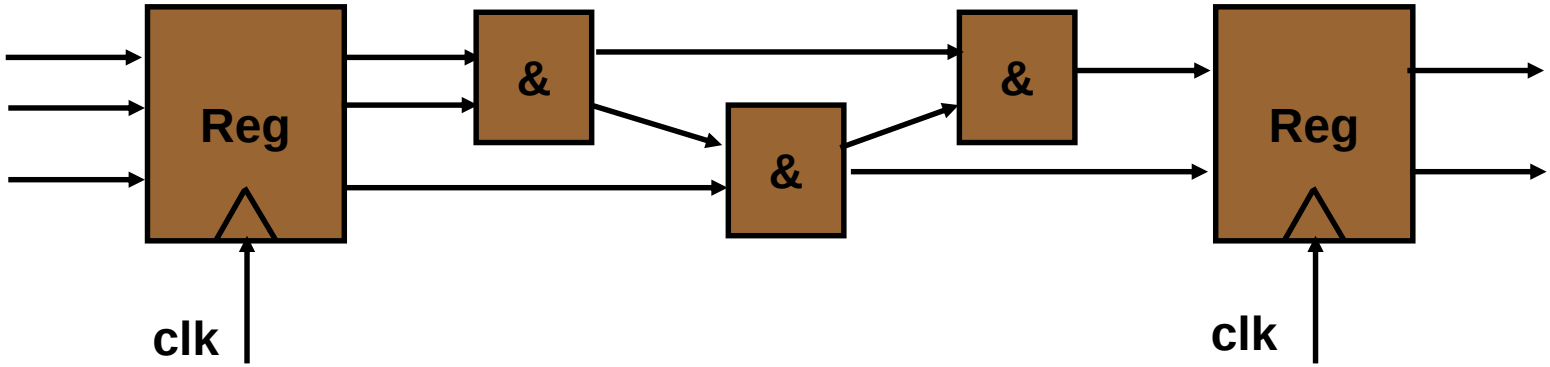
Propagation delay (clk_to_Q):
Worst case (maximum) delay after clk↑ before new output data is valid on Q.

Setup time:
Minimum time input must be stable before clk↑

Hold time:
Minimum time input must be stable after clk↑

Clock Frequency

- What is the maximum clock frequency?



Register

Propagation delay:	Tckl-Q	250ps
Setup time:	Tsu	200ps
Hold time:	Th	100ps

AND-gate

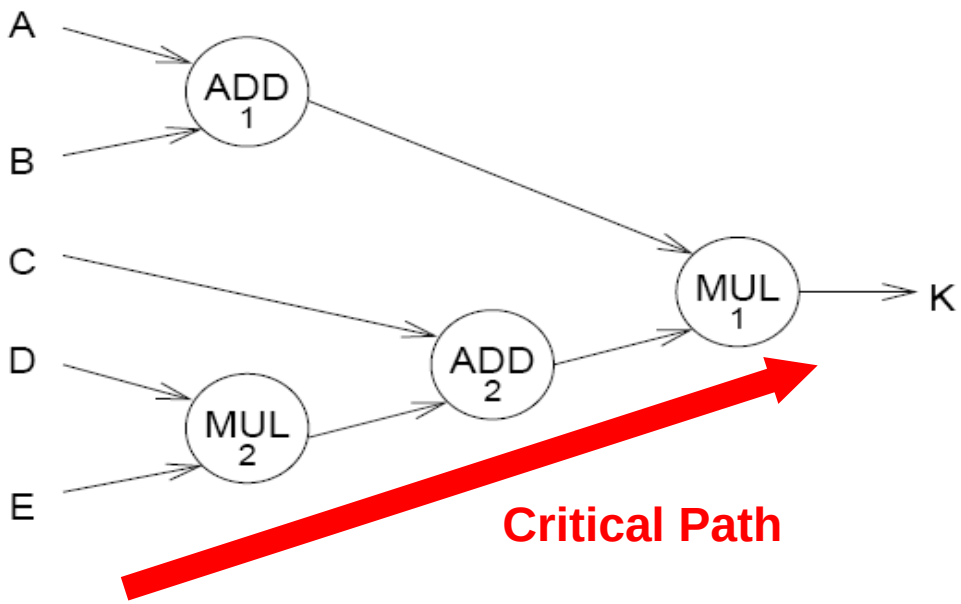
Propagation delay:	Tprop	250ps

250+250*3+200=1.2ns

f=833MHz

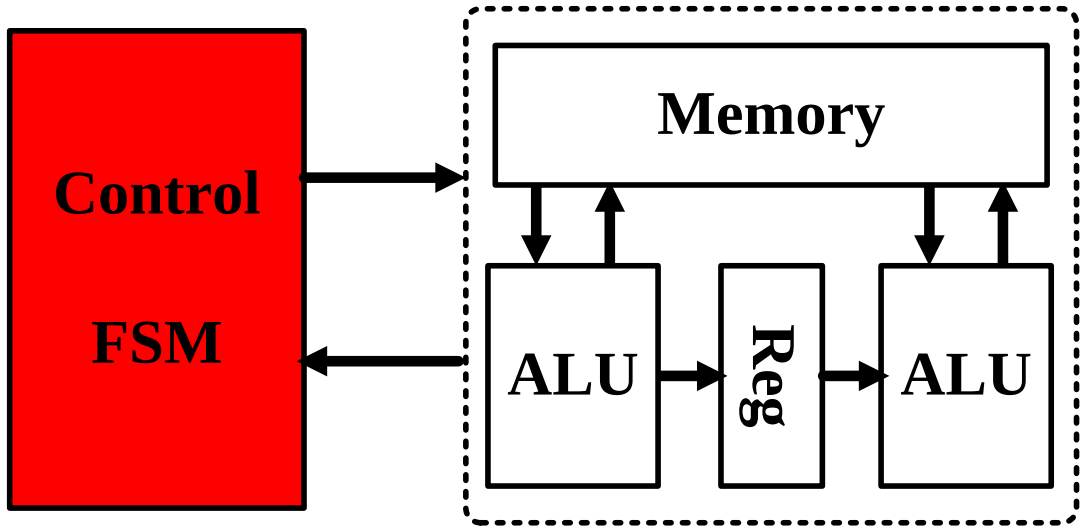
Critical path

- …begin to explore the construction of digital systems with complex behavior
  - Example: K = (A $+_1$ B) $*_1$ (C $+_2$ D $*_2$ E)
- Combinational circuit:



Tomorrow

- 08:00-10:00 in E:C
- The controller: Finite State Machine
- VHDL Basics
- Assignment 1



Thanks