EITF35: Introduction to Structured VLSI Design

Part1.1.1: Course Introduction

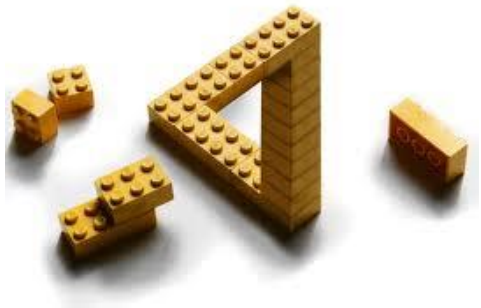
Liang Liu
liang.liu@eit.lth.se

Course Factor

- **Introduction to Structured VLSI (very large scale integration) Design (7.5HP)**

http://www.eit.lth.se/index.php?ciuid=774&L=1

Digital IC



This Course

Course is a pre-requisite for ETIN35- IC-project 1, digital

Outline

- Course Objective
- Teachers
- Lectures and Labs
- Language, Tools, Device
- Assignments
- Examination
- Continuation

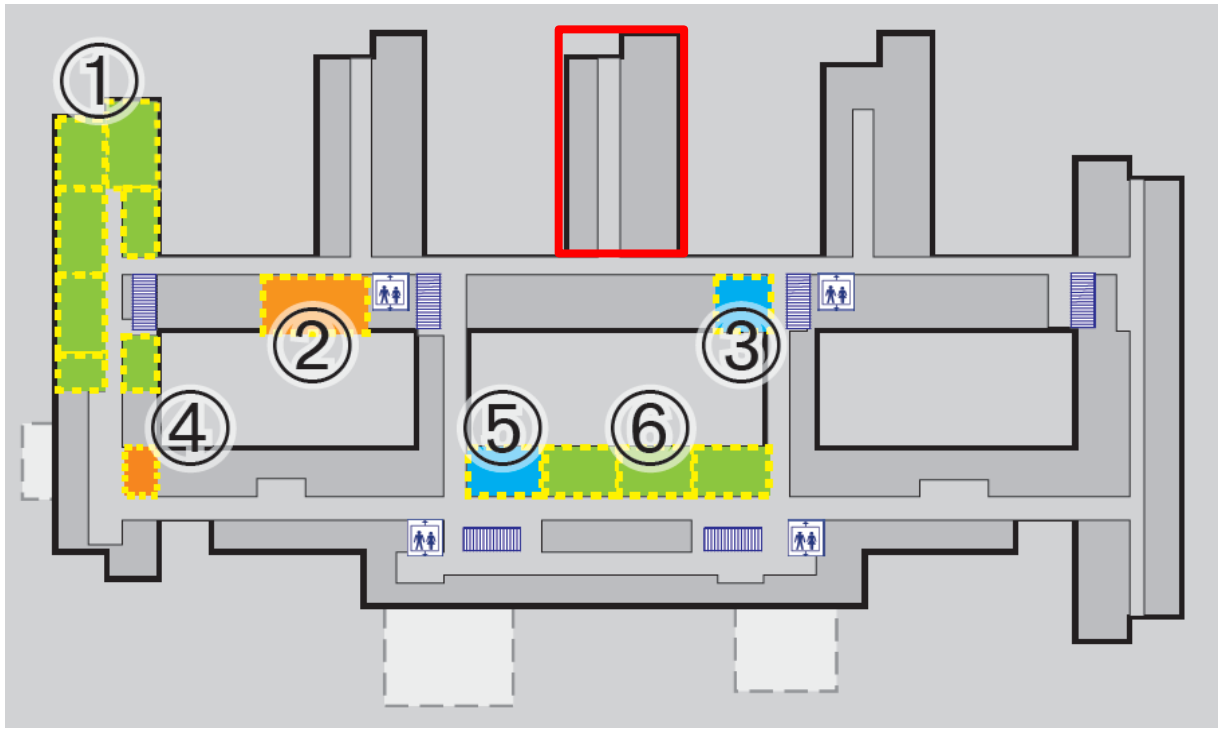
Course Objective

- **To introduce the basic concept and knowledge on digital VLSI realization**
  - Typical function blocks of a large digital system, state machines, datapaths, storage elements
  - Optimization techniques for area, speed, and power
- **To provide the basic VHDL knowledge, design flow and tool training**
- **To provide real-life digital VLSI design experience**
  - Fast prototyping several assignments and projects on commercial FPGA platform

Teachers

Lecture

- Liang Liu, Assistant Professor
- Email: liang.liu@eit.lth.se
- Room: E2342
- Homepage: http://www.eit.lth.se/staff/Liang.Liu



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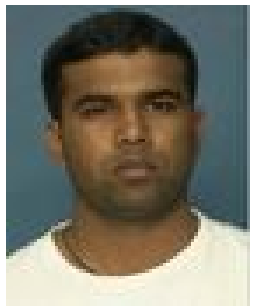
Teaching Assistants

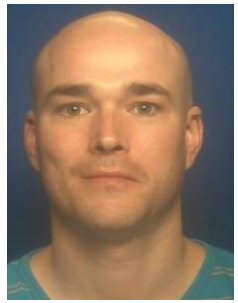
- Rakesh Gangarajaiah
- Oskar Andersson
- Hemanth Prabhu
- Steffen Malkowsky



Rakesh Gangarajaiah

Oskar Andersson

Hemanth Prabhu



Steffen Malkowsky

Guest Lecturers

Guest Lecturers from EIT

- Erik Larsson, Associate Professor
- Joachim Rodrigues, Associate Professor

Invited Lecturers from Industry

ERICSSON

AXIS COMMUNICATIONS

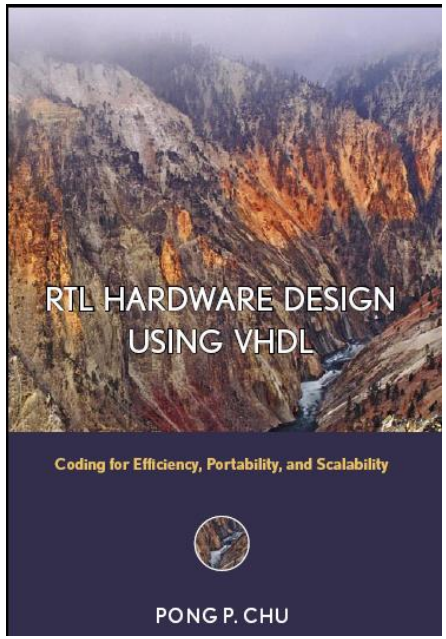
Book Recommendation

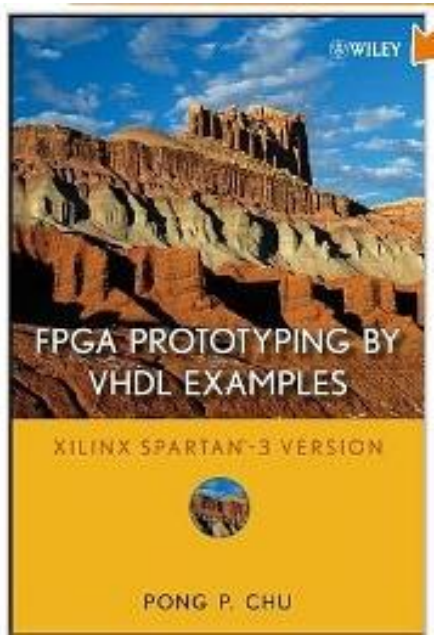
RTL Hardware Design Using VHDL

- Coding for Efficiency, Portability, and Scalability
- Pong P. CHU

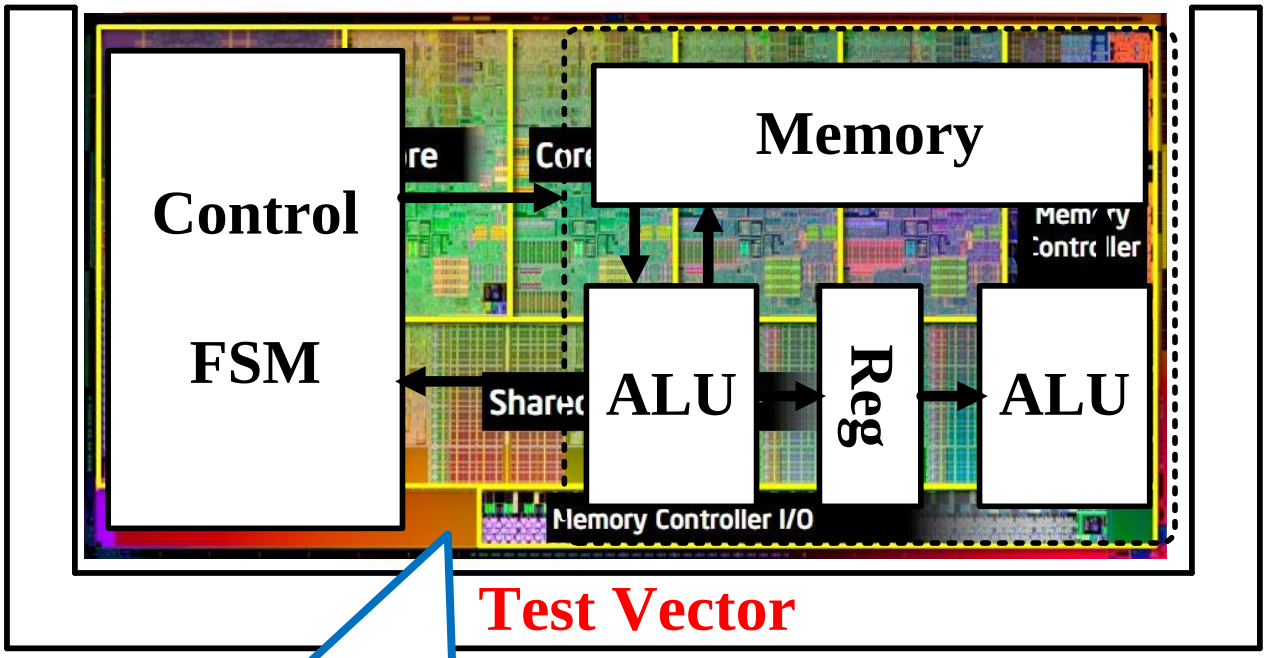
FPGA Prototyping by VHDL Examples

- Xilinx Spartan-3 Version
- Pong P. CHU





Course Content & Schedule



- Concept &Theory
- VHDL Knowledge
- Assignment & Project

- Overview
- Controller
  - FSM
- Data-Path
  - Combinational circuit
  - Sequential circuits
  - Storage elements
- Test & Verification
- FPGA
- Design Optimization

Lectures and Labs

- **Lectures (10)**
  - **Monday: 10:00-12:00 in E:2311**
  - **Tuesday: 08:00-10:00 in E:C**

  In the 1st Week a lecture on FPGA and ISE will be given for Friday at 08:00 (E:C)
- **Labs E:4121** **Group A** **Group B**
  - **Tuesday** **13:00-15:00, 15:00-17:00**
  - **Wednesday** **08:00-10:00, 10:00-12:00 (13:00-15:00, 15:00-17:00 from Week 39)**
  - **Tursday** **13:00-15:00, 15:00-17:00**
  - **Friday** **13:00-15:00, 15:00-17:00 (approval)**
  - **Will present the assignments before the lab**
  - **Each group will have 3 lab slots with TA's per week**
  - **Drop-in with TA support Wednesday 15:15-17:00**
- **Labs are accessible 24/7 if not occupied by other courses**
- **You need to sign up for the lab before you can get access to the 4th floor.**

Language, Tools, Device

Language

- VHDL will be used to develop the circuits

Tools

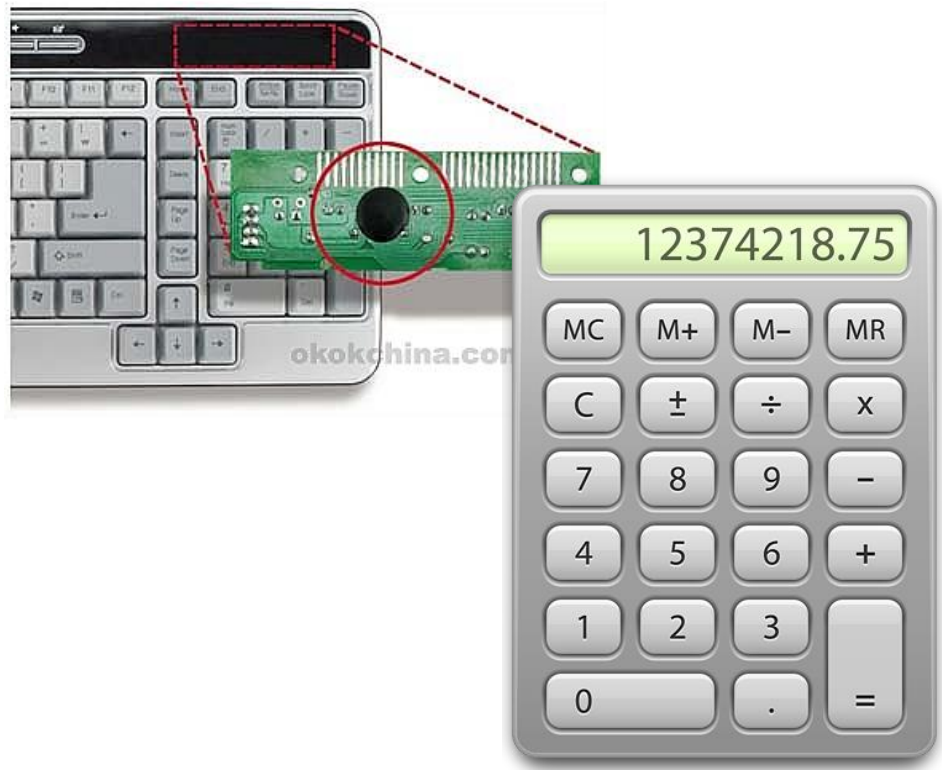
- Modelsim (QuestaSim): VHDL simulator
- ISE Design Suite (v14.6)

Device

- XILINX Spartan 3

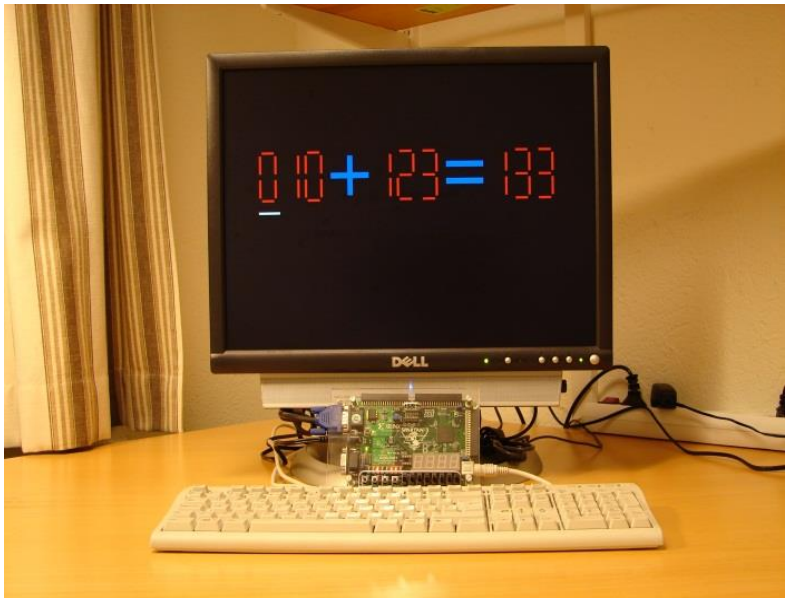
Assignments

- **To pass the course, 3 assignments need to get approved**
  - Sequence Detector
    - ***Simulation***
  - Keyboard Controller
    - ***FPGA implementation***
  - Alrithmetic Logic Unit (ALU)
    - ***FPGA implementation***



- **Assignments approved in time will result in grade 3**

Assignments cont'd



- **Extra projects are required to get grade 4 /5**
  - FPGA implementation
    - ***ALU with input memory***
    - ***ALU output on VGA***
  - Squre-root funtion in the ALU
    - ***Optimize for area and/or speed constraint***

Examination

Before the lab

- All assignments must be prepared and handed in
- Without preparation you are not allowed to continue the lab

Examination cont'd

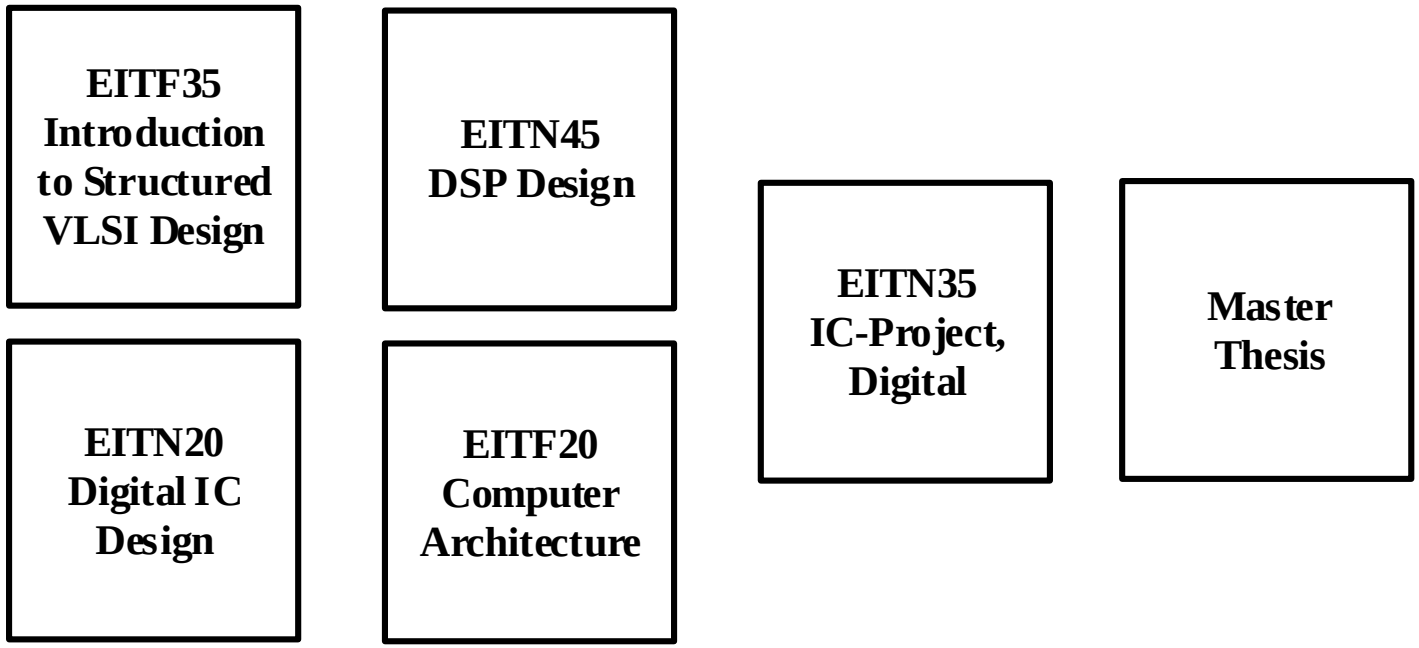
Design Approval

- **All assignments must be demonstrated to the TA's to get approved before deadline.**
- **Students need to demonstrate their understanding of the assignment to get it approved.**
  - Application of learned knowledge
  - Good VHDL coding style
  - Understanding of circuits and timing
- **Graded as a group, but individual grading may be applied if an "unbalance" is discovered.**
  - Both team members need to be present at design approval
  - Oral test might be given to both team members

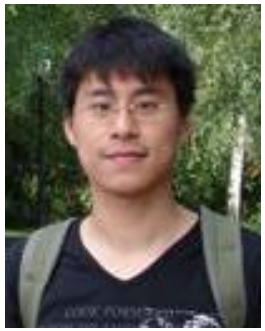
Next Step

What can we do after finishing this course?

Digital Path



Digital Path



Chenxin Zhang

Intro. VLSI (mouse control)

DSP Design IC Project Comp. Arc. (MIPS processor)

Master Thesis (multi-core MIPS)

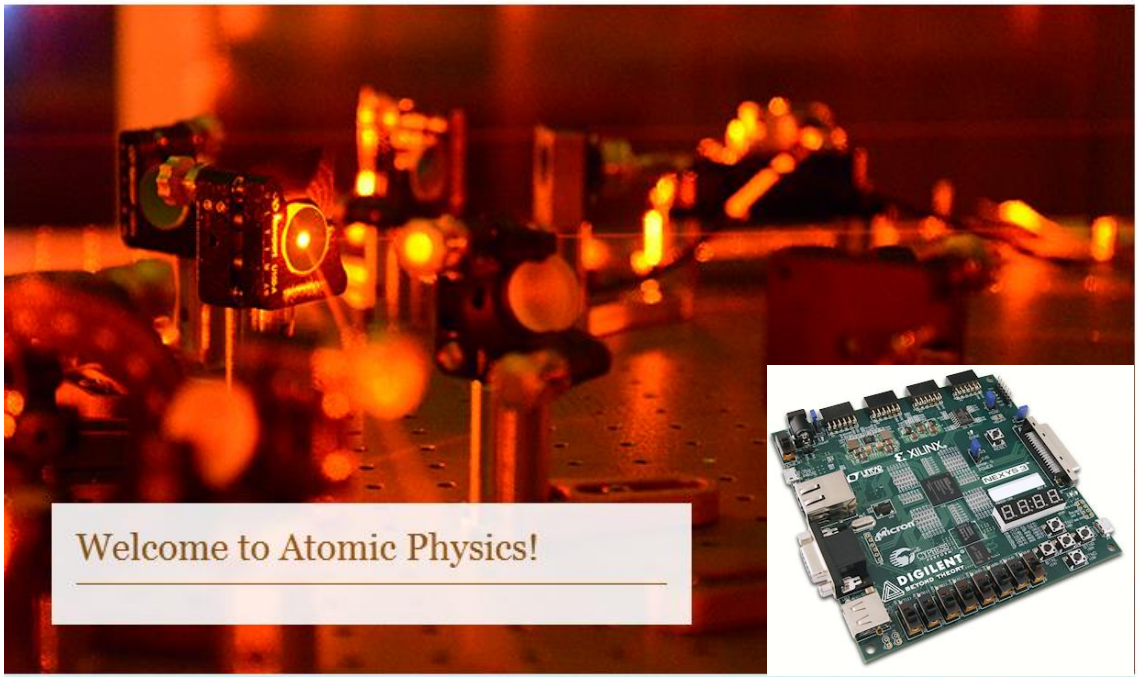
PHD (Processor for LTE-A.)

BroadCom (Processor for LTE-A.)

Projects and Thesis last year

Ultra-fast laser measurement

- **Cooperate with Anne L'Huillier (committee member, Nobel Physics Prize) in Atomic Physics**



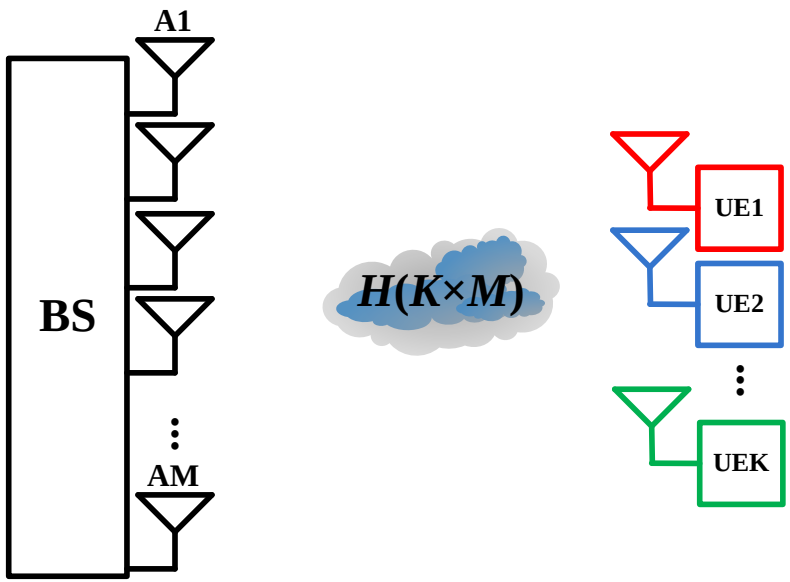
Projects and Thesis last year

- **Verification of LTE modems**
  - **Ericsson Lund**

- **Higher-level synthesis**
  - **ARM Lund**

FPGA and VHDL Support Tech. Evolution

- **World-first Massive MIMO test-bed for 5G**



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Questions?