Introduction to structured VLSI design

Design for Test (DfT) - Part 2

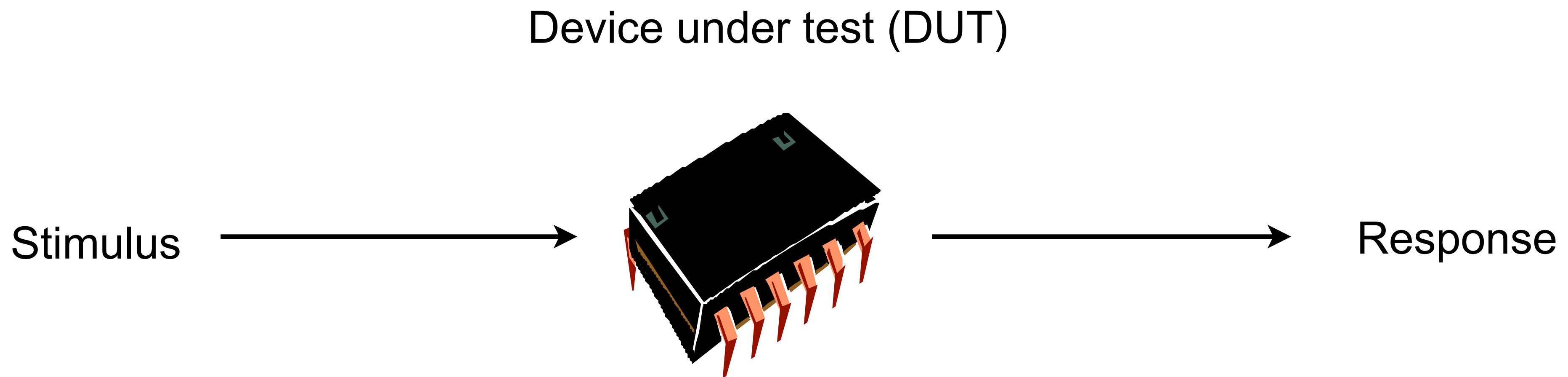
Erik Larsson

EIT, Lund University

Outline

- Electronics
- Manufacturing
- Test, diagnosis, and verification
- Test generation
- Test points and Scan
- Test Compression
- Built-In Self-Test (BIST)
- Systems-on-chip test
- Boundary scan (IEEE 1149.1)

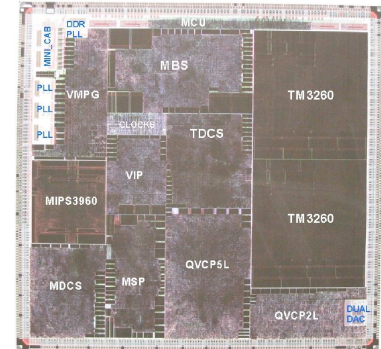
Test



Stimulus: test vectors

Test pattern: test vector + expected test response (ordered n-tuple of binary values)
Produced test response is compared against expected test response

Test application



Automatic Test Equipment (ATE)

Test stimuli (TS)
0010100
0110000

Expected responses (ER)
1011001
1101010

Compare

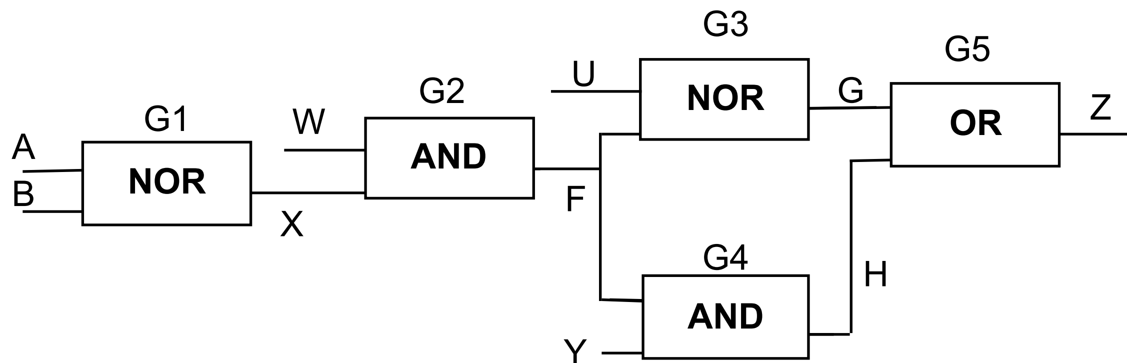
Pass/fail

Device under test

Produced responses (PR)
0111011
0100101

Stuck-at Fault (SAF) Model

- A line is fixed to logic value 0 (stuck-at-0) or 1 (stuck-at-1)
- For the stuck-at fault model there are for a circuit with n lines 2*n possible faults



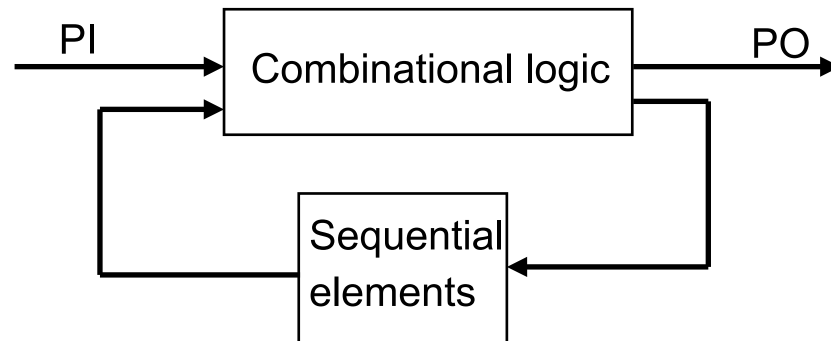
- Quality of a test is given by:
  fault coverage = faults detected / total number of faults
- Example: 12 lines (24 faults) detect 15 faults: f.c.=15/24 (63%)

Commercial ATPG Tools

- Commercial ATPG tools are often for combinational circuits
- Commercial tools usually make use of a random test generation for 60-80% of the faults (easy to detect) and deterministic test generation for the remaining part (hard to detect)
- Examples of commercial ATPG tools:
  - Encounter Test - Cadence
  - TetraMax - Synopsis
  - FastScan, FlexTest - Mentor Graphics

Test Generation for Sequential Circuits

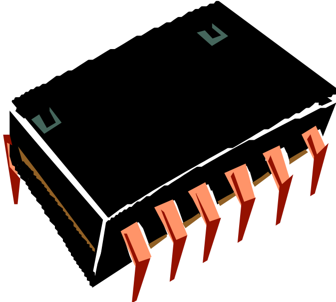
- Most real circuits are sequential
- A major problem is that the output depends not only on inputs but also on current state

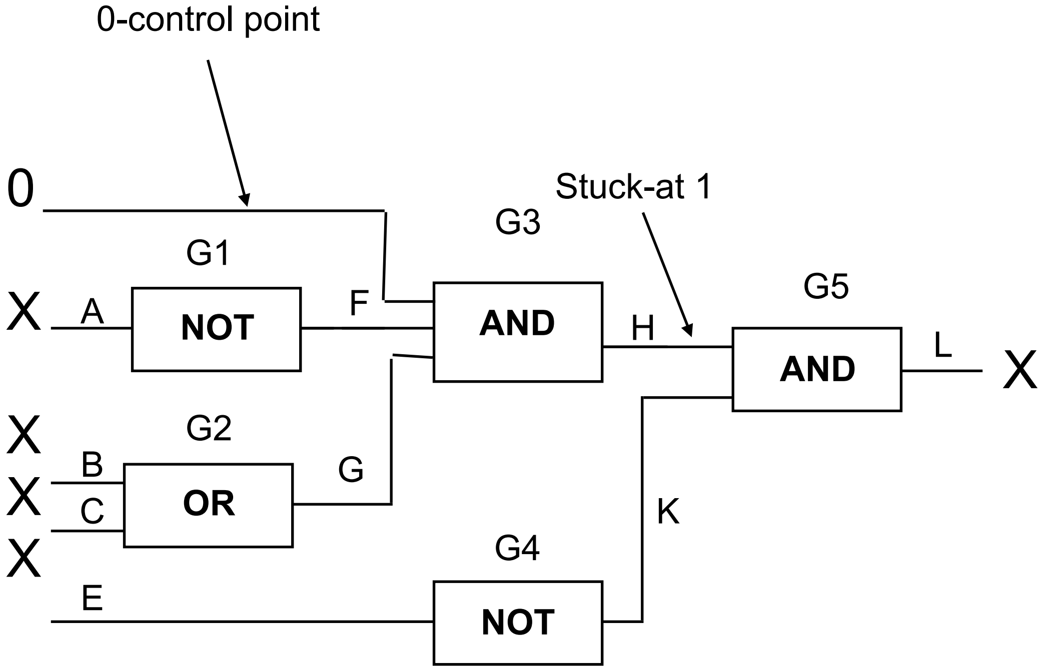


Outline

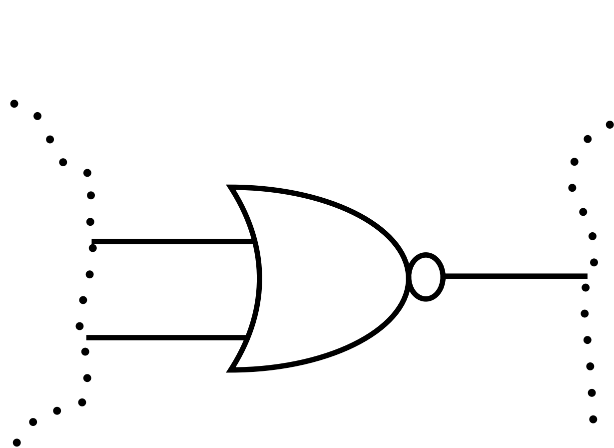
- Electronics
- Manufacturing
- Test, diagnosis, and verification
- Test generation
- <u>Test points and Scan</u>
- Test Compression
- Built-In Self-Test (BIST)
- Systems-on-chip test
- Boundary scan (IEEE 1149.1)

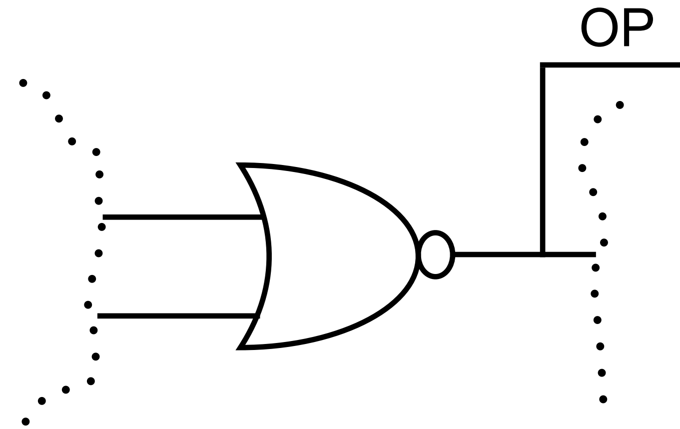
Test Point Insertion



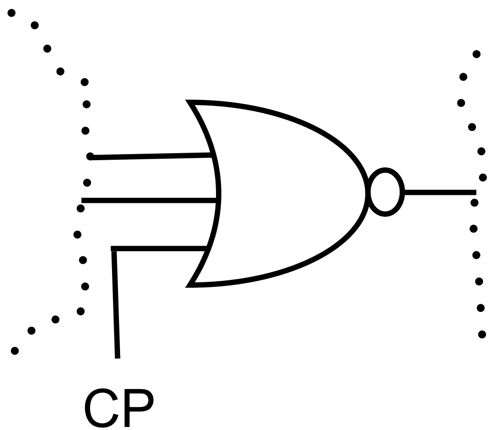


Test Point Insertion

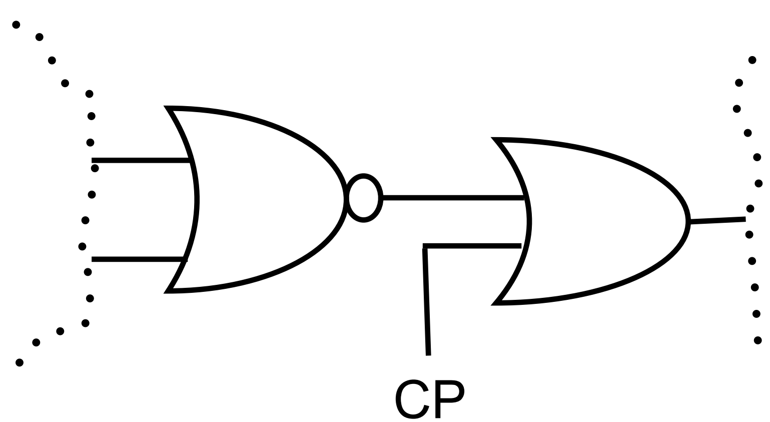

Original



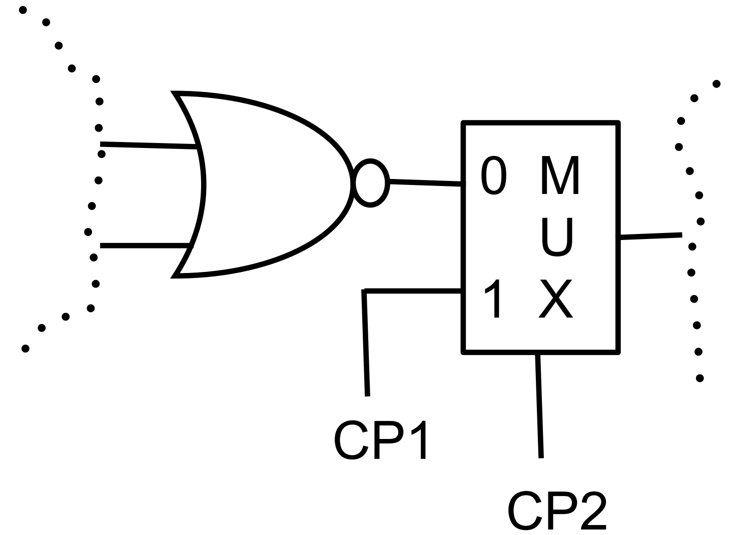
Observation



0-controllability



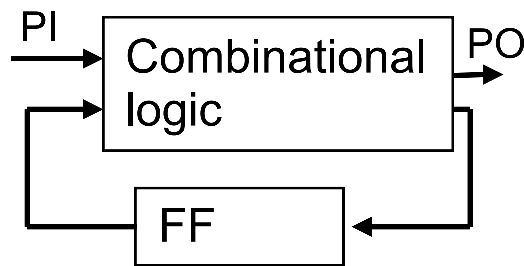
1-controllability



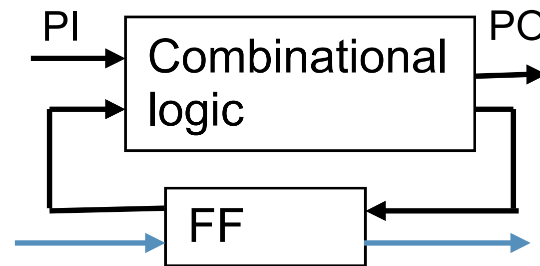
1/0-controllability

Sequential -> Combinational

- Problem: ATPG works for combinational logic while most ICs are sequential
- Solution: Provide a test mode in which flip flops can be accessed directly
- Register provide virtual primary inputs/primary outputs

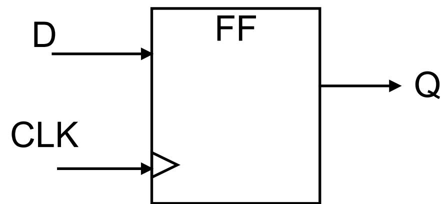


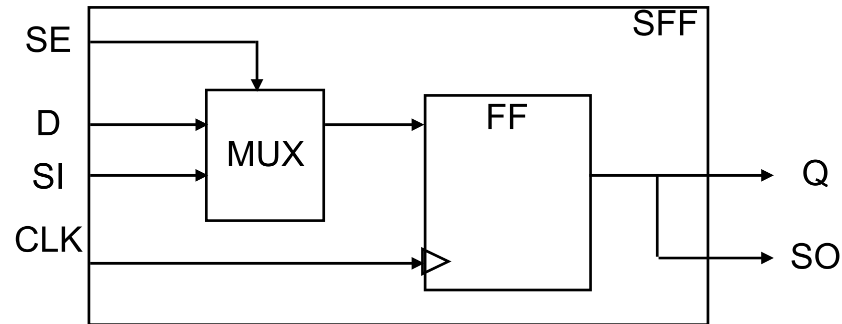
Flip flops



1. Write flip flops
2. Stimulus at inputs
3. Normal cycle launch/capture
4. Observe output
5. Read flip flops

Scan Design Concept



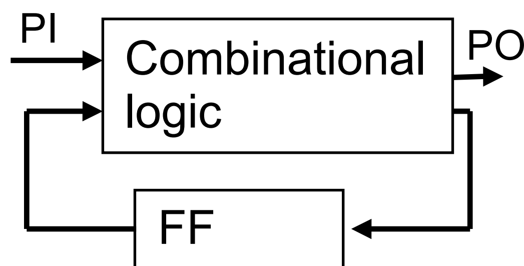


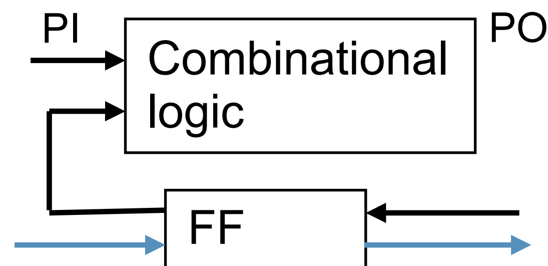
SE: Scan enable
SI: Scan input
SO: Scan output

- Replace flip flop (FF) with scan flip flop (SFF): extra multiplexer on data input
- Connect SFFs to form one or more scan chains
- Connect multiplexer control signal to scan enable

Sequential -> Combinational

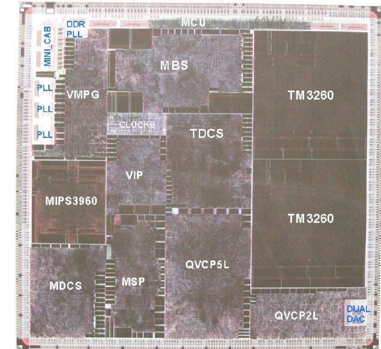
- Circuit can be in two modes: Functional mode and Test mode
- In Test mode test data can be shifted in and shifted out
- Test mode adds virtual PI and PO such that test data can be directly applied to combinational logic
- ATPG for combinational logic works also for sequential





1. Write flip flops
2. Stimulus at inputs
3. Normal cycle launch/capture
4. Observe output
5. Read flip flops

Test application



Automatic Test Equipment (ATE)

Test stimuli (TS)
0010100
0110000

Device under test

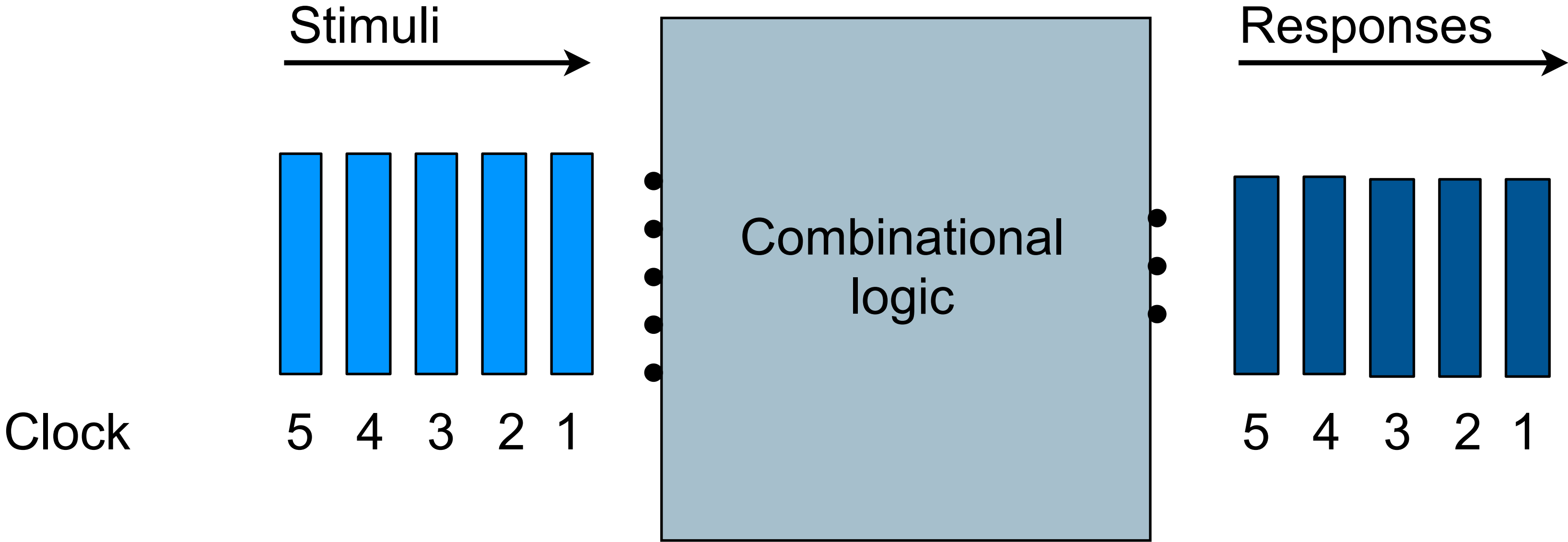
Expected responses (ER)
1011001
1101010

Produced responses (PR)
0111011
0100101

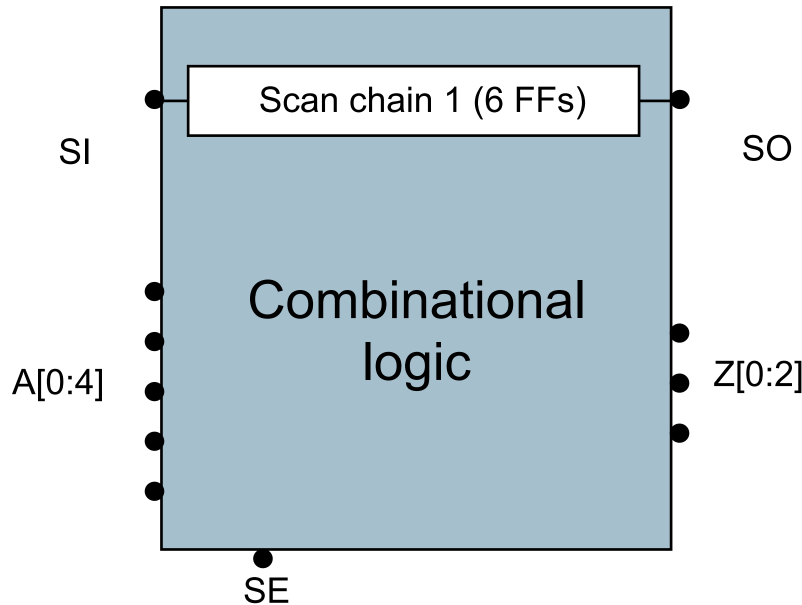
Compare

Pass/fail

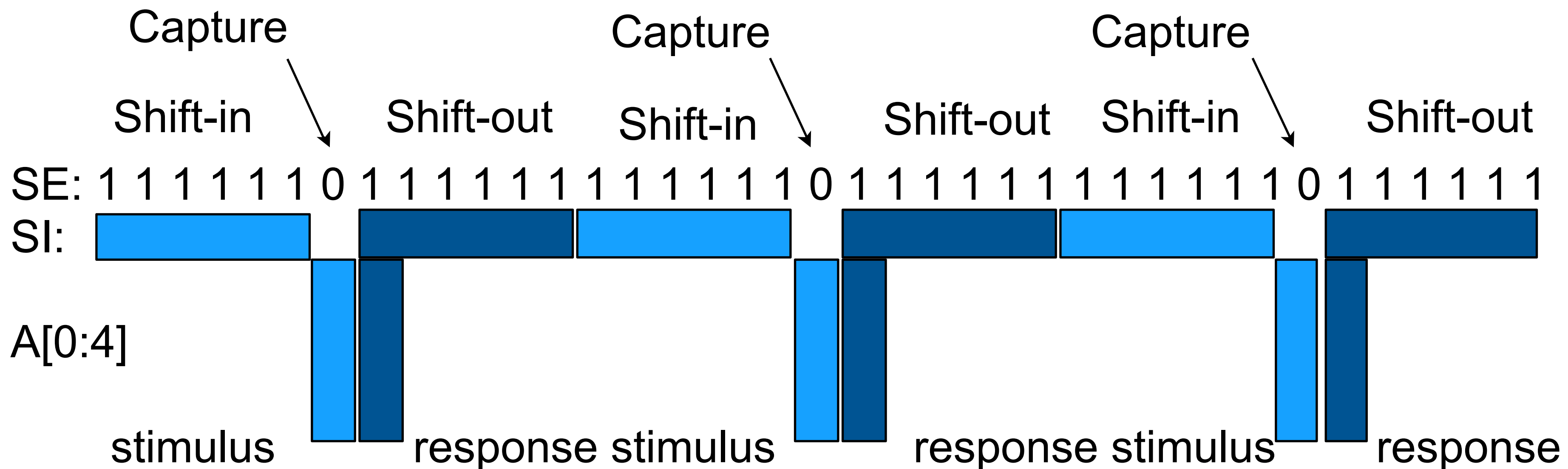
Test Application



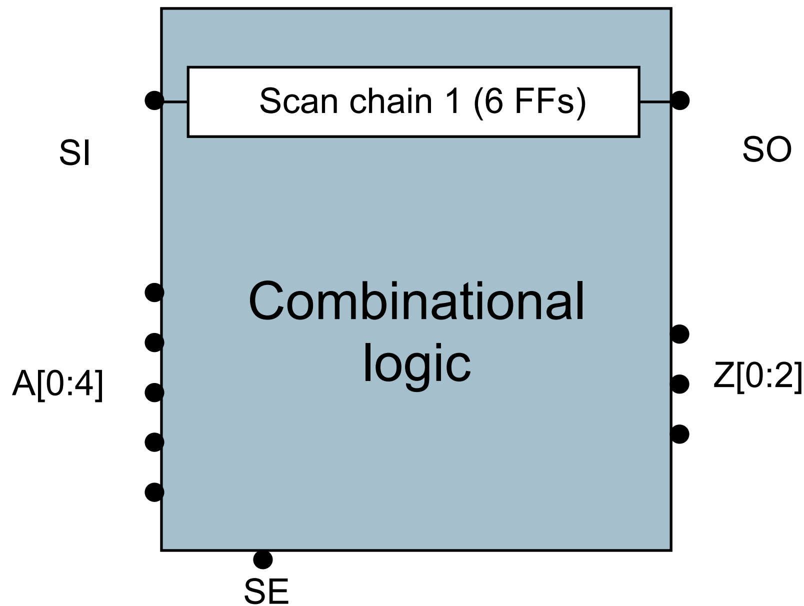
Scan Test Application - first attempt



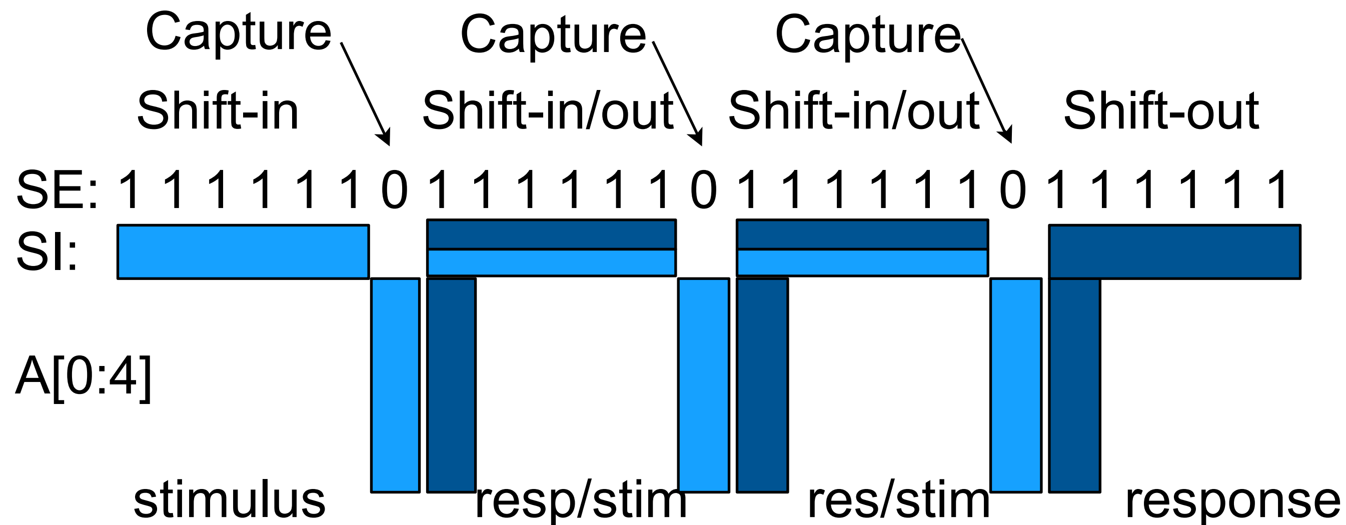
Test time=number of patterns *(shift-in + capture + shift-out)= 3*(6+1+6)=39



Scan Test Application - second attempt



Test time=number of patterns *(shift-in + capture) + shift-out= 3*(6+1)+6=27



Scan Benefits and Costs

Scan Benefits

- Automatic scan insertion
- ATPG
- High fault coverage
- Short test development time

EDA tools

- For scan insertion (converting flip flops to scan flip flops)
- Connection
- Partial scan selection
- Scan stiching

Scan Costs

- Silicon area - Mux, scan chain, scan enable
- Performance reduction - Multiplexer in time-critical path
- IC pins - Scan-in (SI), scan-out (SO), scan_enable (SE)
- Test time - Serial shifting is slow

Delay Test

- Stuck-at-fault test consist of one vector. Each vector applied at slow speed (DC-scan).
- Timing related faults need two vectors and they are to be applied on consecutive clock cycles (at normal clock speed) (AC-scan)
- At speed test:
  - Vector V1 is applied to set the circuit in its state
  - Vector V2 is applied
  - Response is captured
- Three approaches:
  - Launch-on-capture
  - Launch-on-shift
  - Enhanced scan

Launch on shift (LOS) and launch on capture (LOC)

- Launch on capture (broadside or double capture)
  - shift in test stimuli (usually at low speed). For an n-bit shift register, shift in n bits.
  - apply a capture to create transition
  - apply another capture cycle to capture the response
- Launch on shift (skewed load)
  - shift in test stimuli (usually at low speed). For an n-bit shift register, shift in n-1 bits at low speed.
  - The final bit is shifted at high speed and then a capture is applied in high speed.

Outline

- Electronics
- Manufacturing
- Test, diagnosis, and verification
- Test generation
- Test points and Scan
- <u>Test Compression</u>
- Built-In Self-Test (BIST)
- Systems-on-chip test
- Boundary scan (IEEE 1149.1)

ATE-based testing

- Advantages with ATE-based testing
  - High quality test
  - Diagnosis possible
- Disadvantages with ATE-based testing
  - ATEs are expensive
  - Interface between ATE and device-under-test
  - Low throughput due to:
    - Long scan-chains
    - Low test shift speed
    - Limited number of channels
  - Limited tester memory
  - Only possible to test at manufacturing

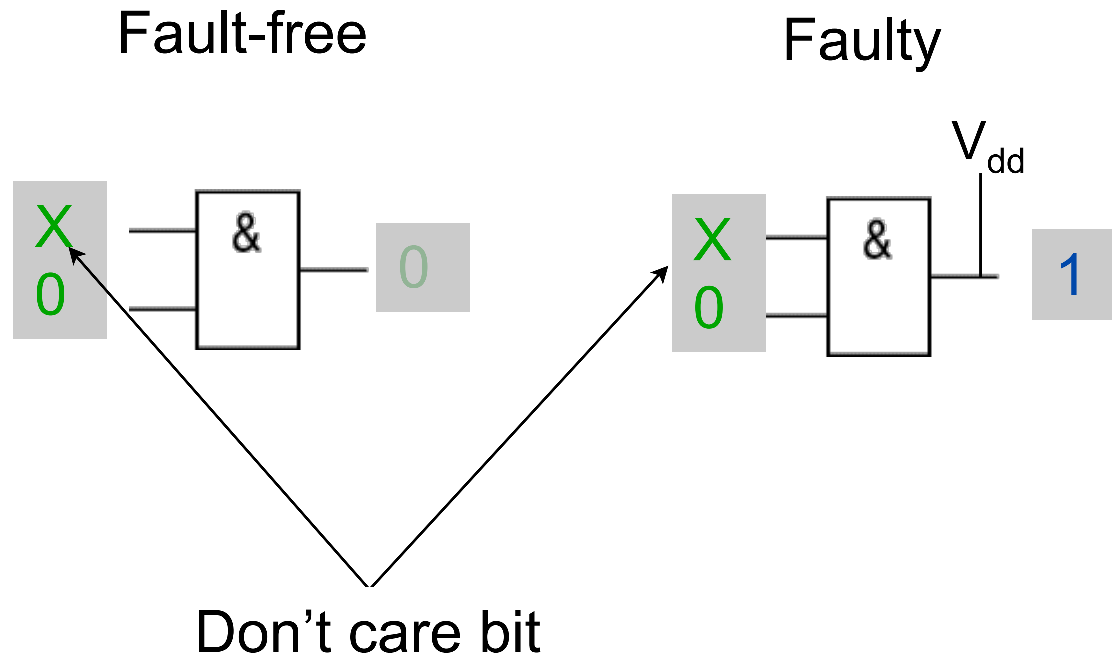
Alternatives

- Test data compression
- Built-In Self-Test
  - Logic BIST and Memory BIST

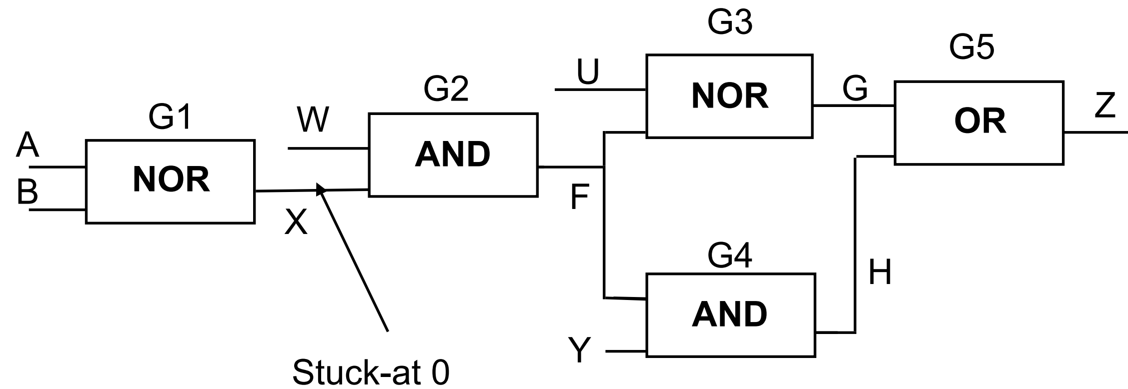
- Important aspects:
  - Test stimuli
  - Test responses

Test generation

Example: Create test for output connected to V_{dd}



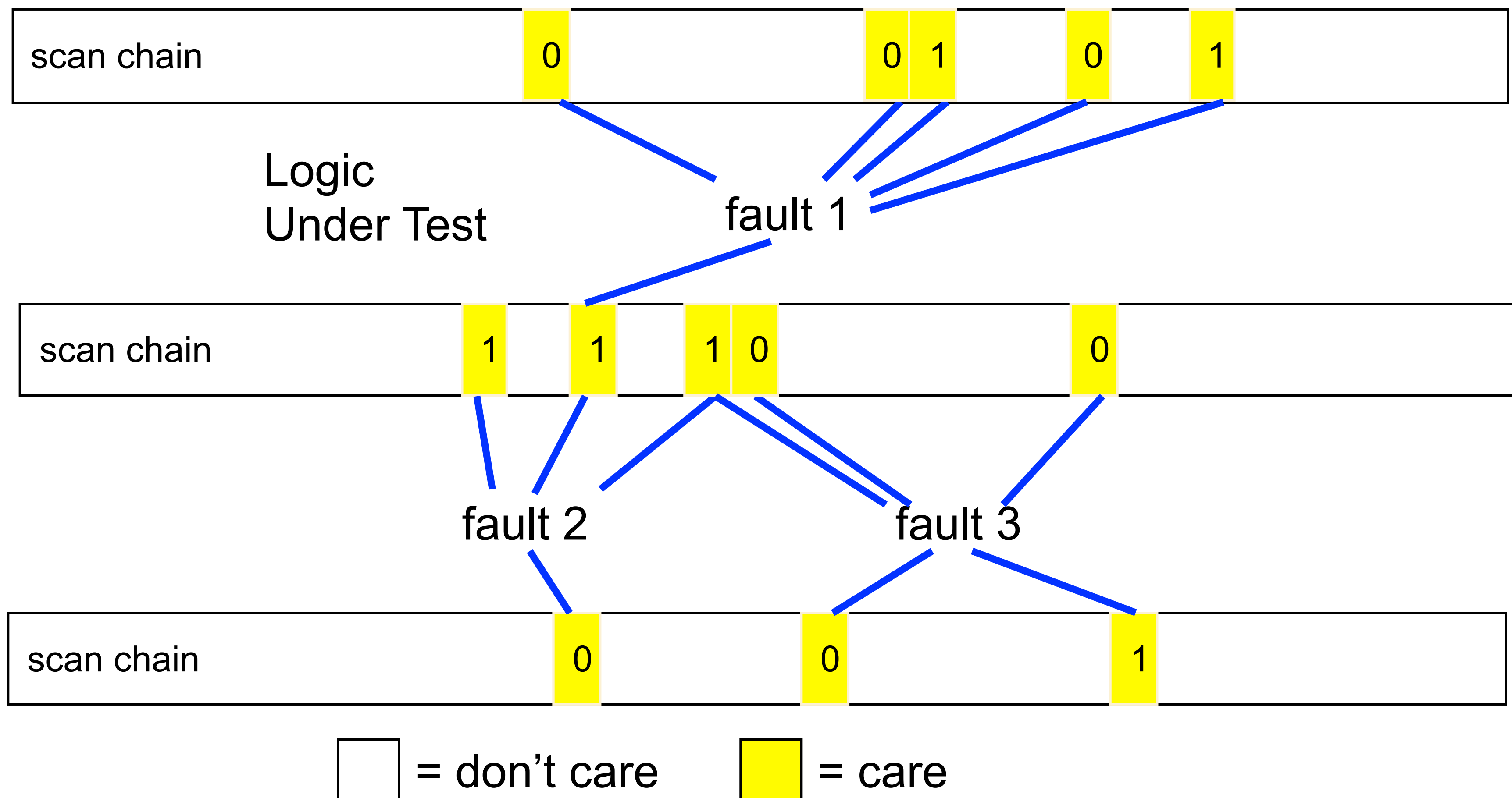
D-Algorithm



- Initialize the circuit by placing X on each line
- For a SA0, X=D and A=B=0 (for the selected fault)
- Propagate D through G2
- Select a sensitizing path (we select G3)
- To propagate through G3, we let U=0
- Propagate through G5
- Reached a primary output with D
- Justify values on H, Y, U, W. H=0 (ok). F=0? Conflict! Select Y=0

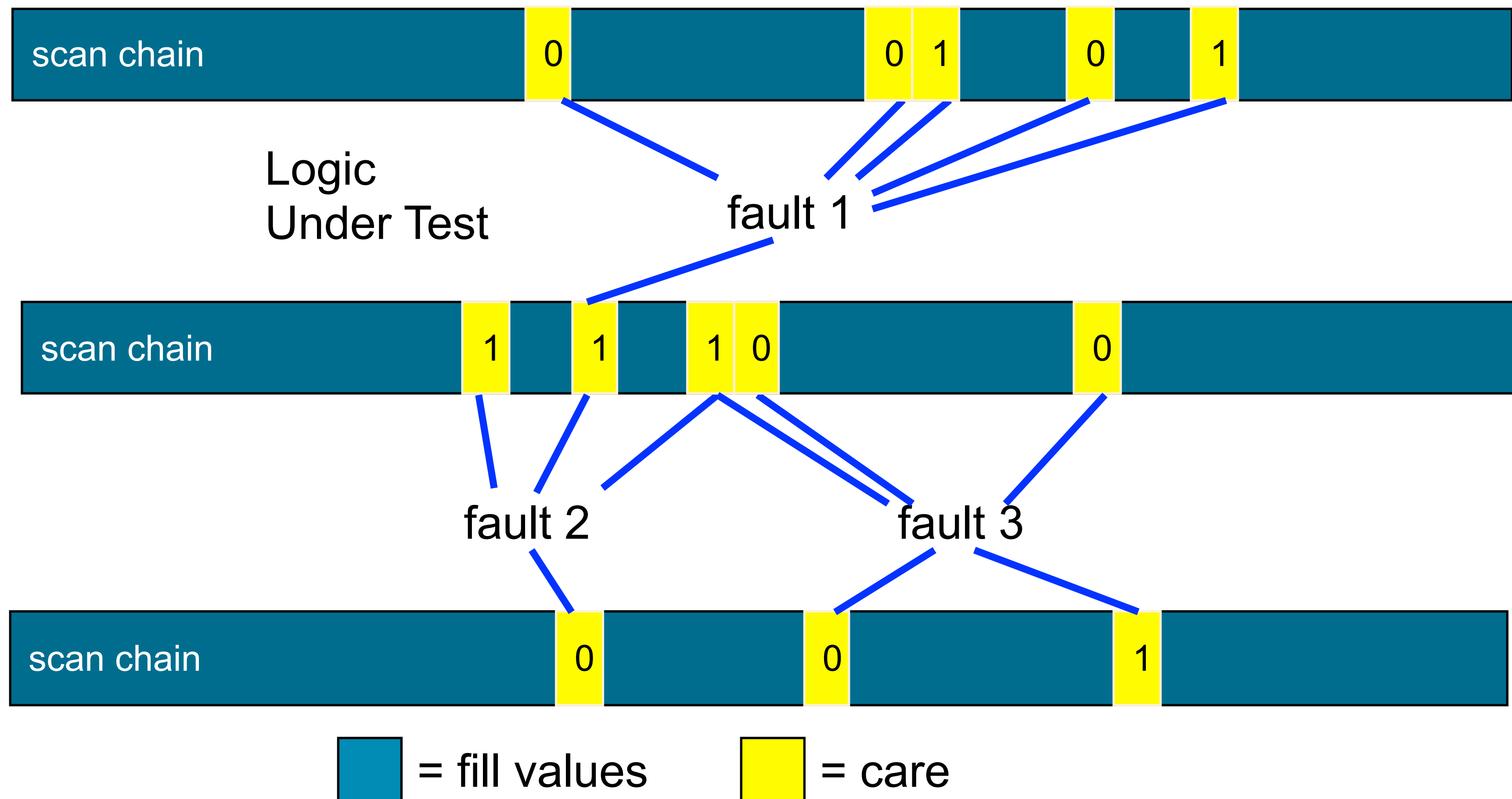
Analysis of Scan Test

- ATPG first creates test cubes
  - Merged for several faults; many unspecified don't care values

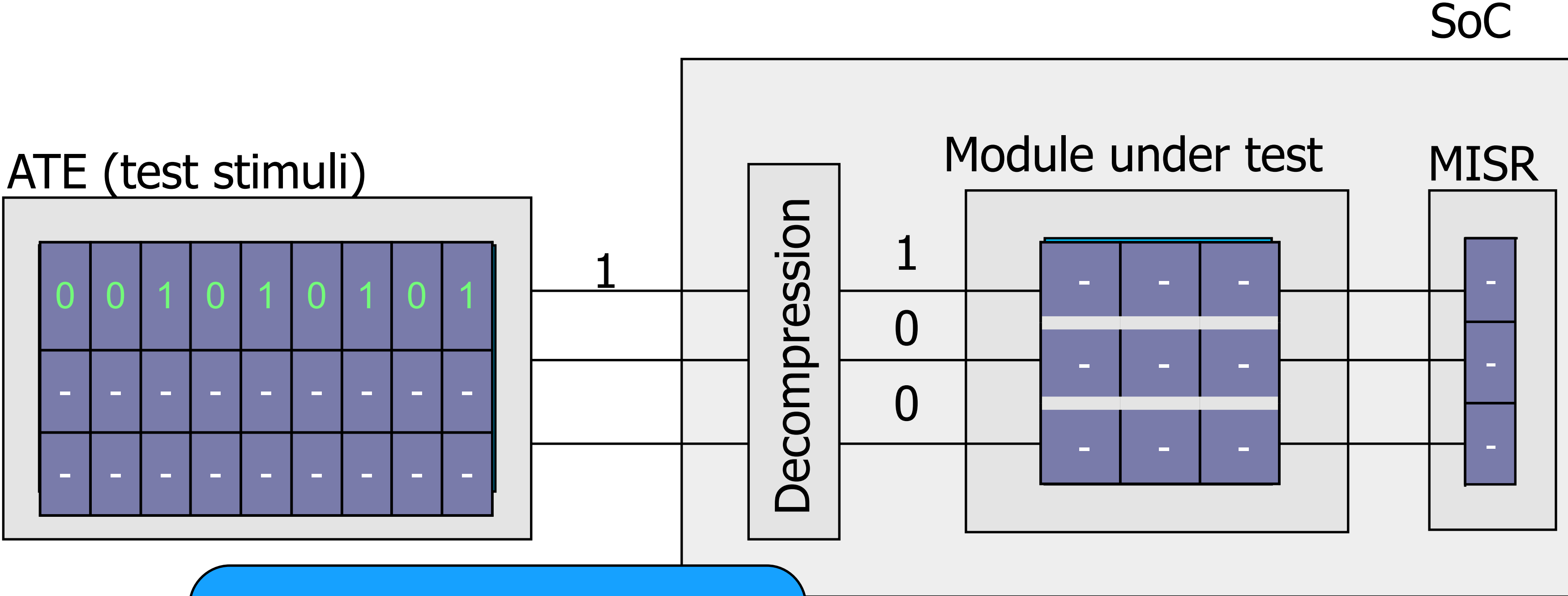


Analysis of Scan Test

- Then, convert cubes to vectors by filling don't cares
  - Fault simulate vectors to mark off additional faults



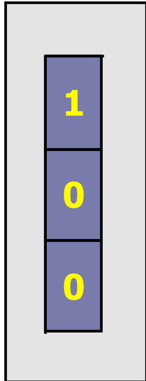
Test data compression

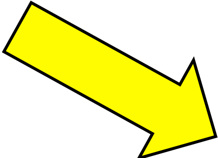


Few ATE channels and many (short) scan-chains lead to shorter test times

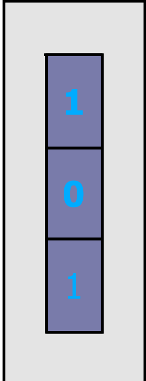
Test data compression

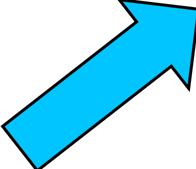
MISR (produced)

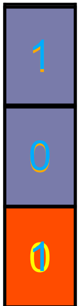




MISR (expected)







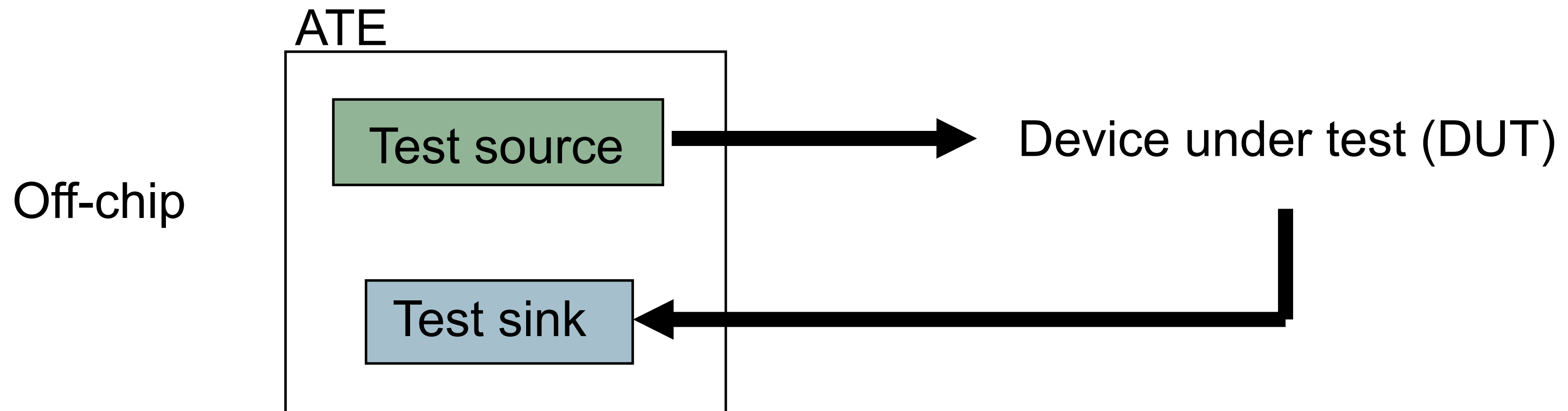
Faulty module!

Outline

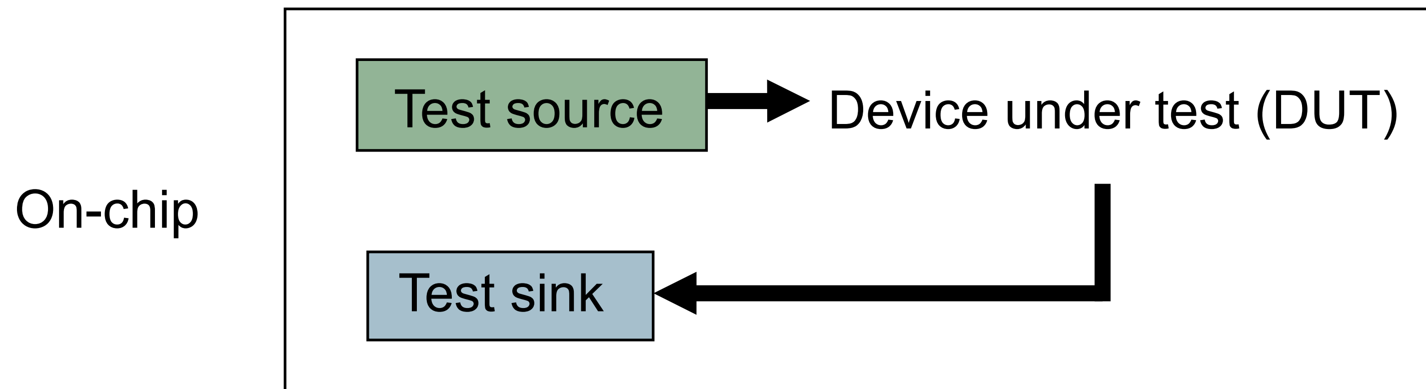
- Electronics
- Manufacturing
- Test, diagnosis, and verification
- Test generation
- Test points and Scan
- Test compression
- <u>Built-In Self-Test</u>
- Systems-on-chip test
- Boundary scan (IEEE 1149.1)

On-chip/off-chip

Off-chip



On-chip



Test Pattern Generation

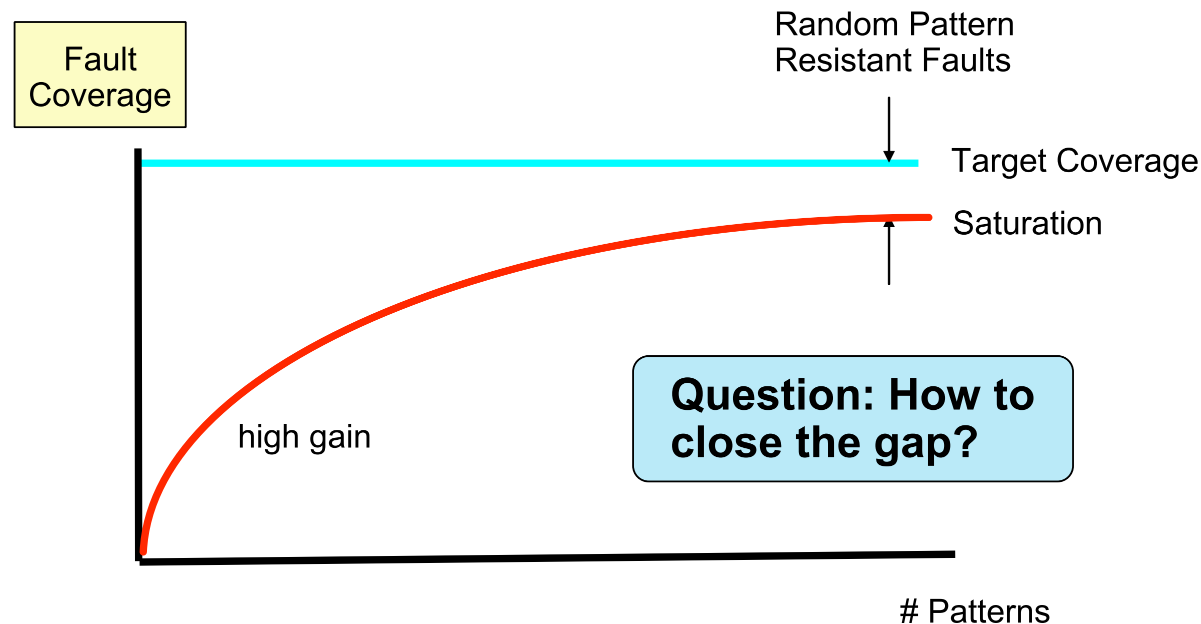
- How store/generate test patterns on-chip?

- Deterministic test patterns
- Exhaustive test patterns
- Pseudo-exhaustive/random test patterns
- Random test patterns

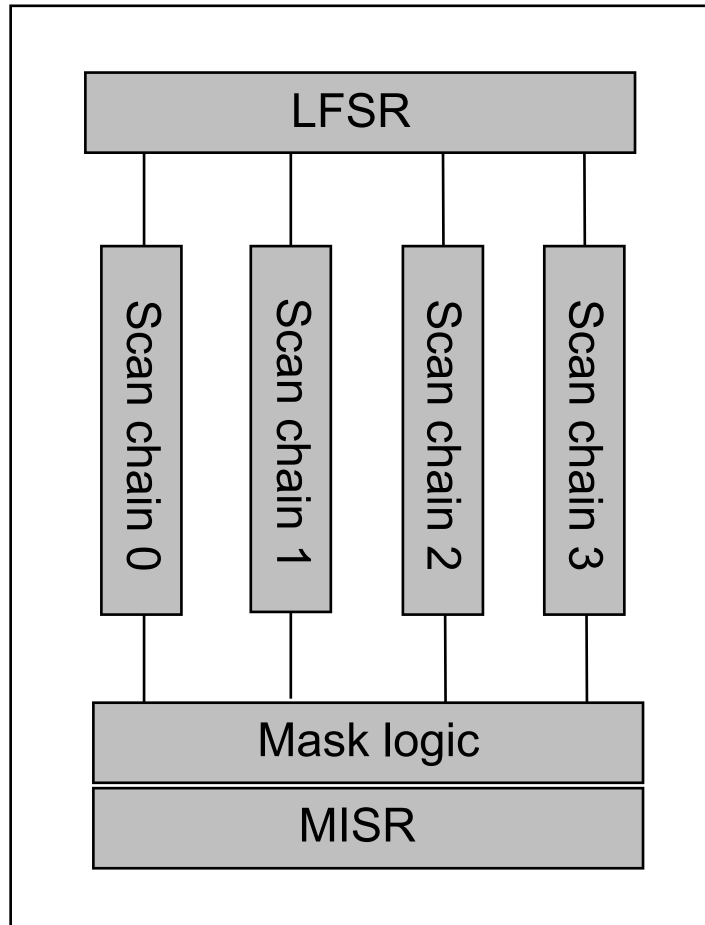
- Commercial tools usually make use of a random test generation for 60-80% of the faults (easy to detect) and deterministic test generation for the remaining part (hard to detect)

Test generations

- Some logic takes too long to test with pseudo-random patterns
  - Too many specific input bit values are required
  - Too many pseudo-random trials needed to achieve the required value combination



STUMPS: Self-testing using MISR and parallel shift register sequence generator



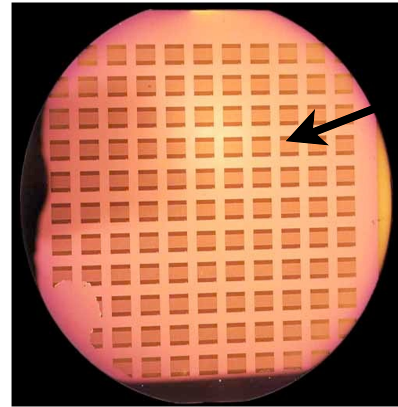
Test source: **L**inear **F**eedback **S**hift **R**egister (LFSR)
Test sink: **M**ultiple **I**nput **S**ignature **R**egister (MISR)

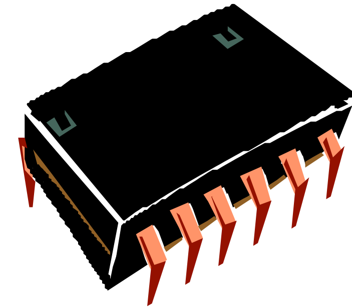
Outline

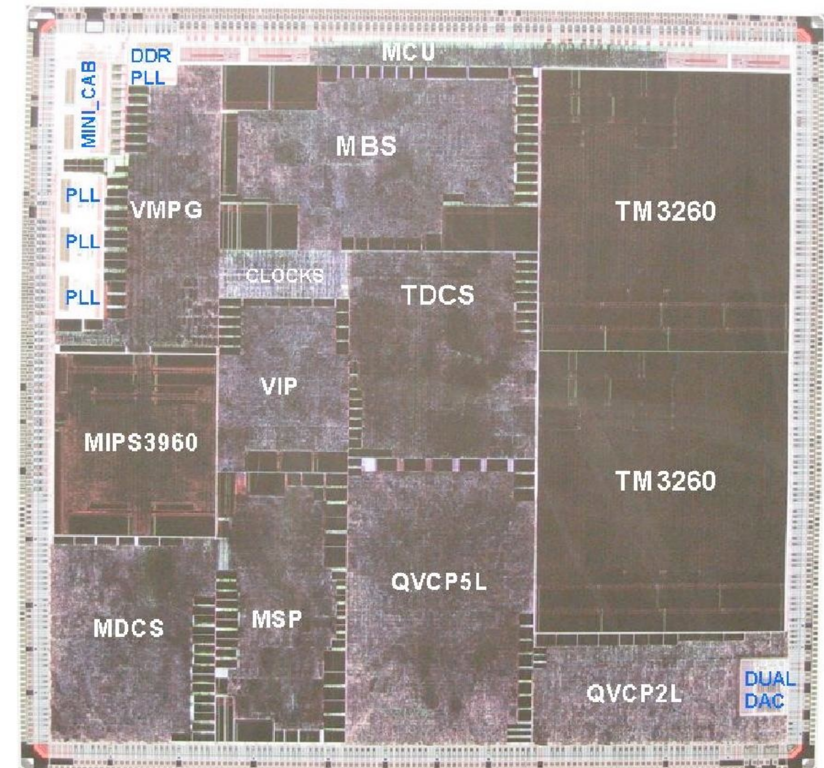
- Electronics
- Manufacturing
- Test, diagnosis, and verification
- Test generation
- Test points and Scan
- Test compression
- Built-In Self-Test (BIST)
- <u>Systems-on-chip test</u>
- Boundary scan (IEEE 1149.1)

System-on-Chip

Die

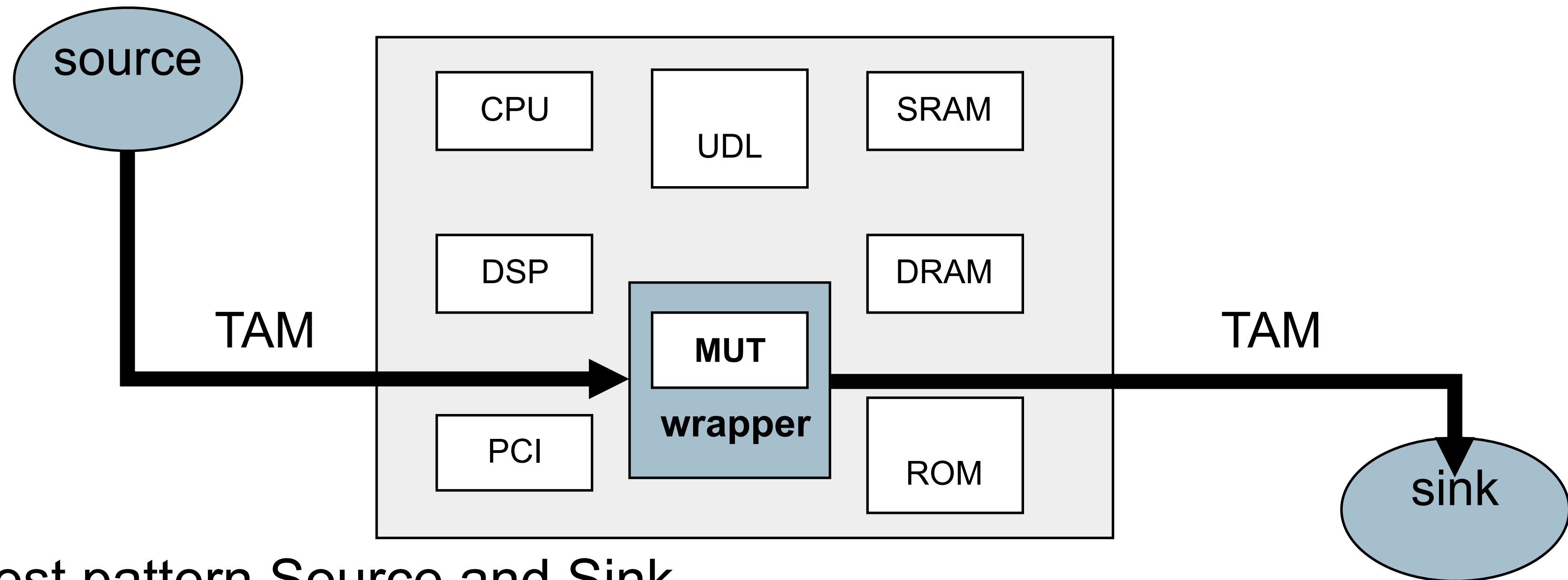






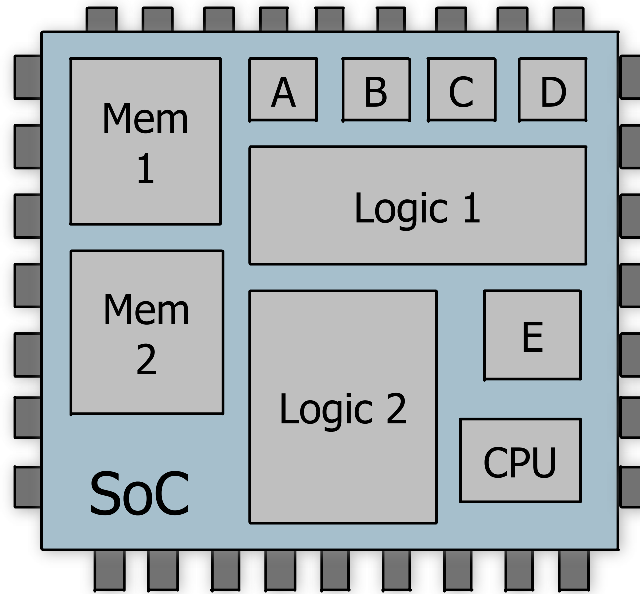
- Viper 2.0 RevB
- Analog/Digital TV Processor
- 10mm x 10 mm (100 mm^2)
- ~10 M gates
- ~50 M transistors
- ~100 clock domains

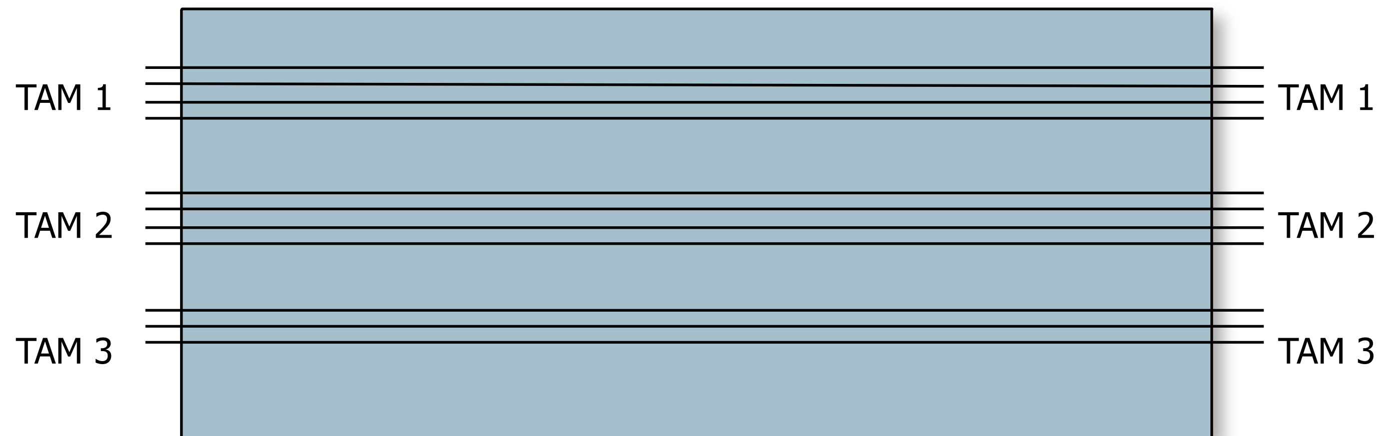
Generic Test Access Architecture



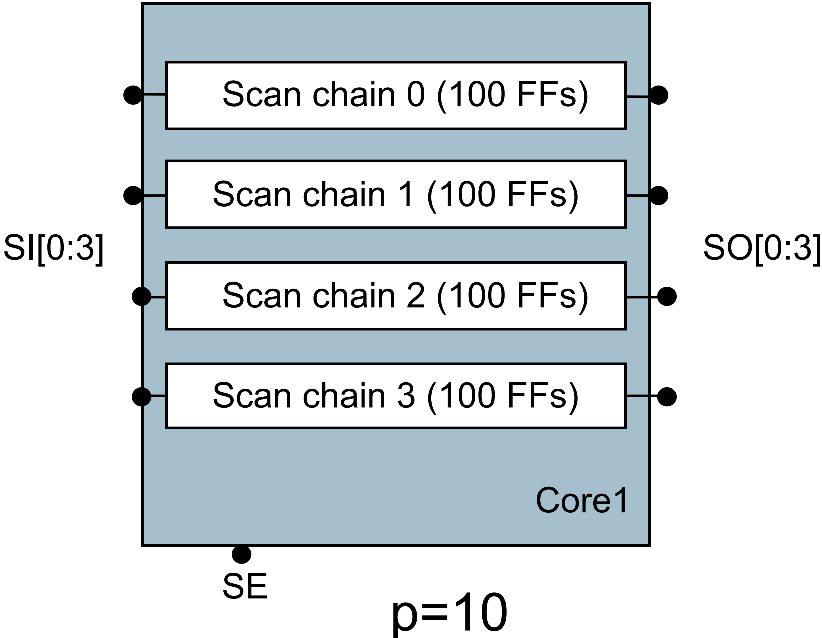
- Test pattern Source and Sink
  - Store/generate test stimuli and store/evaluate test responses
- Test Access Mechanism (TAM)
  - Transports test patterns to/from module under test (MUT)
- Test Wrapper
  - Provides test access to MUT
  - Isolates MUT at test

Architecture Design

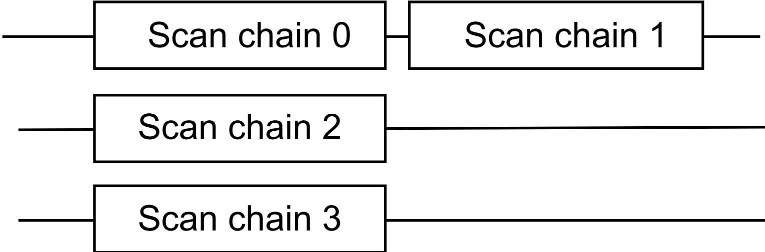




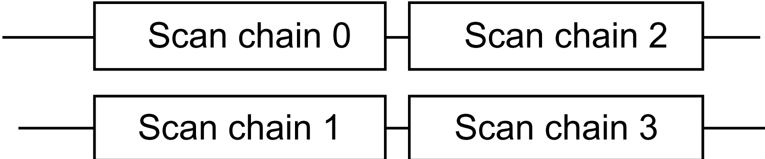
Wrapper Design



p=10

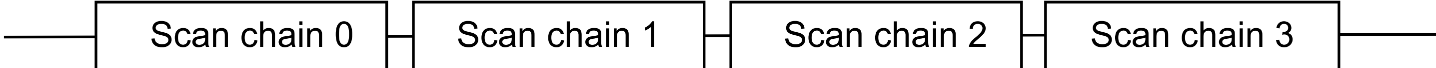


T=(200+1)*10+200=2210



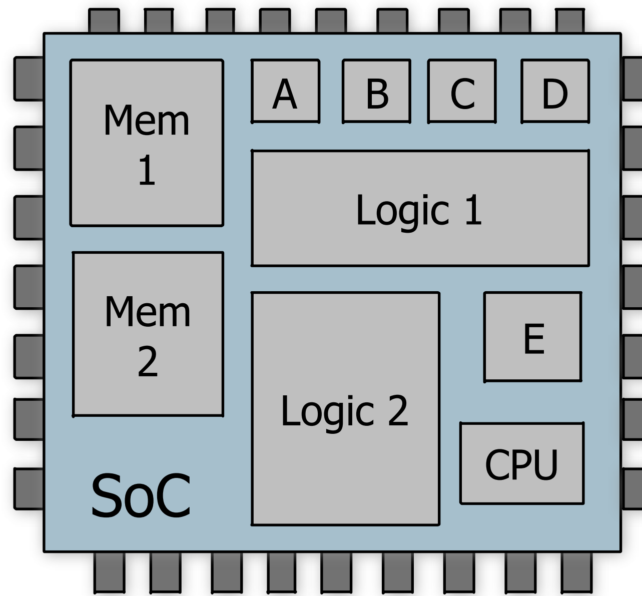
T=(200+1)*10+200=2210

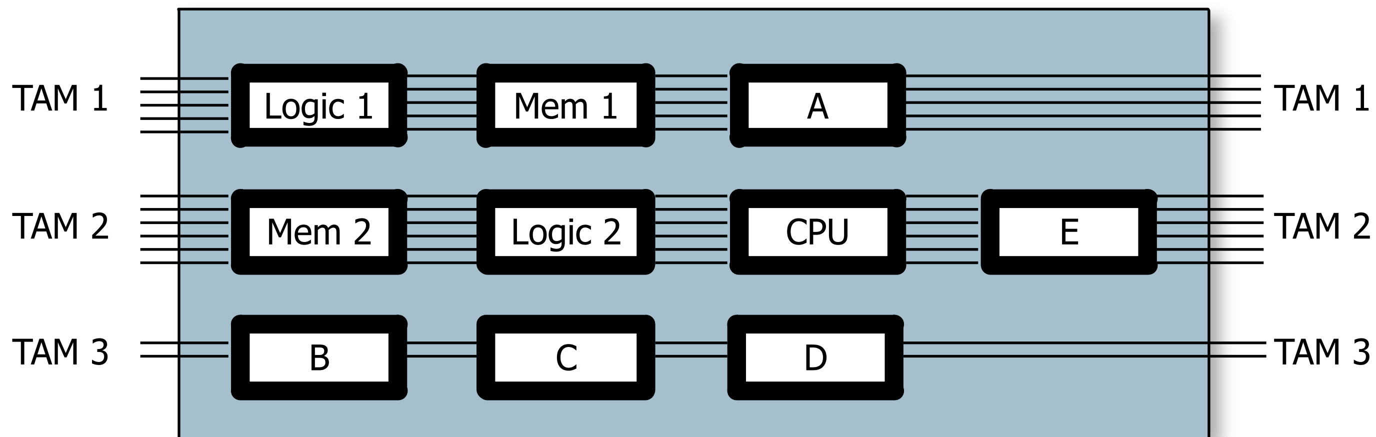
Test time (T) = (sc+1)*p+sc



T=(400+1)*10+400=4410

Core To TAM Assignment

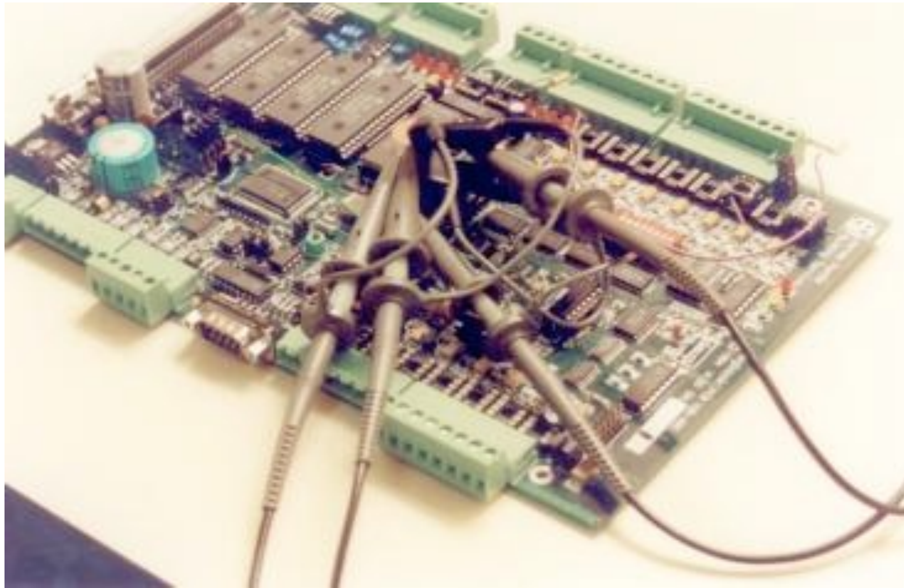




Outline

- Electronics
- Manufacturing
- Test, diagnosis, and verification
- Test generation
- Test points and Scan
- Test Compression
- Built-In Self-Test (BIST)
- Systems-on-chip test
- <u>Boundary scan (IEEE 1149.1)</u>

Probing for Test



Model TR-5-1216

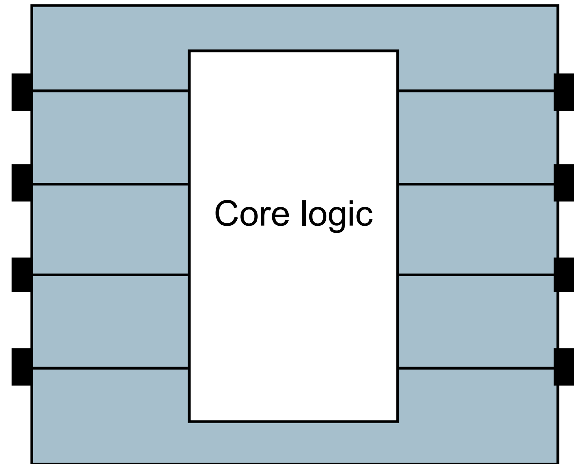
Test Objectives

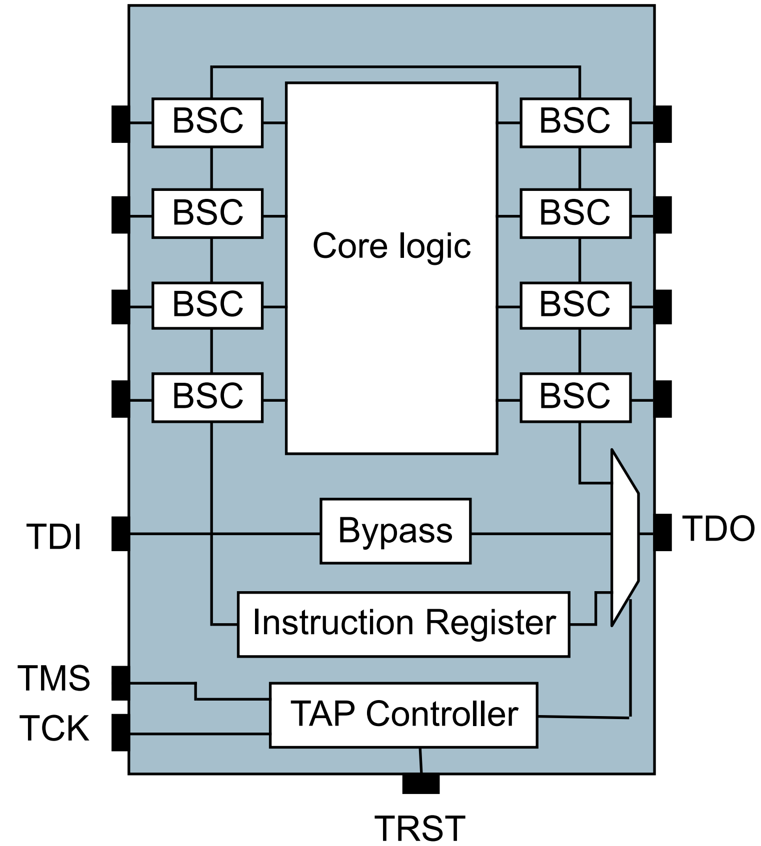
- Given a Printed Circuit Board (PCB) composed of a set of components (ICs) where each component is tested good.
- The main objectives are to ensure that all components are:
  - correct (the desired ICs are selected)
  - mounted correctly at the right place on the board and
  - ensuring that interconnections are functioning according to specification
- Problems that may occur:
  - A component does not contain logic
  - A component is not placed where it should be,
  - A component is at its place but turned wrongly,
  - A component is correct but the interconnection is not correct, for example due to bad soldering.

Boundary Scan (IEEE std. 1149.1)

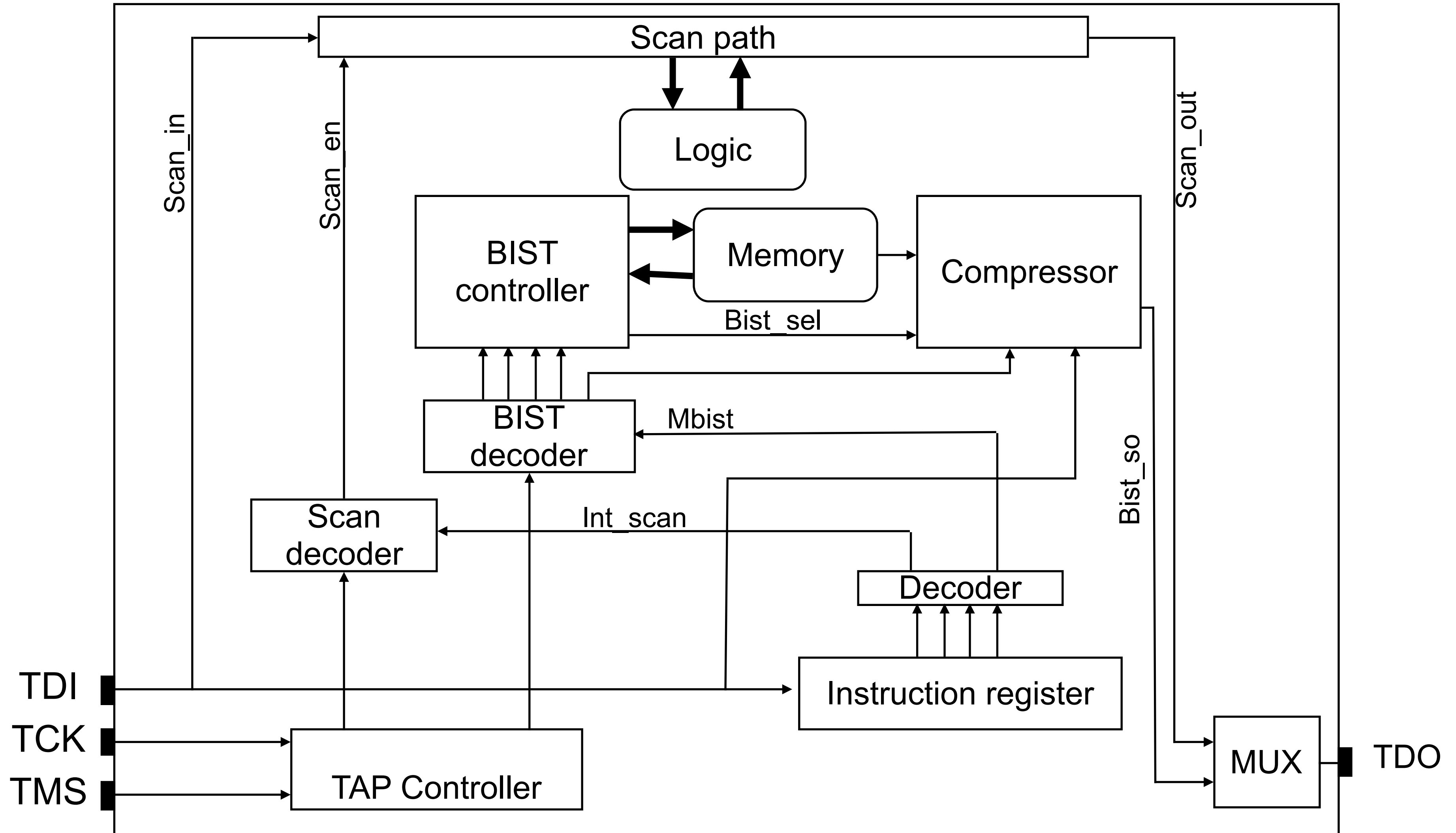
- The Joint European Test Action Group (JETAG), formed in mid-80, became Joint Test Action Group (JTAG) in 1988 and formed the IEEE std 1149.1. The standard consists of:
  - Test Access Port (TAP)
  - TAP Controller (TAPC),
  - Instruction Register (IR), and
  - Data Registers (DR)

Boundary Scan





Scan and MBIST support with Boundary Scan



Introduction to structured VLSI design

Design for Test (DfT) - Part 2

Erik Larsson

EIT, Lund University