Introduction to structured VLSI design

Design for Test (DfT) - Part 1

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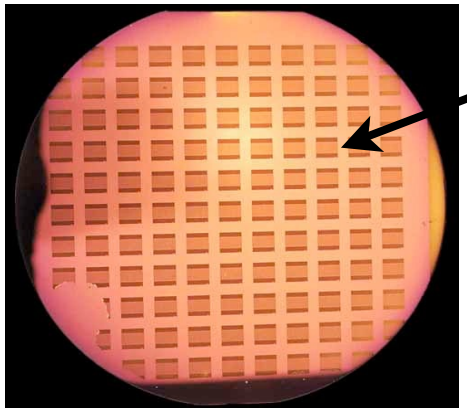
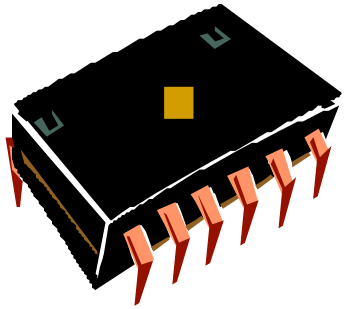
Outline

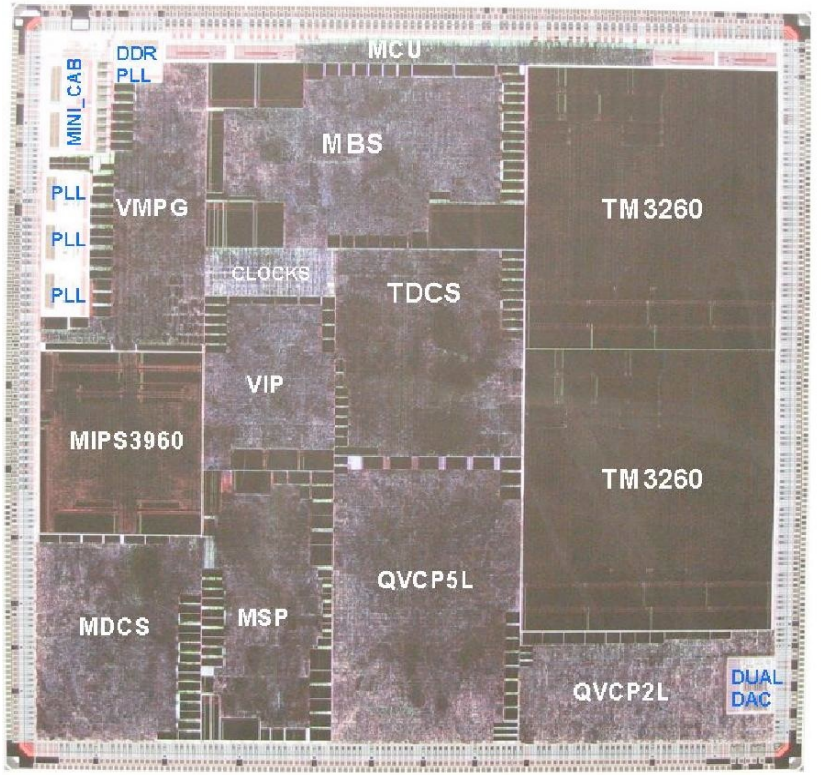
- Electronics
- Manufacturing
- Test, diagnosis, and verification
- Test generation

Integrated Circuits (IC)



Die

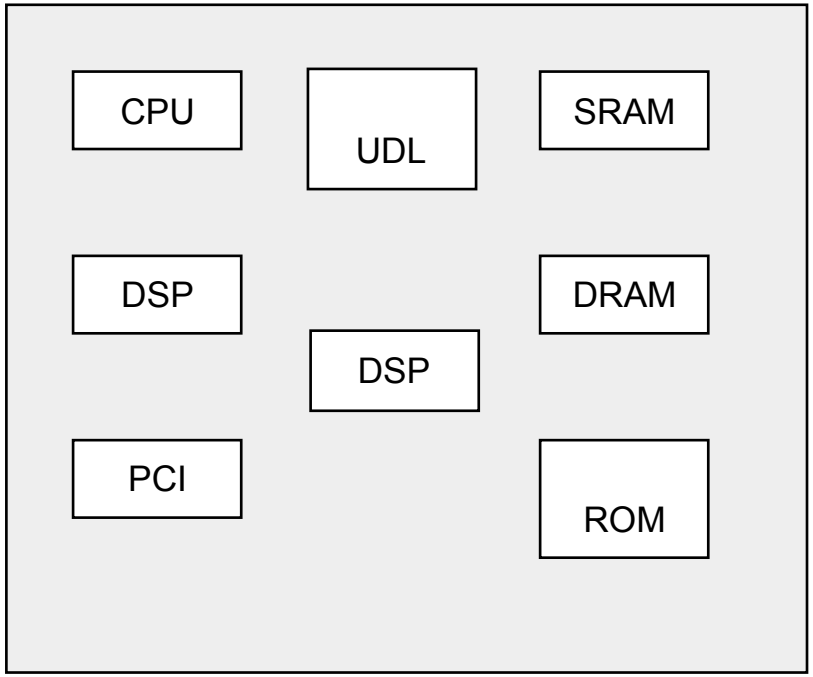




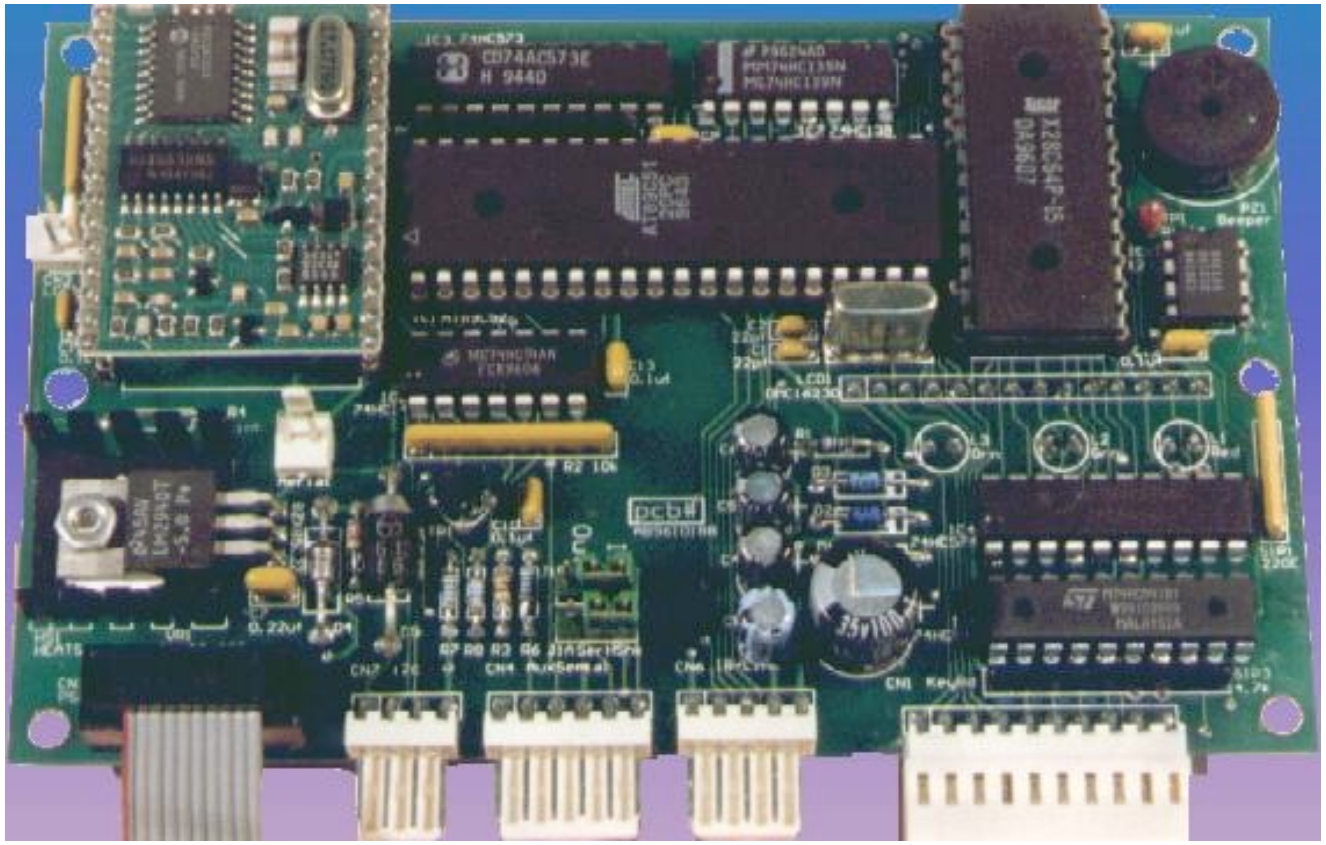
- Viper 2.0 RevB
- Analog/Digital TV Processor
- 10mm x 10 mm (100 mm^2)
- ~10 M gates
- ~50 M transistors
- ~100 clock domains

System-on-Chip

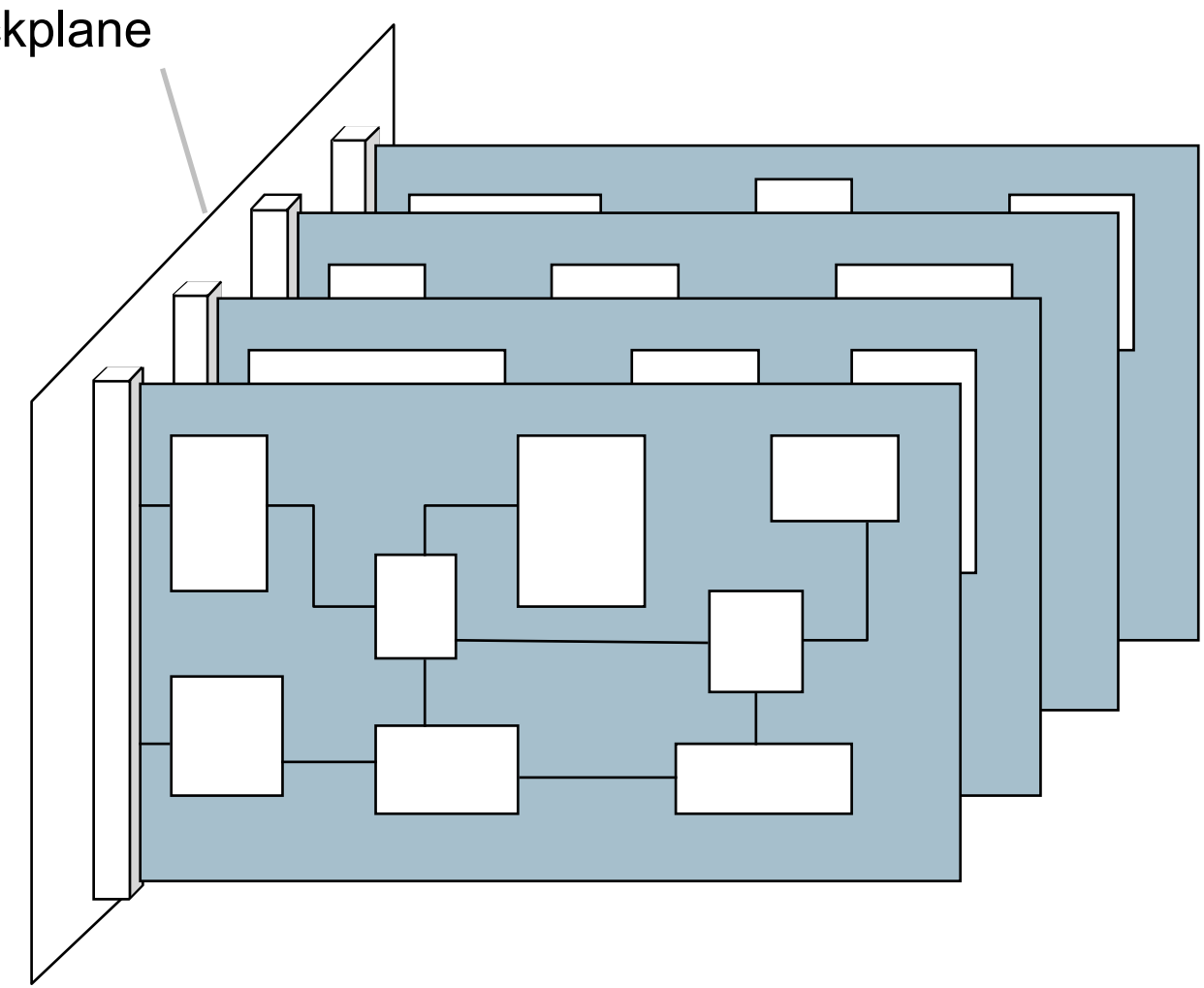
- Processor Cores
  - ARM, MIPS, PowerPC
- Memories
  - SRAM, ROM, Flash, DRAM
- DSP Cores
- Peripherals
  - DMA Controllers, MMU
- Interface
  - PCI, USB, UART
- Multimedia
  - JPEG compression, MPEG decoder
- Networking
  - Ethernet controller



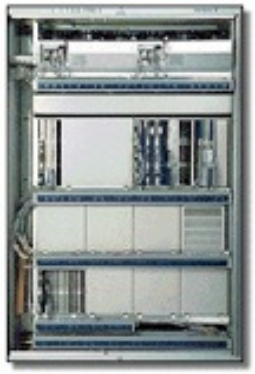
Printed Circuit Board (PCB)



Multi-board System



Products with Electronics



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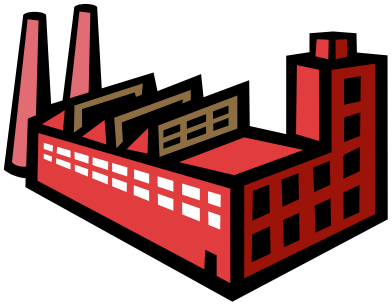
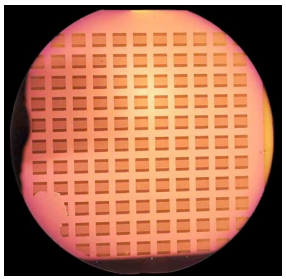
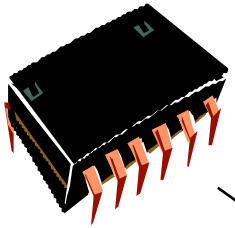
Electronics

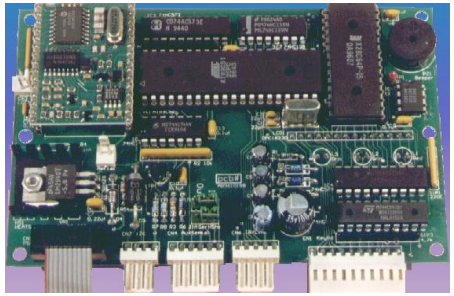


Wafer



IC

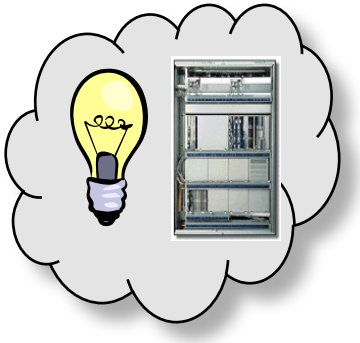




Board

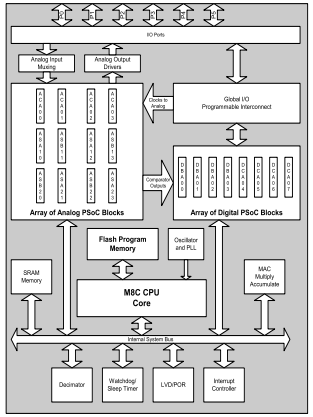
“System”

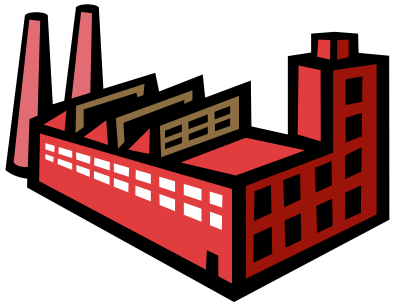
Making Electronic Products



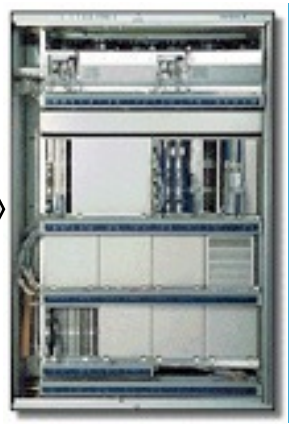
Design

Design specification



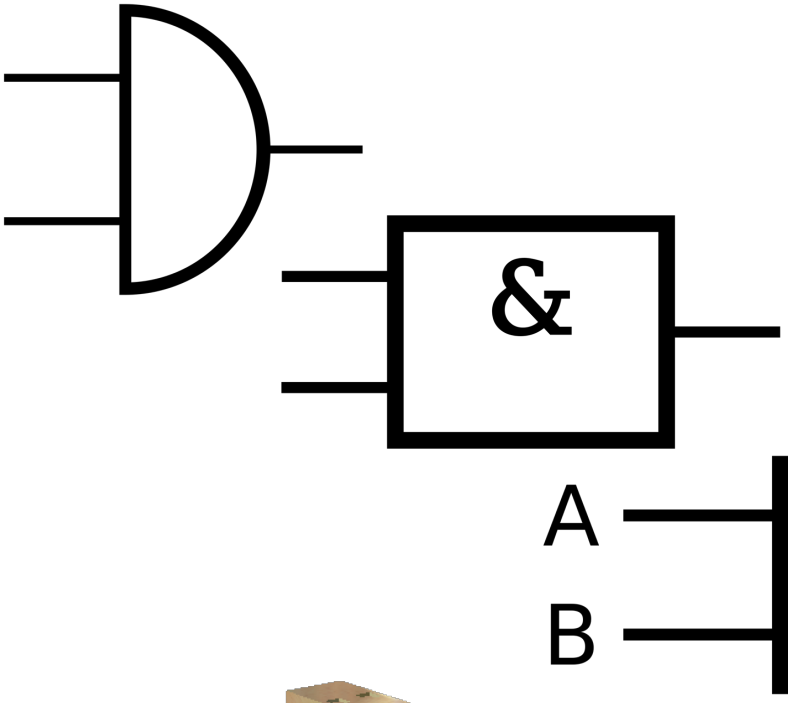


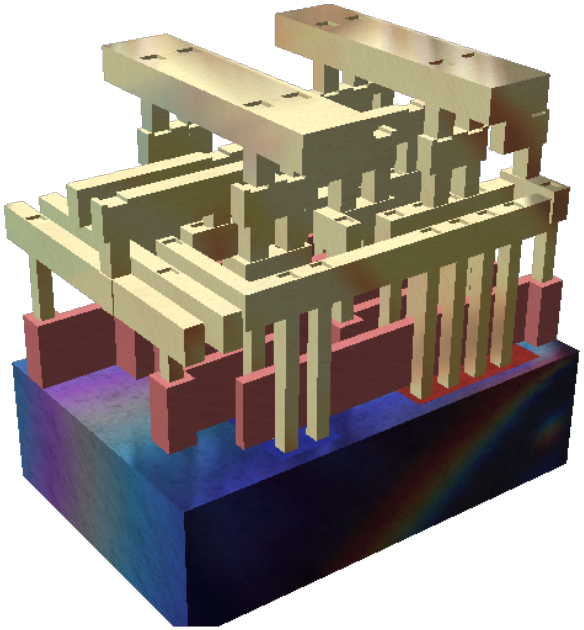
Production

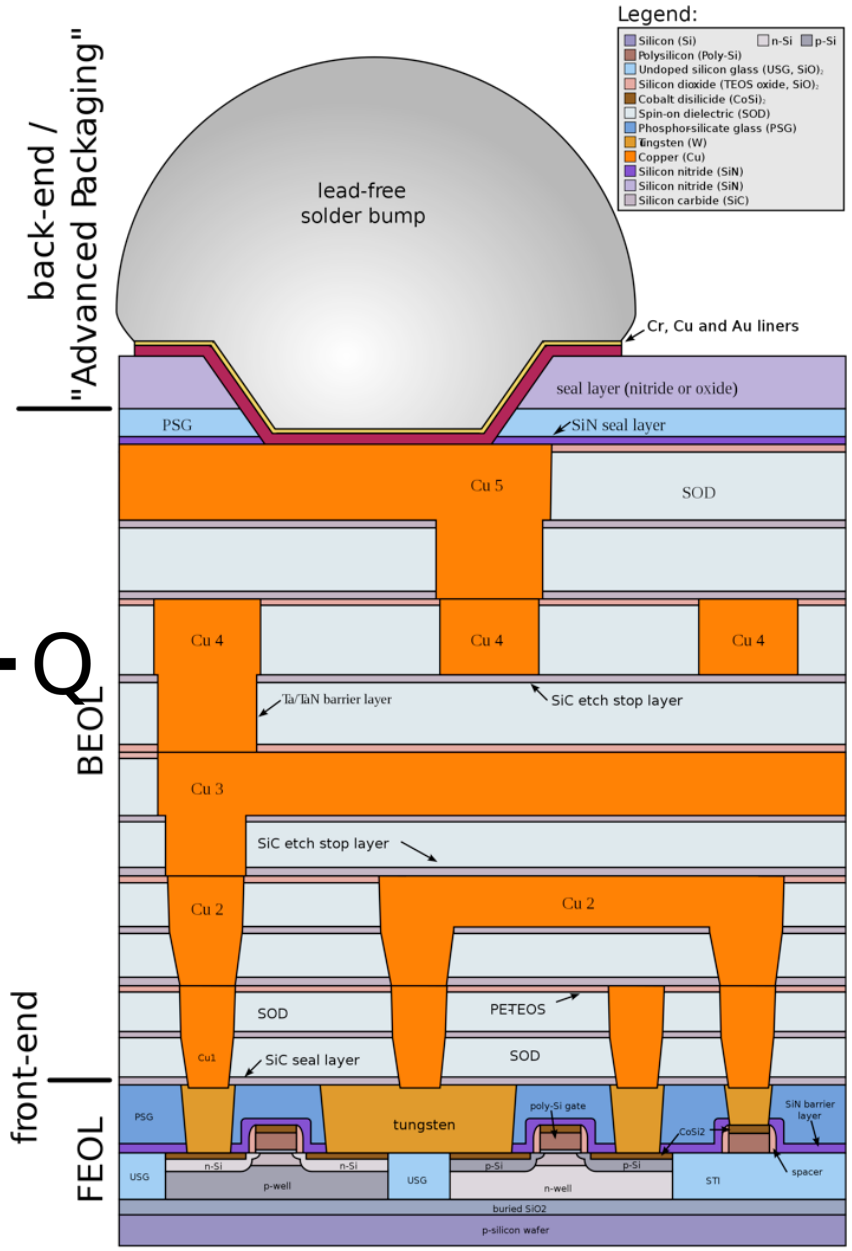


Product

AND-gate

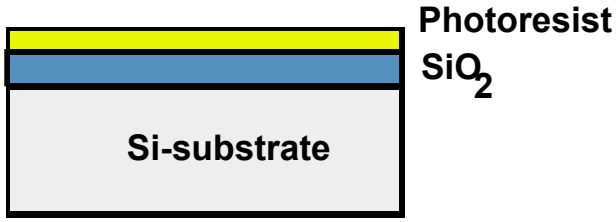

&
A
B
Q



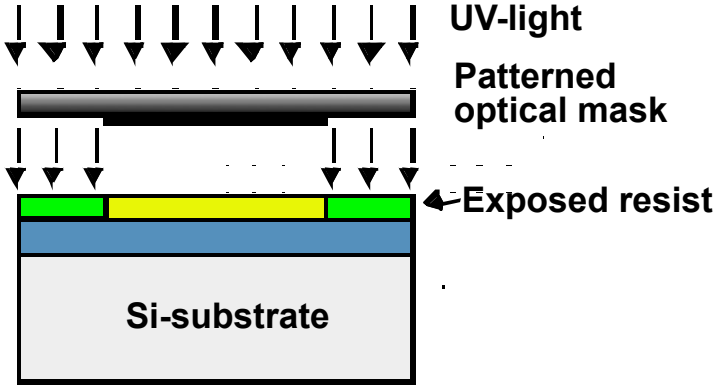

Legend:
Silicon (Si)
n-Si
p-Si
Polysilicon (Poly-Si)
Undoped silicon glass (USG, SiO)2
Silicon dioxide (TEOS oxide, SiO)2
Cobalt disilicide (CoSi)2
Spin-on dielectric (SOD)
Phosphorsilicate glass (PSG)
Tungsten (W)
Copper (Cu)
Silicon nitride (SiN)
Silicon nitride (SiN)
Silicon carbide (SiC)
back-end / "Advanced Packaging"
BEOL
front-end
FEOL
lead-free solder bump
Cr, Cu and Au liners
seal layer (nitride or oxide)
PSG
SiN seal layer
Cu 5
SOD
Cu 4
Cu 4
Cu 4
Ta/TaN barrier layer
SiC etch stop layer
Cu 3
SiC etch stop layer
Cu 2
Cu 2
SOD
PETEOS
Cu1
SiC seal layer
SOD
PSG
tungsten
poly-Si gate
SiN barrier layer
CoSi2
USG
n-Si
n-Si
p-well
USG
p-Si
p-Si
n-well
STI
spacer
buried SiO2
p-silicon wafer

IC Manufacturing

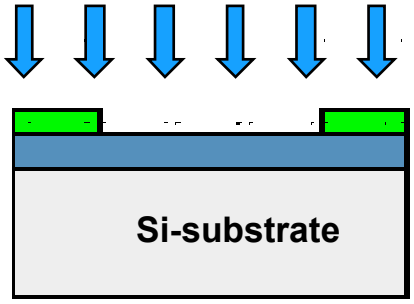
(a) Silicon base material



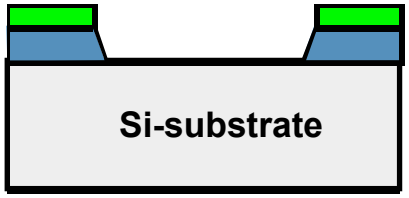
(b) After oxidation and deposition of negative photoresist



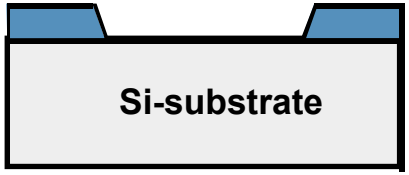
(c) Stepper exposure



(d) After development and etching of resist, chemical or plasma etch of SiO_2

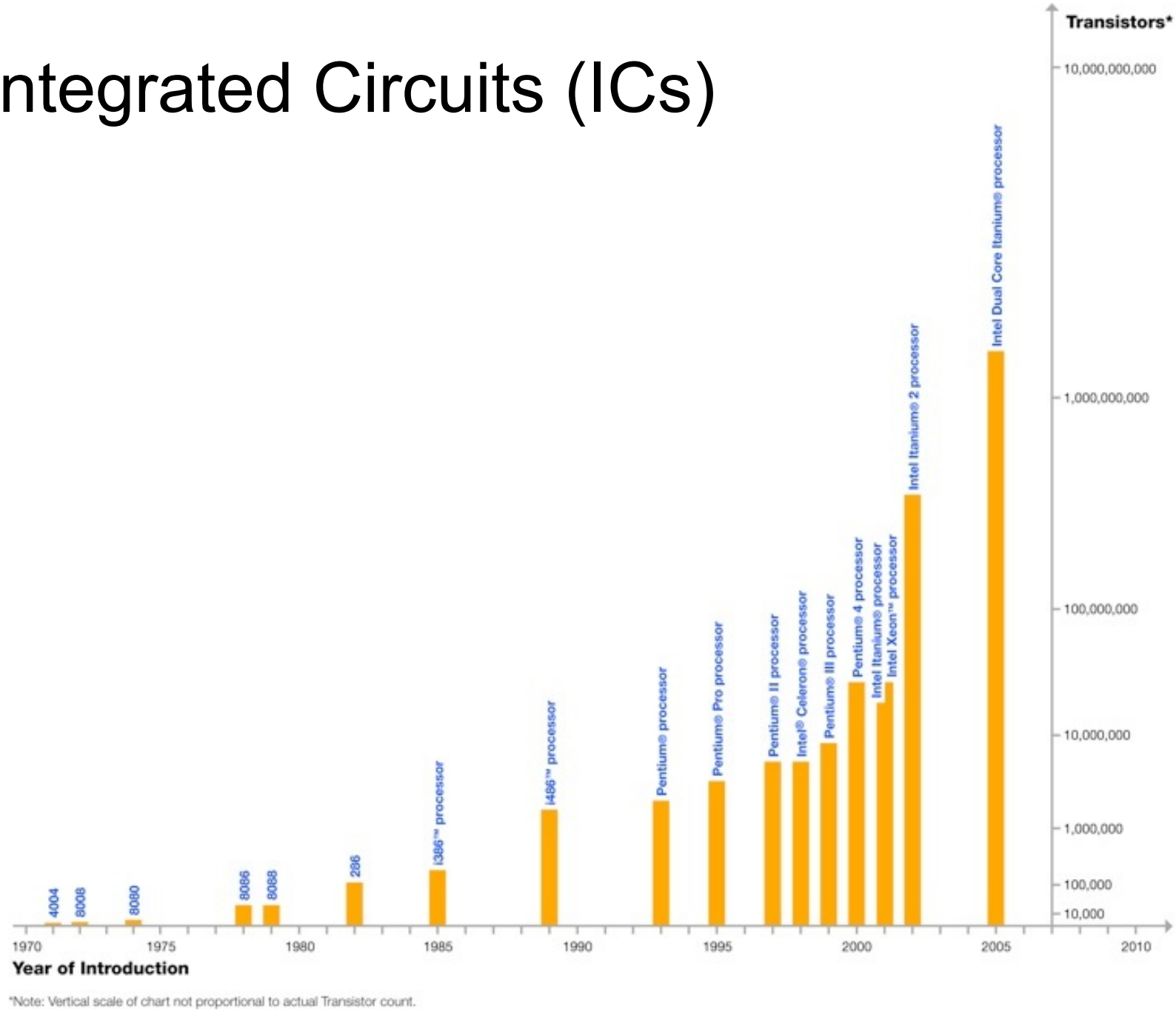


(e) After etching



(f) Final result after removal of resist

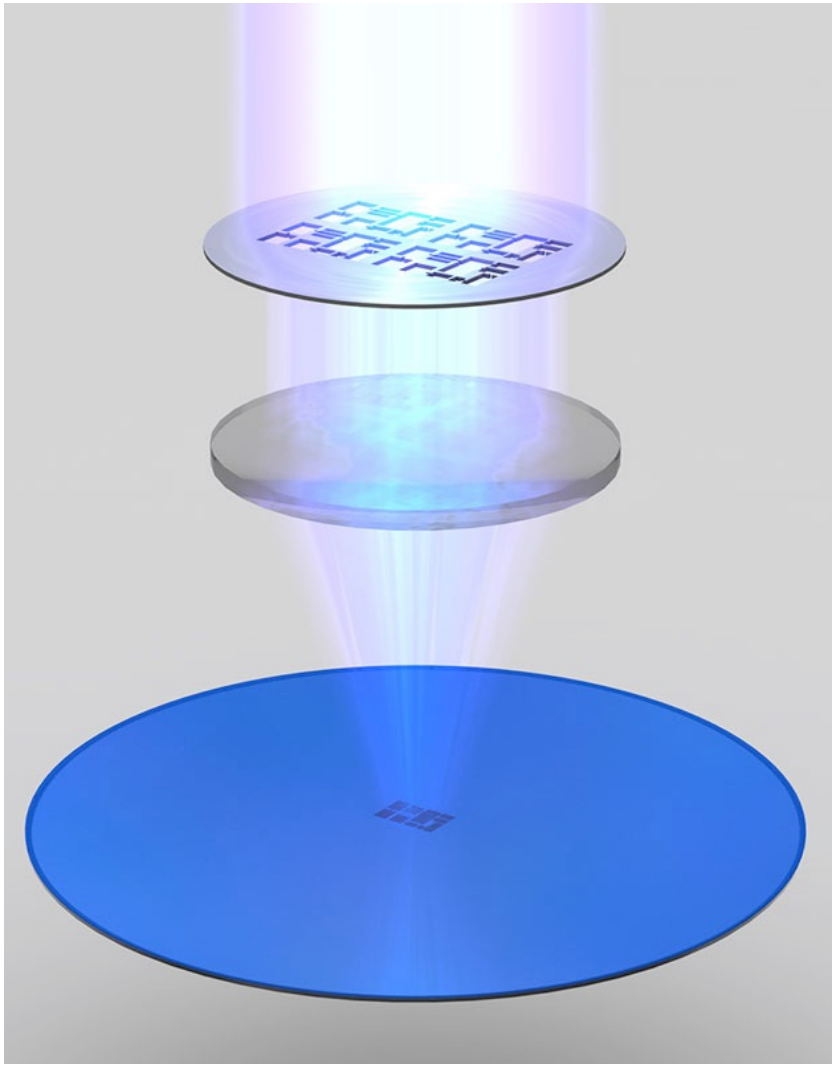
Integrated Circuits (ICs)



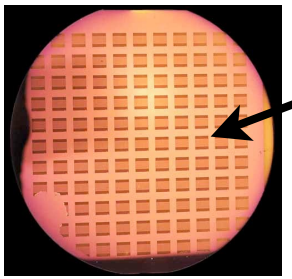
*Note: Vertical scale of chart not proportional to actual Transistor count.

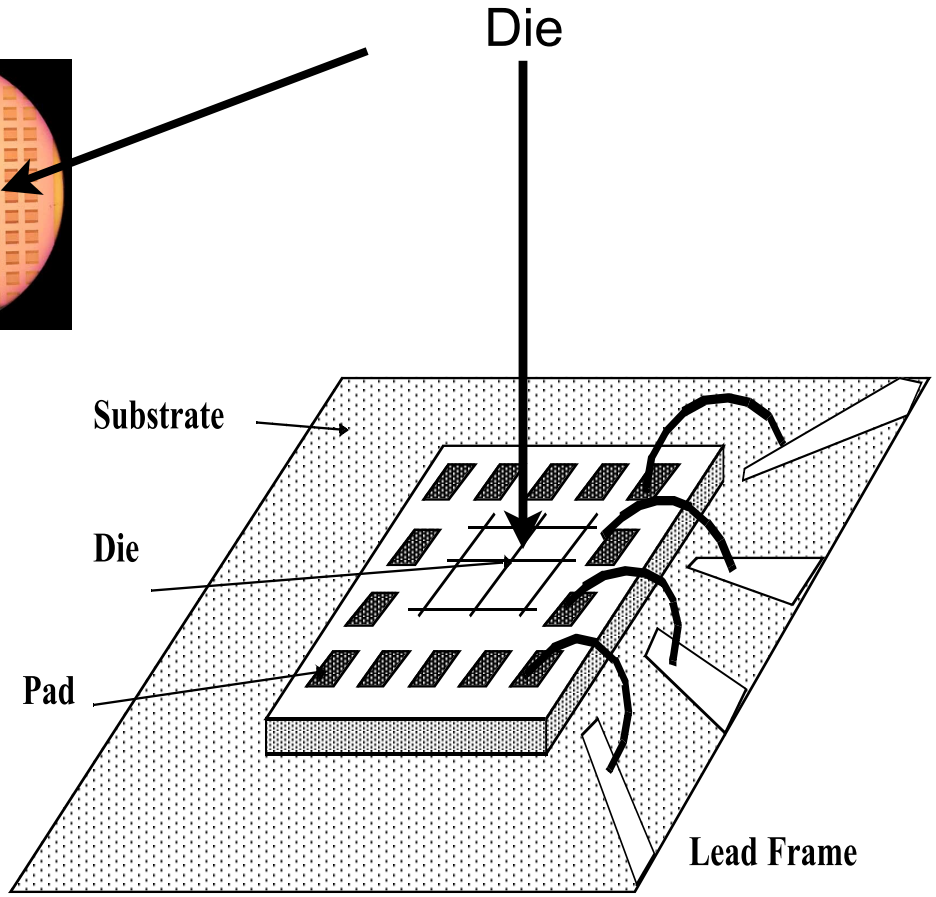
IC Manufacturing

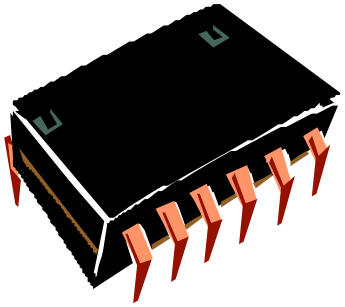
- The cost to set up a modern 45 nm process is $200–500 million
- The purchase price of a photomask can range from $1,000 to $100,000 for a single mask.
- As many as 30 masks (of varying price) may be required to form a complete mask set.



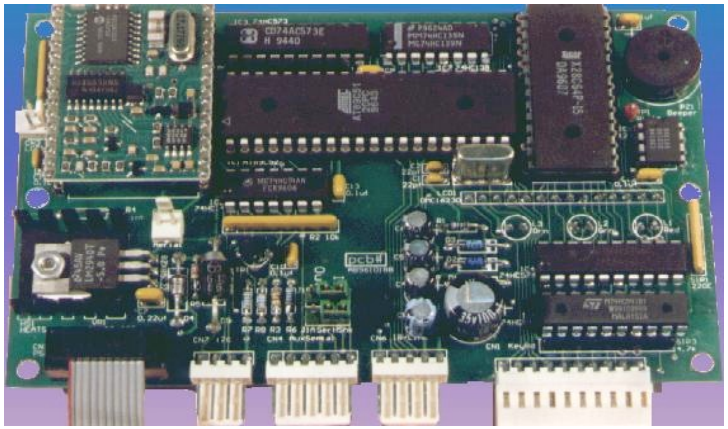
Bonding Techniques

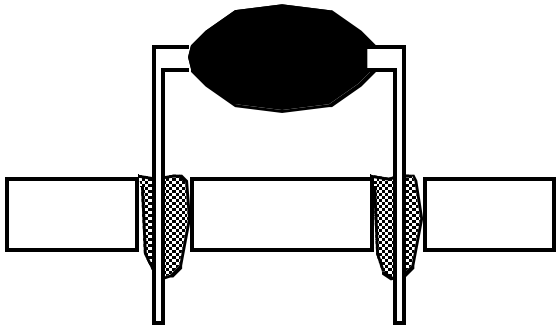




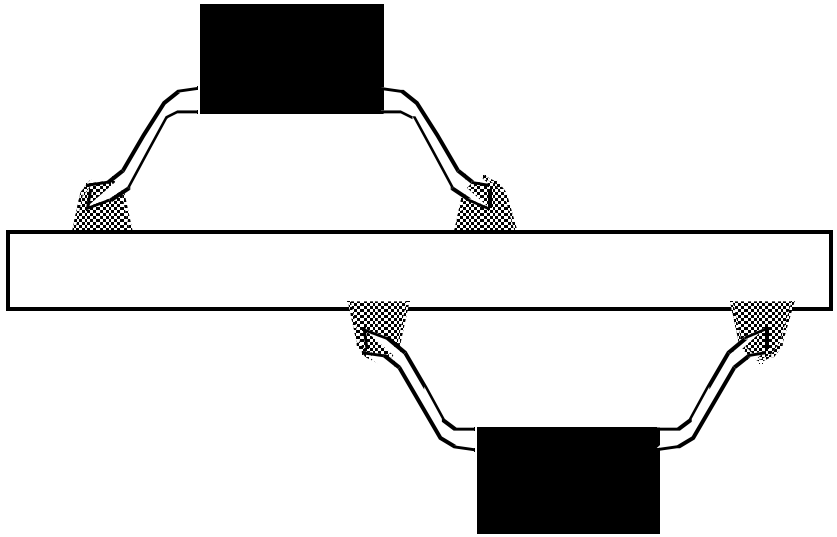


Package-to-Board Interconnect





(a) Through-Hole Mounting



(b) Surface Mount

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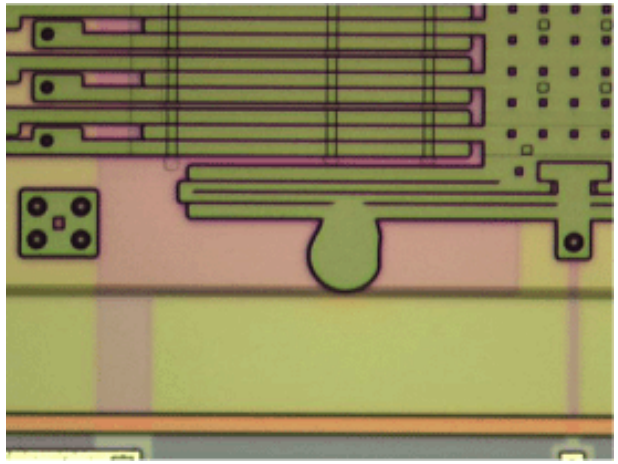
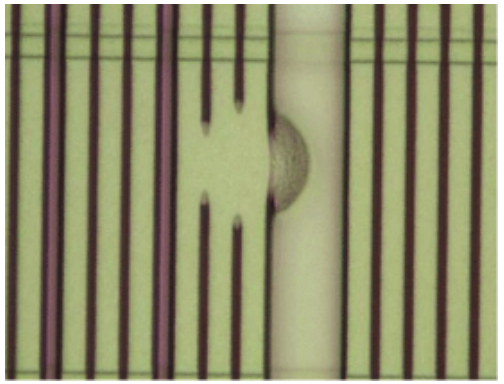
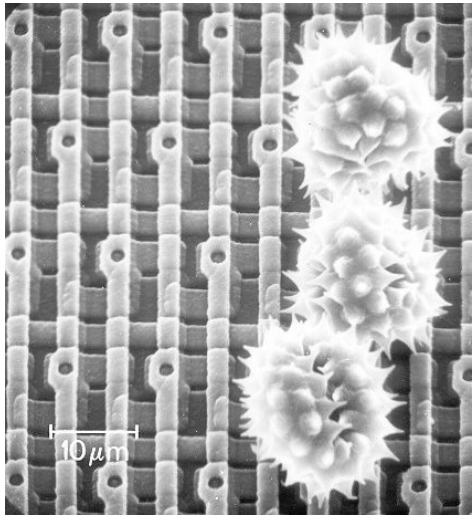
IC Defects

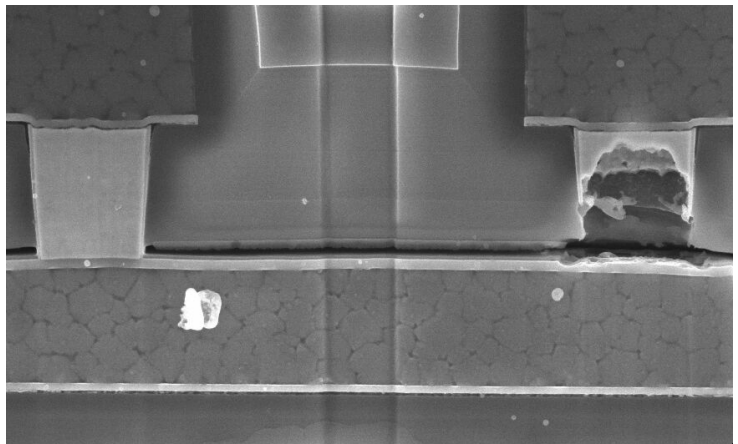




Seed



Salt

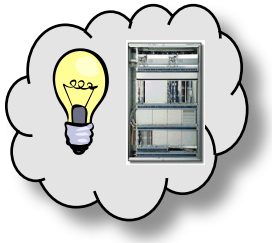


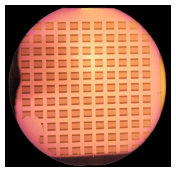
PCB Defects

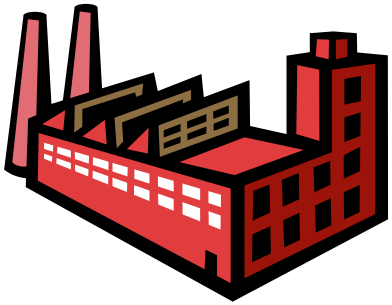
Defect classes	Occurrence frequency (%)
Shorts	51
Opens	1
Missing components	6
Wrong components	13
Reversed components	6
Bent leads	8
Analog specifications	5
Digital logic	5
Performance (timing)	5

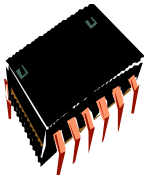
Ref.: J. Bateson, *In-Circuit Testing*, Van Nostrand Reinhold, 1985.

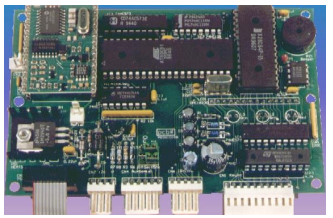
Making Fault Free Electronic Products

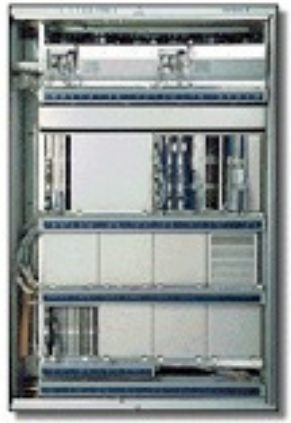












Development

Production

In-Field

Improve design

Improve production

Costumer returns!

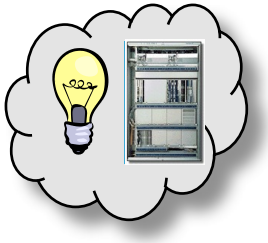
Problem?

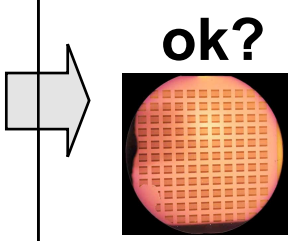
- No Trouble Found (NTF) is when a product fails in operation but when taken to a repair-shop no problem can be found
- NTF is according to Accenture Report, in 2008 in US, around 70% of all product returns. Cost-wise, NTF amounted up to 50% of total 13.8 billion USD (10.5 billion EUR) returns and repairs cost in US, which approximates to 25 USD (19 EUR/170 SEK) per year per capita
  - Translating to Sweden: Annual cost becomes 1700 000 000 (1.7 miljarder) SEK
- The International Technology Roadmap for Semiconductors (ITRS), 2012, lists ageing in semiconductor devices as one of the few most difficult challenges of process integration that affects reliability.

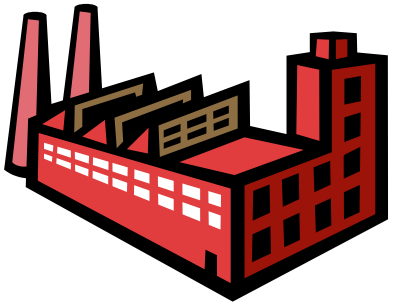
Future challenges

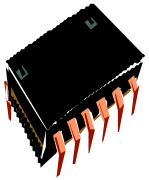
Late 20	**The New Reality**
Moore's Law — 2× transistors/chip every 18-24 months	Transistor count still 2× every 18-24 months, but see below
Dennard Scaling — near-constant power/chip	Gone. Not viable for power/chip to double (with 2× transistors/chip growth)
The modest levels of transistor unreliability easily hidden (e.g., via error correction)	Transistor reliability worsening, no longer easy to hide
Focus on computation over communication	Restricted inter-chip, inter-device, inter-machine communication; communication more expensive than computation
One-time (non-recurring engineering) costs growing, but amortizable for mass- market parts	Expensive to design, verify, fabricate, and test, especially for specialized-market platforms

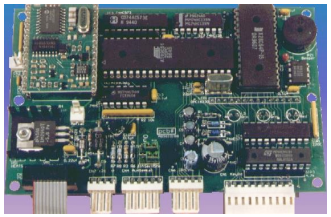
Making Fault Free Electronic Products

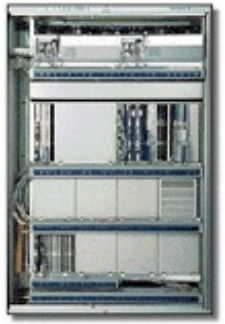












Test Preparation

Improve design

Production Test

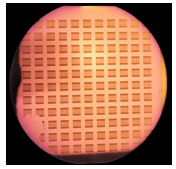
Improve production

In-Field Test

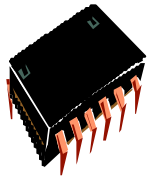
Costumer returns!

Types of Test

- Wafer sort - tests the logic of each die on the wafer



- Final test - tests the logic of each packaged IC

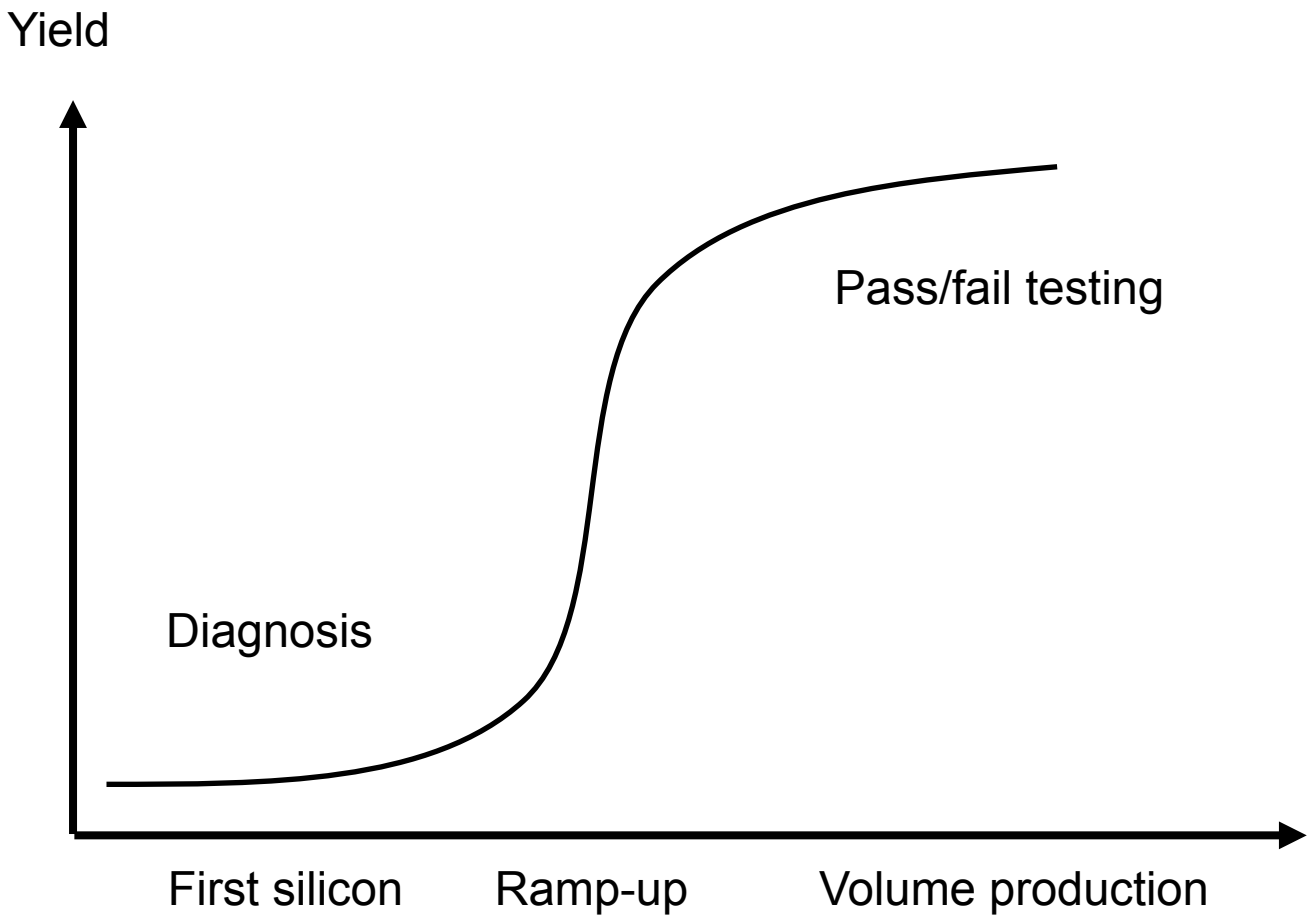


- Board test - tests interconnections (soldering errors)

Verification, Test and Diagnosis

- Verification is to verify the correctness of the design. It is performed through simulation, hardware emulation, or formal methods. It is performed once prior to manufacturing. Responsible for quality of design.
- Test verifies the correctness of manufactured hardware. Test is a two-part process:
  - Test generation: software process executed once during design, and
  - Test application: electrical tests applied to hardware. Test application performed on every manufactured device. Responsible for quality of devices.
- Diagnosis: Identification of a specific fault that is present.

Diagnosis and Volume Production



Tests

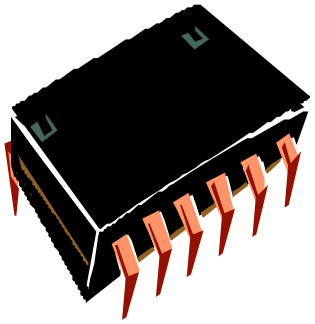
- Good IC that pass test -> OK
  Bad IC that fail test -> OK

- Bad ICs that pass test -> test escape
  Good ICs that fail test -> yield loss

		Outcome of test	
		Pass	Fail
IC	Good	OK	Yield loss
	Bad	Test esc.	OK

Test

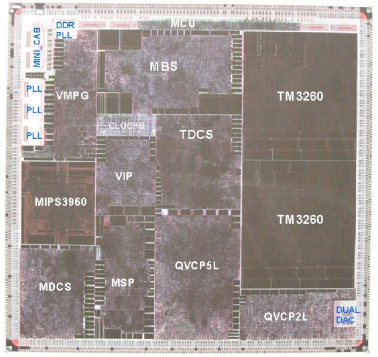
Device under test (DUT)

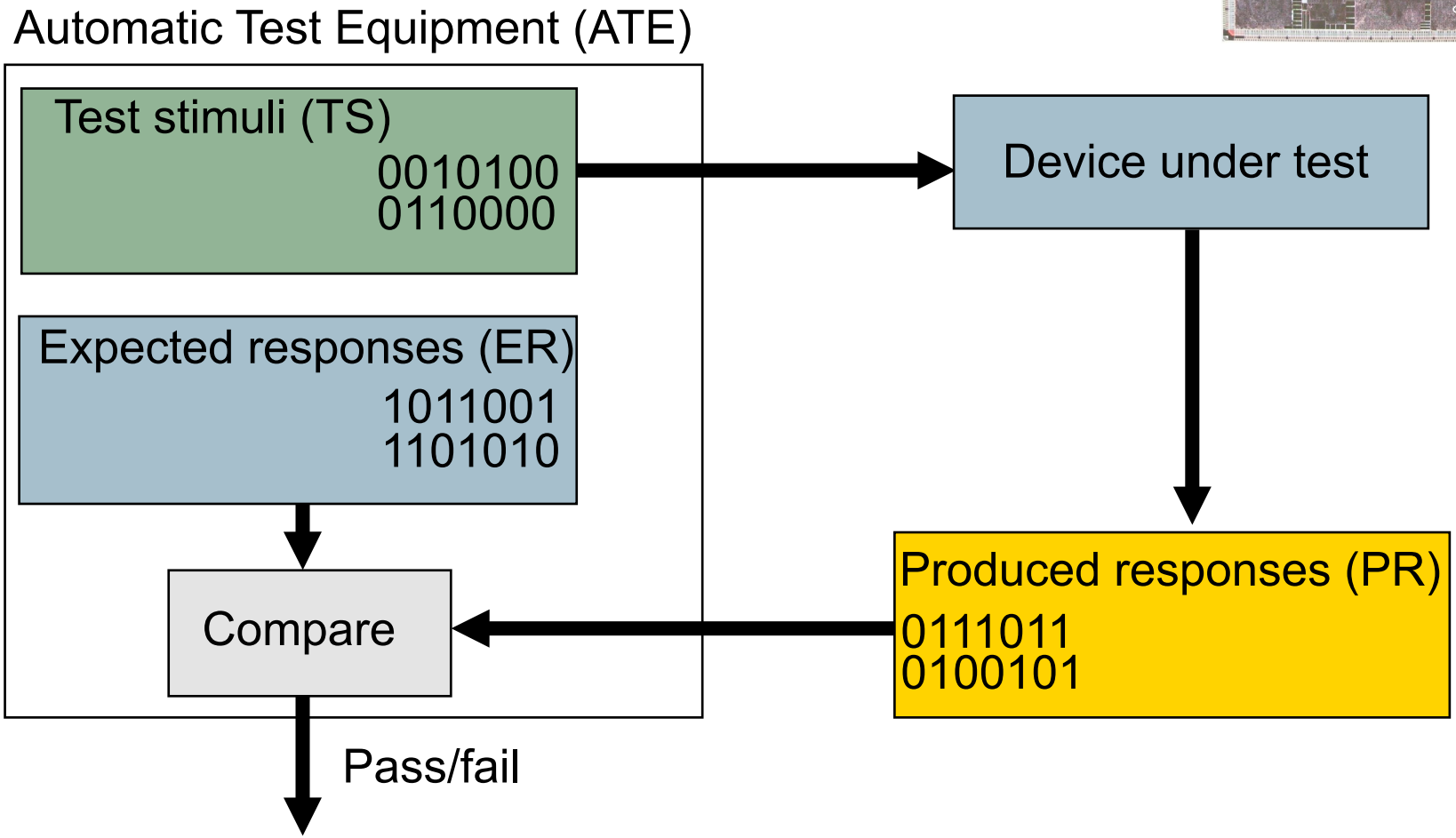
Stimulus →  → Response

Stimulus: test vectors

Test pattern: test vector + expected test response
Produced test response is compared against expected test response

Automatic Test Equipment (ATE)





Automatic Test Equipment (ATE)

- Consists of:
  - Powerful computer
  - Powerful 32-bit Digital Signal Processor (DSP) for analog testing
  - Test Program (written in high-level language) running on the computer
  - Probe Head (actually touches the bare or packaged chip to perform fault detection experiments)
  - Probe Card or Membrane Probe (contains electronics to measure signals on chip pin or pad)

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ADVANTEST

VERIGY

Objective with Test

- Specify the test vector
- Determine correct response (expected response)
- Evaluate cost of test (# patterns related to cost)
- Evaluate quality of test

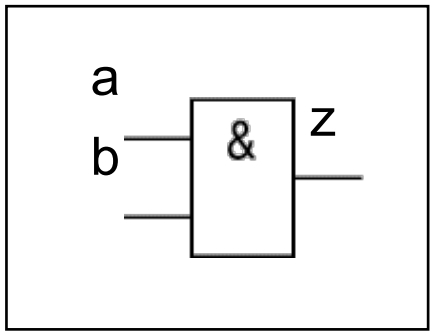
- Fault coverage = No of faults detected / No. faults modeled
- Yield = Number of good parts / Total number of tested parts

Outline

- Electronics
- Manufacturing
- Test, diagnosis, and verification
- Test generation

Exhaustive Test Generation

- Try all possible alternatives.
- For a 2-input design, 2^2 (4 vectors are needed).



a	b	z
0	0	0
0	1	0
1	0	0
1	1	1

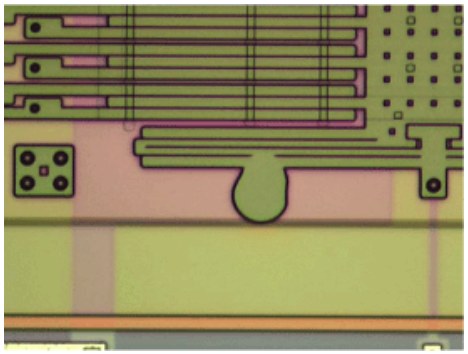
- For a 30-input pin design, 2^{30} (1073741824 vectors are needed)
- 1 vectors per second and we know that there are 60*60*24*365=31536000 seconds in a year
- 2^{30} / 31536000 = 34 years

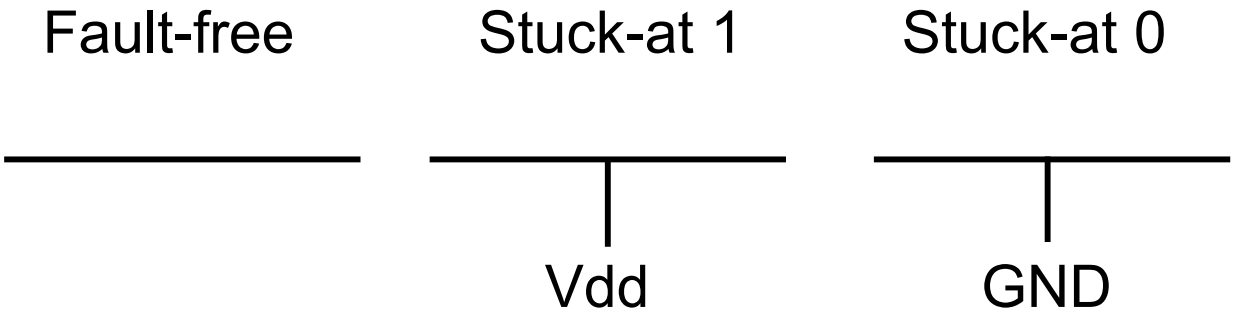
Defects, Faults, and Fault Models

- Real defects too numerous and often not analyzable
- A fault model
  - identifies targets for testing
  - makes analysis possible
- A defect manifests itself as a fault
- A fault is modeled by a fault model
- Example of fault models:
  - Stuck-at Fault, Bridging Fault, Shorts (Resistive shorts), Opens, Delay Faults, Transient Fault
- So far stuck-at fault model is the most used one:
  - Motivations: Simple and covers quite well possible defects

Defects, Faults and Fault Models

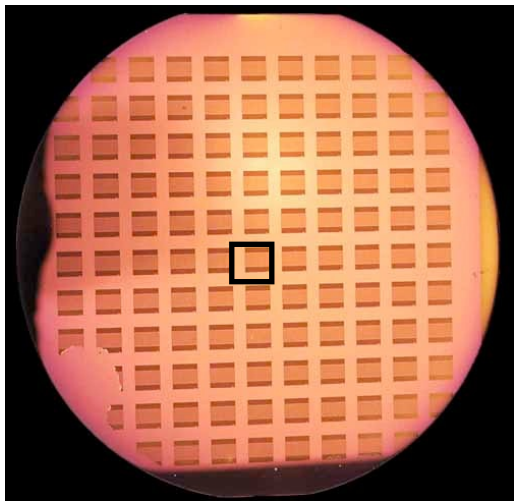
- Example of a defect

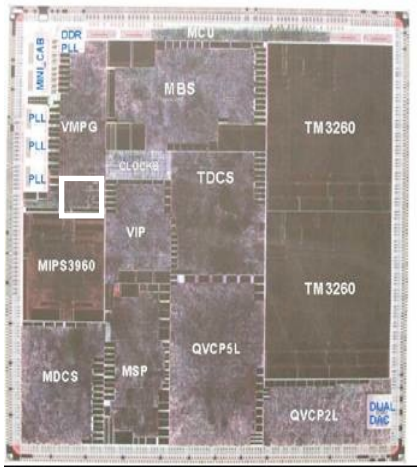


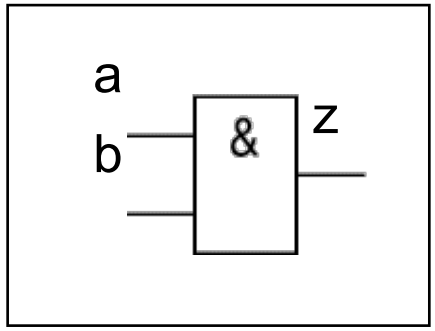


- A defect manifests itself as a fault
- A fault is modeled with a fault model

Test generation





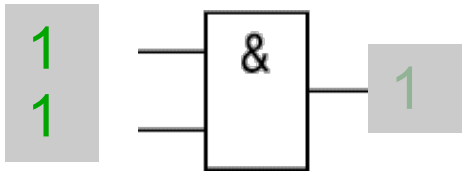


a	b	z
0	0	0
0	1	0
1	0	0
1	1	1

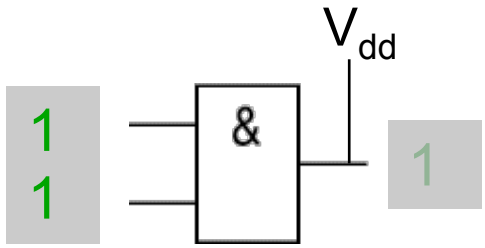
Test generation

Example: Create test for output connected to V_{dd}

Fault-free



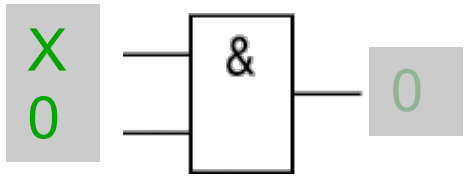
Faulty



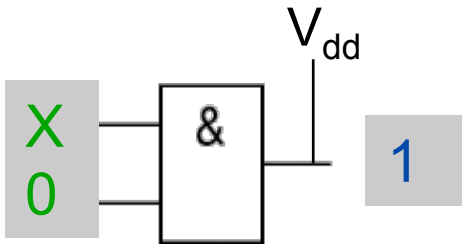
Test generation

Example: Create test for output connected to V_{dd}

Fault-free

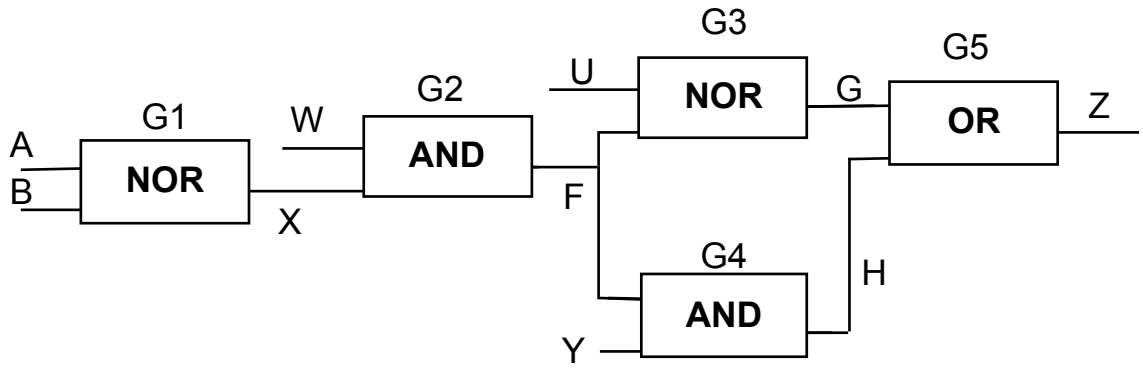


Faulty



Stuck-at Fault (SAF) Model

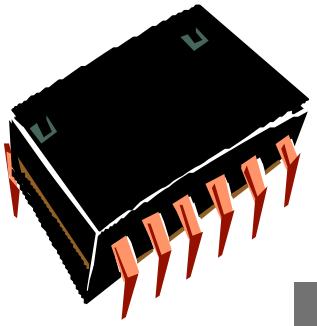
- A line is fixed to logic value 0 (stuck-at-0) or 1 (stuck-at-1)
- For the stuck-at fault model there are for a circuit with n lines 2*n possible faults

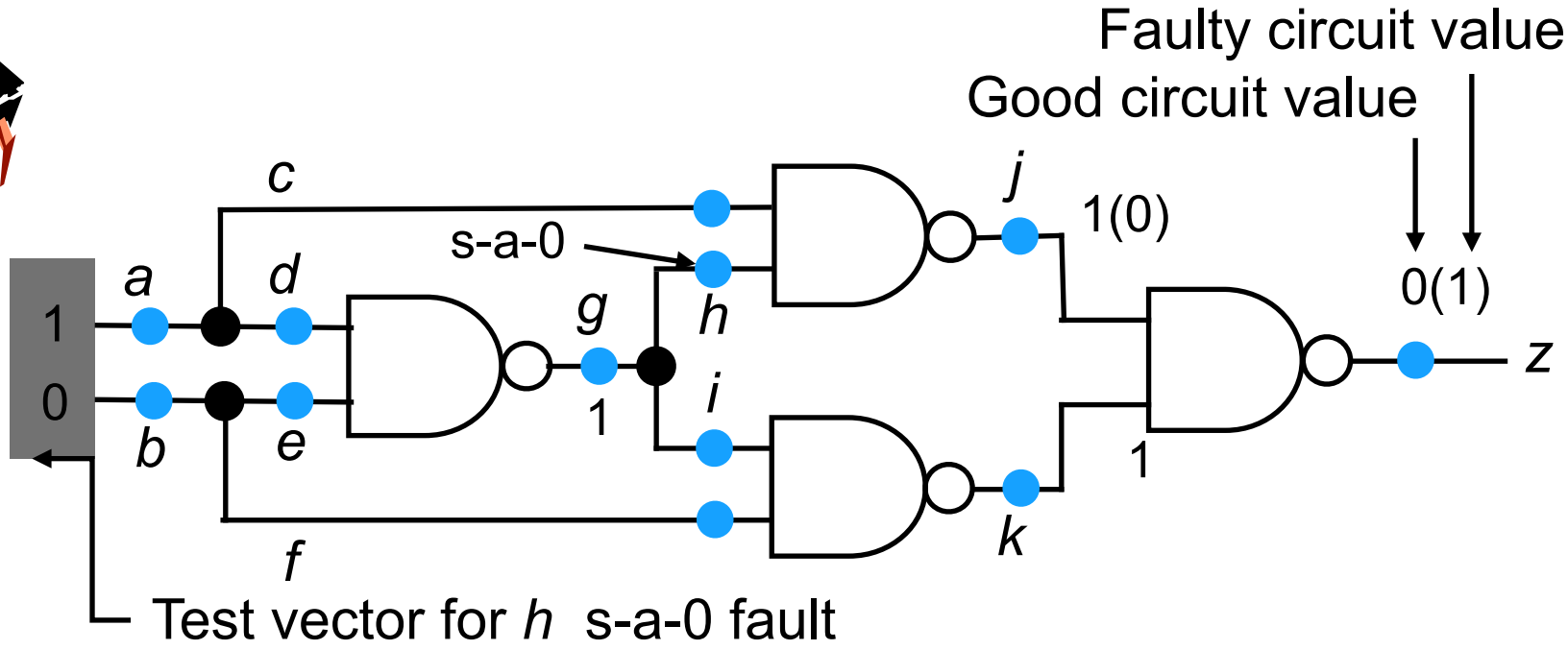


- Quality of a test is given by:
  fault coverage = faults detected / total number of faults
- Example: 12 lines (24 faults) detect 15 faults: f.c.=15/24 (63%)

Single Stuck-at Fault

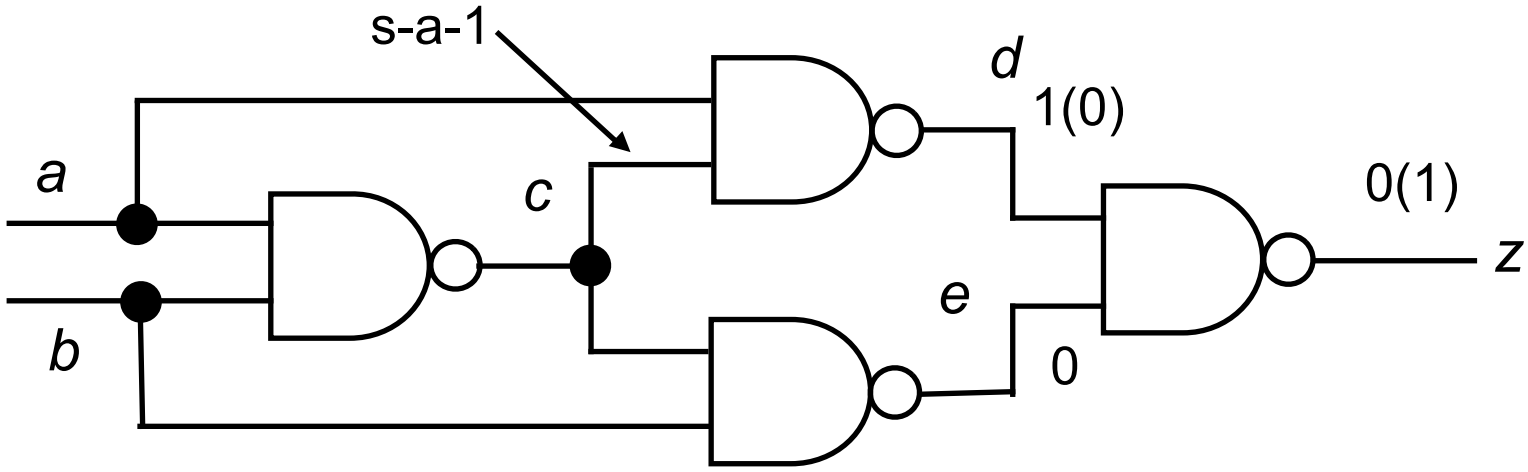
- Three properties define a single stuck-at fault
  - Only one line is faulty
  - The faulty line is permanently set to 0 or 1
  - The fault can be at an input or output of a gate
- Example has 12 fault sites (●) and 24 single stuck-at faults





Single Stuck-at Fault

- Let us generate a s-a-1 on the same line
- To get c=0, set a=1 and b=1
- To get fault effect on d (1/0), set a=1
- To get fault effect on z (0/1), set e=0
- To get e=0, set b=1 and c=1 (but c=0 - see above)



Deterministic Test Generation

While fault coverage < desired limit {

Select an uncovered fault f

Generate test for the fault f

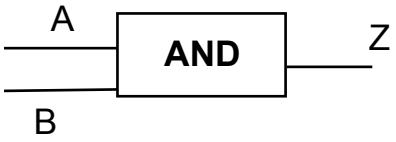
Evaluate fault coverage

}

- Needed functions to generate a test:
  - Excite (provoke) the fault
  - Sensitize (propagate) the results to primary outputs
  - Justify other values in the circuit
- ATPG:
  - D-algorithm
  - Path-Oriented Decision-Making (PODEM)
  - Fanout-oriented Test Generation (FAN)
  - Structure-oriented cost-reducing automatic test pattern generation (SOCRATES)

D-notation

- Five-valued algebra (0,1,X,D,D')
  - D=1/0
  - D'=0/1

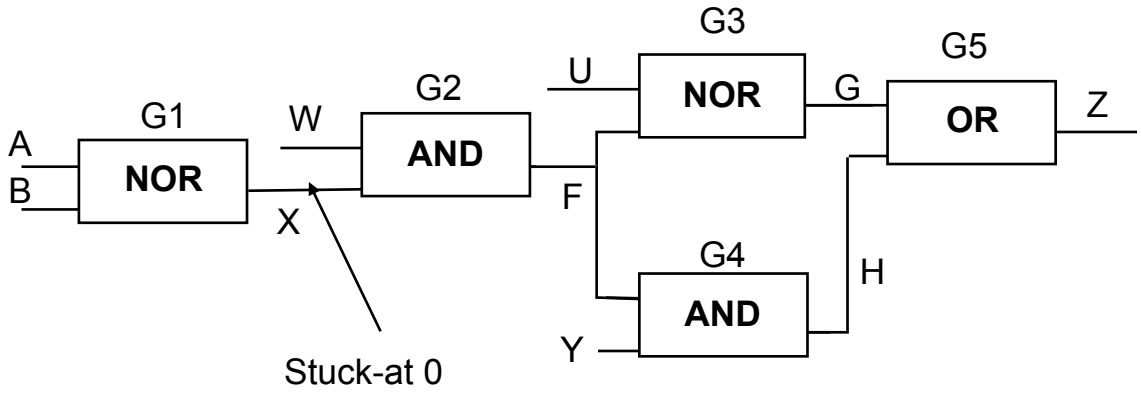


- Stuck-at 0 on A ->
- Line A = D
- To propagate D (fault effect) to Z (check table) set B=1

OR	0	1	D	D'	X
0	0	1	D	D'	X
1	1	1	1	1	1
D	D	1	D	1	X
D'	D'	1	1	D'	X
X	X	1	X	X	X

AND	0	1	D	D'	X
0	0	0	0	0	0
1	0	1	D	D'	X
D	0	D	D	0	X
D'	0	D'	0	D'	X
X	0	X	X	X	X

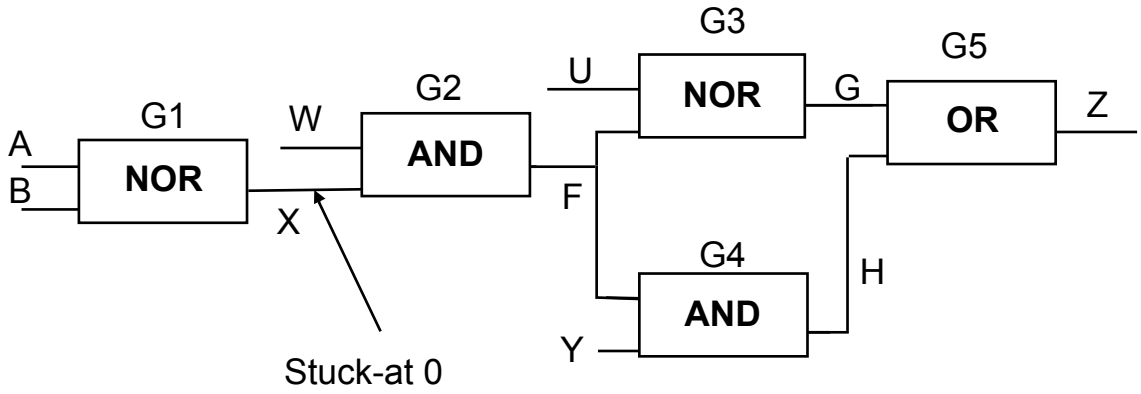
D-Algorithm



- Initialize the circuit by placing X on each line
- For a SA0, X=D and A=B=0 (for the selected fault)
- Propagate D through G2
- Select a sensitizing path (we select G3)
- To propagate through G3, we let U=0
- Propagate through G5
- Reached a primary output with D
- Justify values on H, Y, U, W. H=0 (ok). F=0? Conflict! Select Y=0

D-Algorithm

- D=1/0



1	Operation	Gate	A	B	X	Y	W	U	F	G	H	Z
2	Initialization		x	x	x	x	x	x	x	x	x	x
3	Provoke	G1	0	0	D	x	x	x	x	x	x	x
4	D-drive	G2	0	0	D	x	1	x	D	x	x	x
5	D-drive	G3	0	0	D	x	1	0	D	D’	x	x
6	D-drive	G5	0	0	D	x	1	0	D	D’	0	D’
7	Justification	H=0	0	0	D	x	1	0	!	D’	0	D’
8	Justification	H=0	0	0	D	0	1	0	D	D’	0	D’

Commercial ATPG Tools

- Commercial ATPG tools are often for combinational circuits
- Commercial tools usually make use of a random test generation for 60-80% of the faults (easy to detect) and deterministic test generation for the remaining part (hard to detect)
- Examples of commercial ATPG tools:
  - Encounter Test - Cadence
  - TetraMax - Synopsis
  - FastScan, FlexTest - Mentor Graphics

Introduction to structured VLSI design

Design for Test (DfT) - Part 1

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