

EITF35: Introduction to Structured VLSI Design

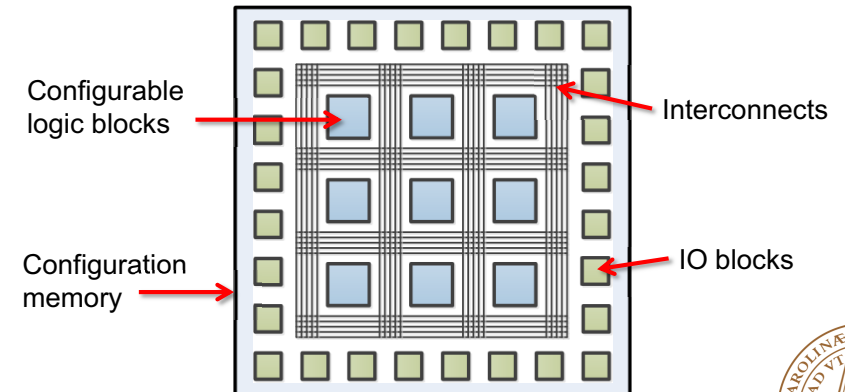
Introduction to FPGA design

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WWW.FPGA

- What is FPGA?
 - Field Programmable Gate Array



WWW.FPGA

- What is FPGA?
 - Field Programmable Gate Array
 - Configurable logic blocks + interconnects + IOs + memory
- Why do we use it?
 - High performance & Flexible
 - Shorter time to market
- Where do we use it?
 - Prototyping
 - Computer vision
 - Medical imaging
 - Software-defined radio
 - ...



FPGA vs. Microprocessor

	Intel Itanium 2	Xilinx Virtex-II Pro (XC2VP100)
Technology	0.13 μm	0.13 μm
Clock speed	1.6 GHz	180 MHz
Internal memory bandwidth	102 GBytes/S	7.5 TBytes/S
# Processing units	5 FPU (2 MACs+1 FPU) 6 MMU 6 Integer units	212 FPU or 300+Integer units or ...
Power consumption	130 W	15 W
Peak performance	8 GFLOPs	38 GFLOPs
Sustained performance	~2GFLOPs	~19 GFLOPs
IO/External memory bandwidth	6.4 GBytes/S	67 GBytes/S

(Courtesy: Nallatech)



FPGA devices

- Manufacturers:

- **Xilinx:** Spartan, Kintex, Virtex
- **Altera:** Cyclone, Arria, Stratix
- Lattice Semiconductor: flash, low power
- Microsemi (Actel): antifuse, mix-signal
- Achronix: high speed
- QuickLogic: application-specific (handheld)



Some FPGA boards

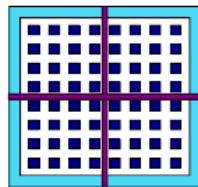
- ERICSSON F500
- Xilinx Virtex-5 OpenSPARC Evaluation Platform
<http://www.digilentinc.com/Products/Detail.cfm?NavPath=2,400,795&Prod=XUPV5>
- Xilinx Virtex-II Pro Development System
<http://www.digilentinc.com/Products/Detail.cfm?NavPath=2,400,794&Prod=XUPV2P>
- **We use Xilinx Spartan-3 board in this course!**
<http://www.digilentinc.com/Products/Detail.cfm?NavPath=2,400,519&Prod=S3BOARD>



FPGA architectures

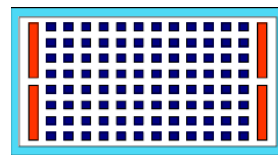
- Early FPGAs

- N x N array of unit cells (CLB + routing)
- Special routing along center axis



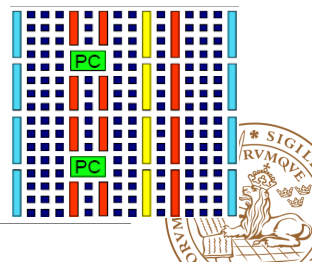
- Next Generation FPGAs

- M x N unit cells
- Small block RAMs around edges



- More recent FPGAs

- Added block RAM arrays
- Added multiplier cores
- Added processor cores



FPGA architecture trends

- Memories
 - Single & Dual-port RAMS
- Digital Signal Processor Engines
- Embedded Processors
 - Hardcore (dedicated processors)
 - Soft core (synthesized from a HDL)
- High speed/performance I/O connectivity
 - PCIe interface block
 - I/O transceiver
- Clock management blocks



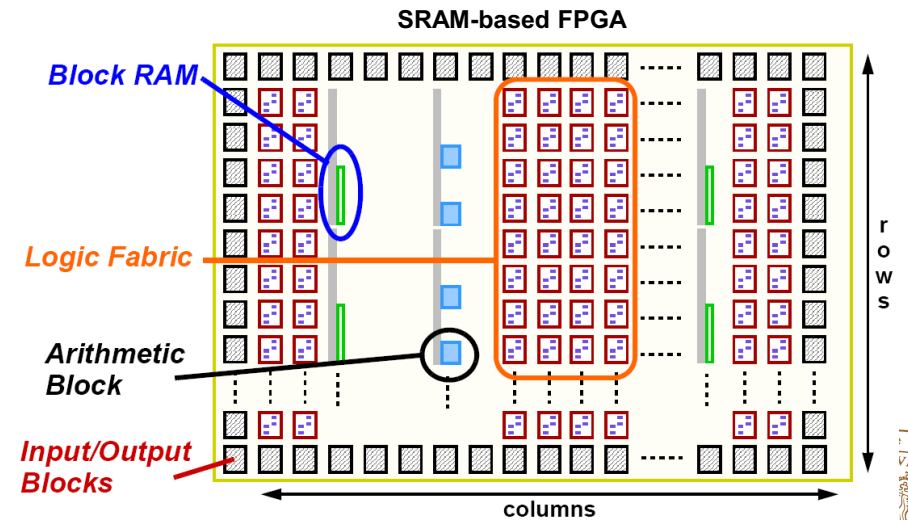
Programming technology

Feature	SRAM	Antifuse	Flash/E2PROM
Technology	State-of-the-art	One or more generations behind	One or more generations behind
Reprogrammable	Yes (in system)	No	Yes (in system or offline)
Reprogramming speed	Fast	---	3x slower than SRAM
Volatile	Yes	No	No
Instant-on	No	Yes	Yes
Security	Acceptable	Very Good	Very Good
Size of Config. Cell	Large (Six transistors)	Very small	Medium-small (Two transistors)
Power consumption	Medium	Low	Medium

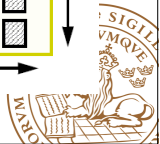
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Xilinx FPGA architecture (Spartan-3)

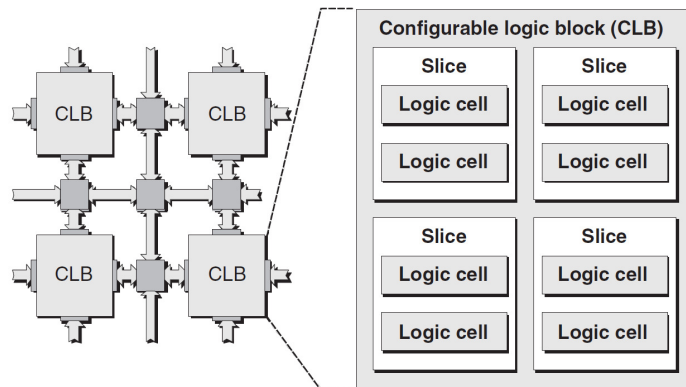


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Configurable logic block (CLB) (I)

- One CLB contains four slices

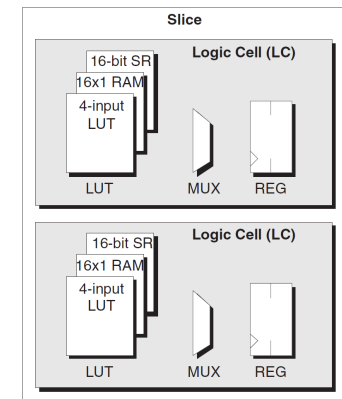


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Configurable logic block (CLB) (II)

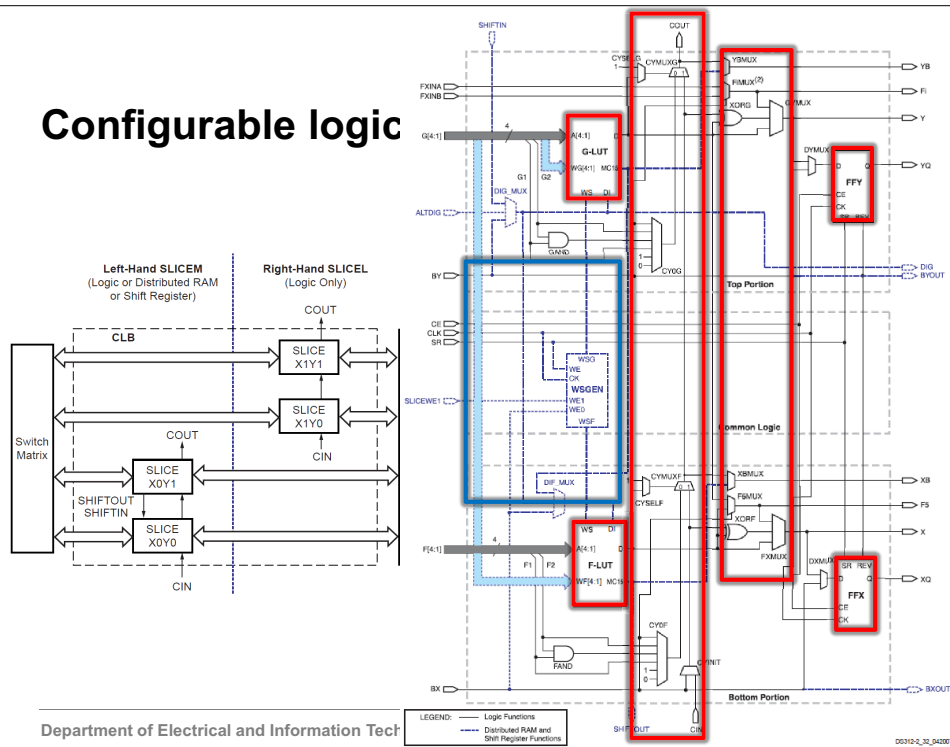
- One CLB contains four slices
- Each slice:
 - Two Look-up tables (LUTs)
 - Two D Flip-Flops (DFFs)
 - Multiplexers and arithmetic gates
 - Carry logic
- Left-hand slice (SLICEM)
 - Distributed RAM
 - Shift register



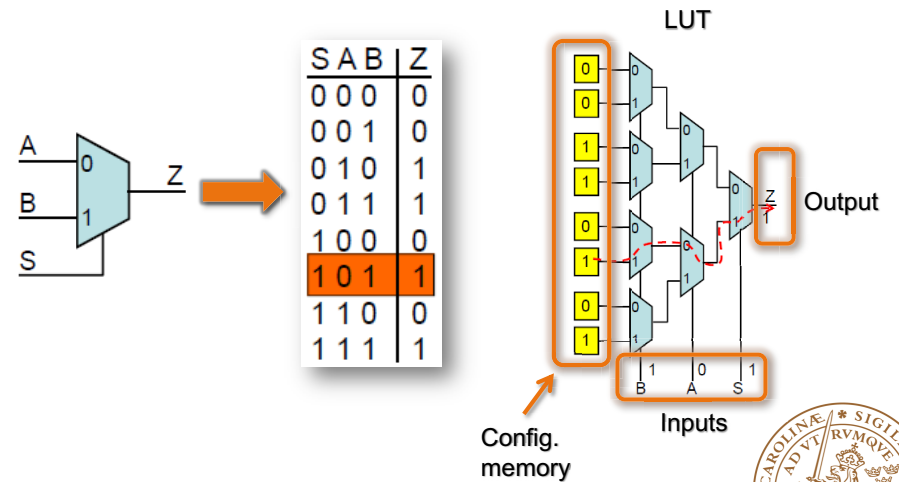
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Configurable logic

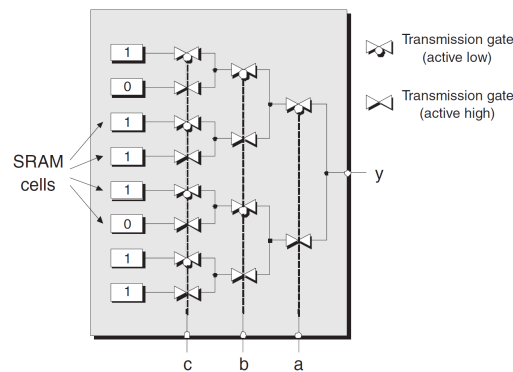


Look-up table (LUT) (I)



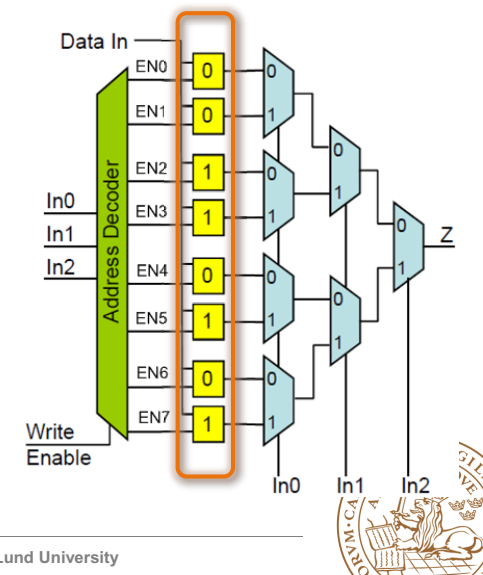
Look-up table (LUT) (II)

- Inputs are used as a pointer into a LUT.
- Decoded using a hierarchy of transmission-gate MUXs.
- Transmission-gate: “pass” or “high-impedance”.



LUT based RAM (Distributed RAM)

- Normal LUT performs “read” operation.
- For “write” operation, address decoders + write enable.
- Can be concatenated to created larger RAMs.
- Can also be used as shift registers (some of the LUTs).



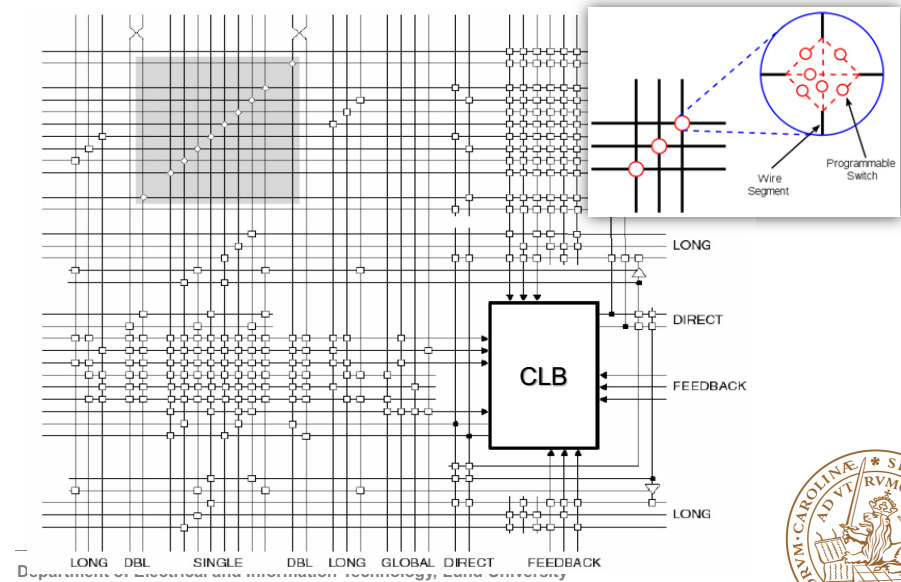
Xilinx Spartan-3 FPGAs

- XC3S200:
 - 480 CLBs = 480*4 Slices = 480*4*2*(4-input LUTs + registers)
 - 12 18-kbit dual-port BRAMs = 12*18 Kb = 216 Kbits
 - Distributed RAM: 480*2*2*2^4 = 30,720b = 20Kb (only 2 LUTs per slice)

Device	System Gates	Equivalent Logic Cells ¹	CLB Array (One CLB = Four Slices)			Distributed RAM Bits (K=1024)	Block RAM Bits (K=1024)	Dedicated Multipliers	DCMs	Maximum User I/O	Maximum Differential I/O Pairs
			Rows	Columns	Total CLBs						
XC3S50 ²	50K	1,728	16	12	192	12K	72K	4	2	124	56
XC3S200 ²	200K	4,320	24	20	480	30K	216K	12	4	173	76
XC3S400 ²	400K	8,064	32	28	896	56K	288K	16	4	264	116
XC3S1000 ²	1M	17,280	48	40	1,920	120K	432K	24	4	391	175
XC3S1500	1.5M	29,952	64	52	3,328	208K	576K	32	4	487	221
XC3S2000	2M	46,080	80	64	5,120	320K	720K	40	4	565	270
XC3S4000	4M	62,208	96	72	6,912	432K	1,728K	96	4	633	300
XC3S5000	5M	74,880	104	80	8,320	520K	1,872K	104	4	633	300

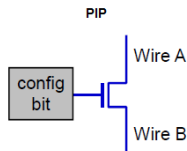
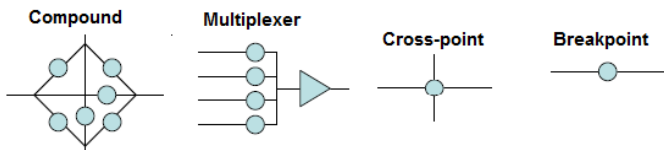
Notes:
 1. Logic Cell = 4-input Look-Up Table (LUT) plus a 'D' flip-flop. "Equivalent Logic Cells" equals "Total CLBs" x 8 Logic Cells/CLB x 1.125 effectiveness.
 2. These devices are available in Xilinx Automotive versions as described in [DS314](#): Spartan-3 Automotive XA FPGA Family.
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Programmable Interconnects (I)



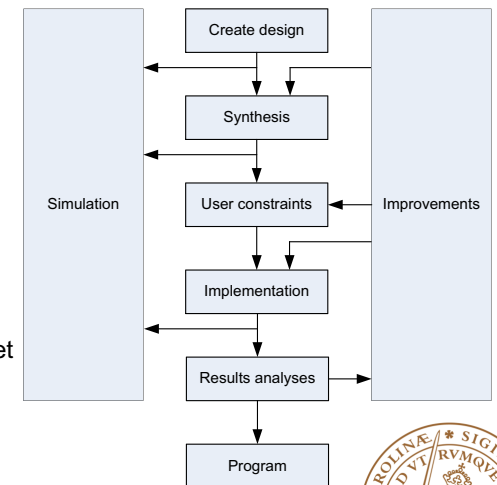
Programmable Interconnects (II)

- Programmable switch, also called programmable interconnect points (PIP).
- Implemented using transmission gates.
- Several types of PIPs:

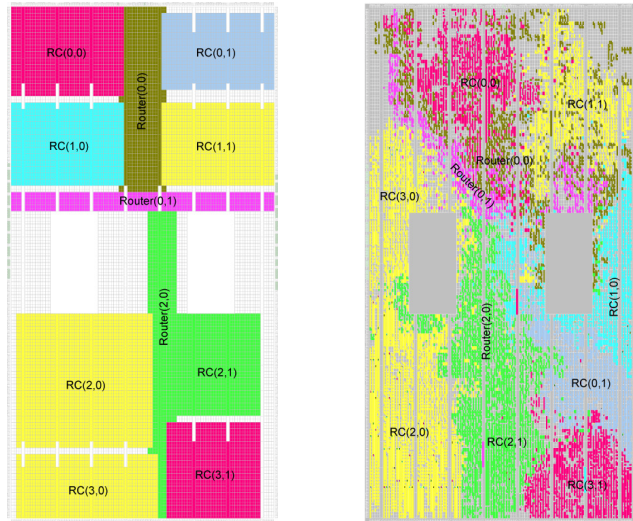


FPGA Design flow

- Synthesis
 - Parses HDL design
 - Infers Xilinx primitives
 - Generates design netlist
- Translate
 - Merges incoming netlists and constraints into a design file
- Map
 - Maps (places) design into the available resources on the target device
- Place and Route
 - Places and routes design



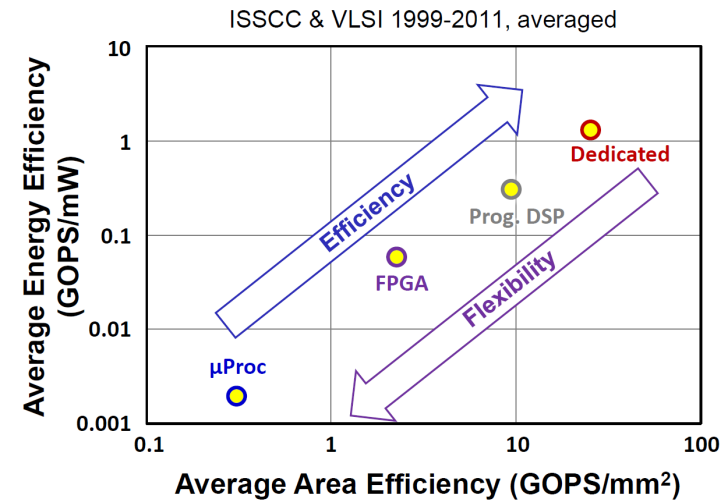
Synthesis constraints



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Are FPGAs perfect?

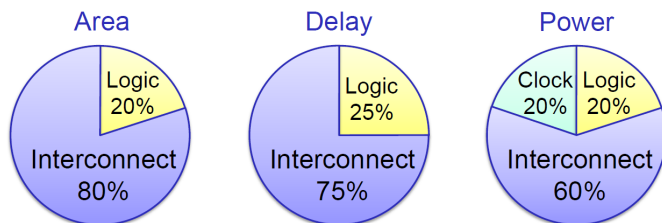


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FPGAs are inefficient

- Compared to ASICs, penalties in FPGAs:
 - Area: 17 – 54x
 - Speed: 3 – 7x
 - Power: 6 – 62x
- Main culprit: **INTERCONNECT!**

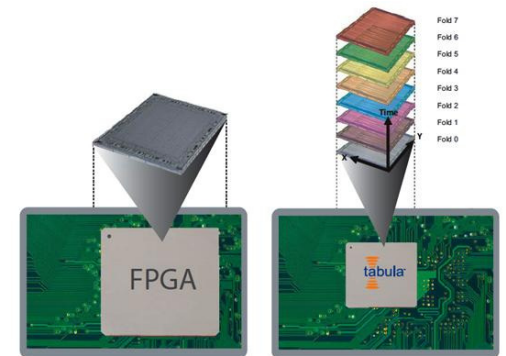


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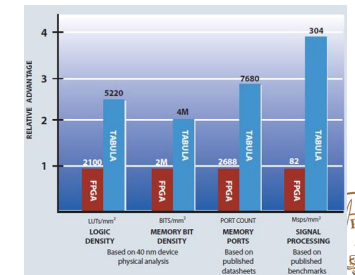


Tabula Spacetime

- Ultra-rapid full/partial reconfiguration with makes it possible to fold more functions onto the same hardware: multi-GHz rates
- Their claim:
 - 2.5x logic density
 - 3.7x DSP performance



www.tabula.com



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Coarse-grained reconfigurable architecture

- Currently in FPGA
 - Dedicated building blocks: multiplier, DSP core, processor
 - Partial configuration
- Moving towards coarse-grained architecture:
 - Block-level instead of bit manipulations
 - Lower area and power consumption
 - High-level programming: e.g. xilinx vivado
 - Run-time configuration



References

- Clive “Max” Maxfield, “The Design Warrior’s Guide to FPGAs – Devices, Tools and Flows”, ELSEVIER, 2004.
- Bill Jason P. Tomas, “Introduction to Field Programmable Gate Arrays (FPGAs)”.
- Xilinx, “Spartan-3 FPGA Family Data Sheet”.

