

# Introduction to Structured VLSI Design

## - 1-bit Adder FPGA Example

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# Purpose

Graphical guide the supplements ISE Quick Start

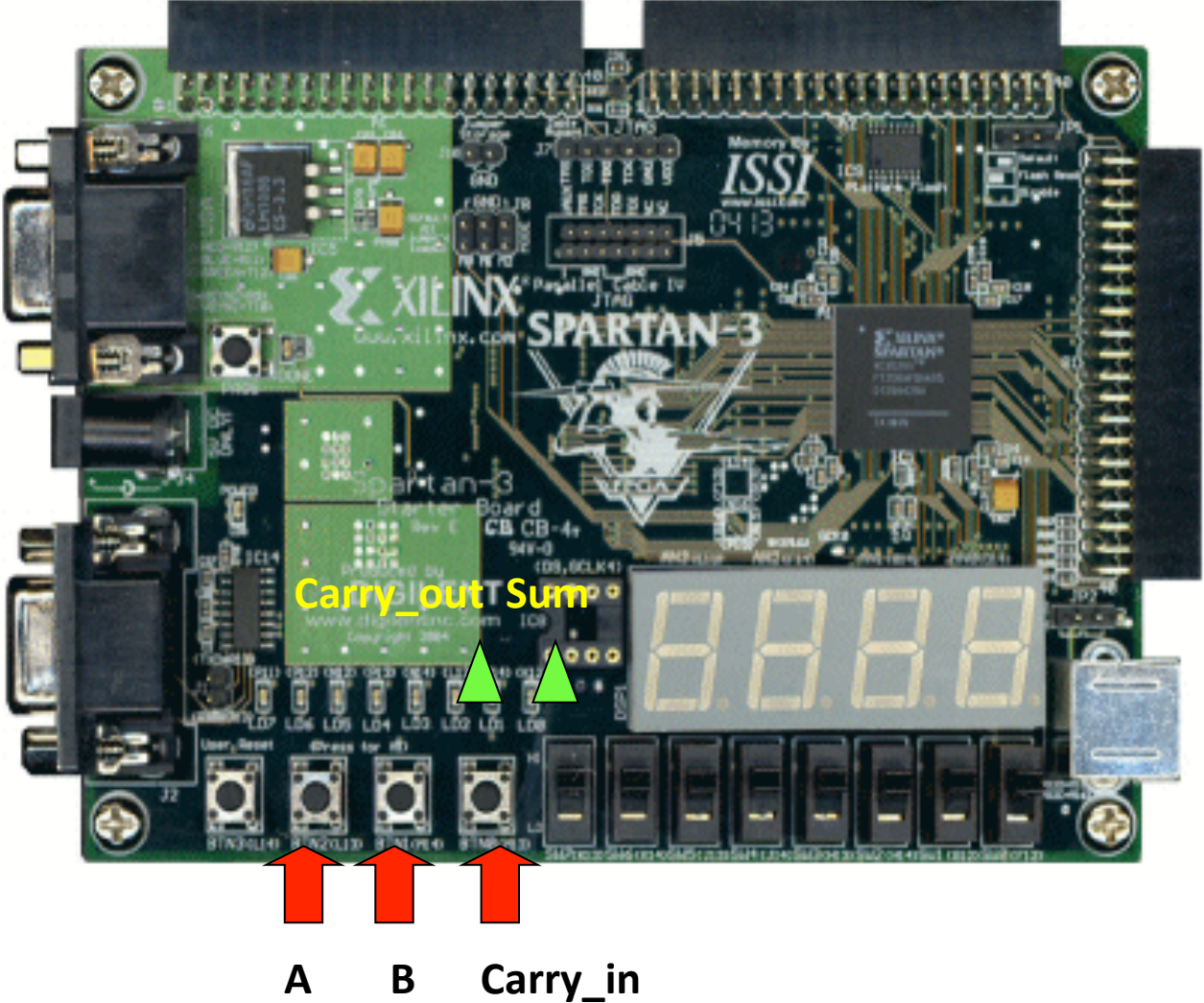
1-bit Full adder will be

- designed
- simulated in Modelsim
- synthesized (mapped)
- placed
- Programmed
- Executed

on a Spartan 3



# In Practice



# Get started

- Start XILINX ISE
- Select Help-> Tutorials-> ISE Quick Start
- Choose
  - File
  - New Projectand continue



# Device Properties

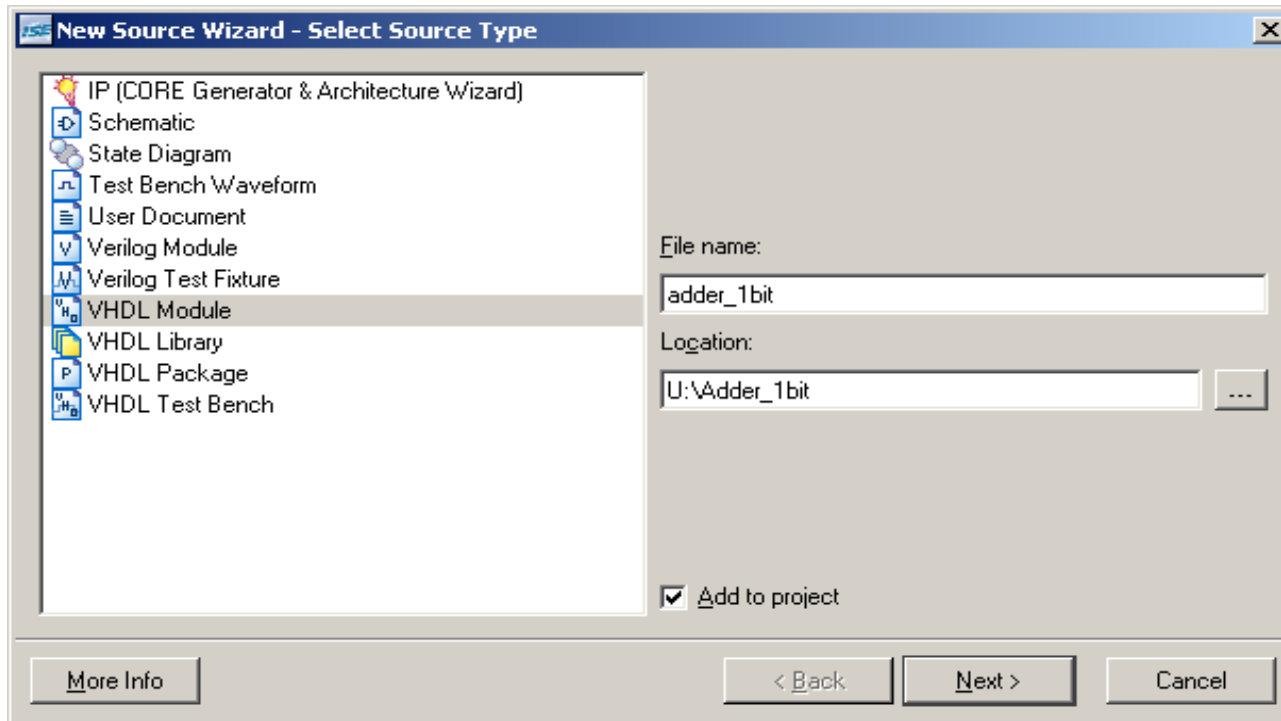
Property Name	Value
<b>Product Category</b>	All
Family	Spartan3
Device	XC3S200
Package	FT256
Speed	-4
Top-Level Source Type	HDL
Synthesis Tool	XST (VHDL/Verilog)
Simulator	Modelsim-XE VHDL
Preferred Language	VHDL
Enable Enhanced Design Summary	<input checked="" type="checkbox"/>
Enable Message Filtering	<input type="checkbox"/>
Display Incremental Messages	<input type="checkbox"/>

**Make sure that the right FPGA is selected**

**Use Modelsim as the simulator**



# Create New design



**Create a new file  
and save it at a  
Convinient location**



# Specify Entity

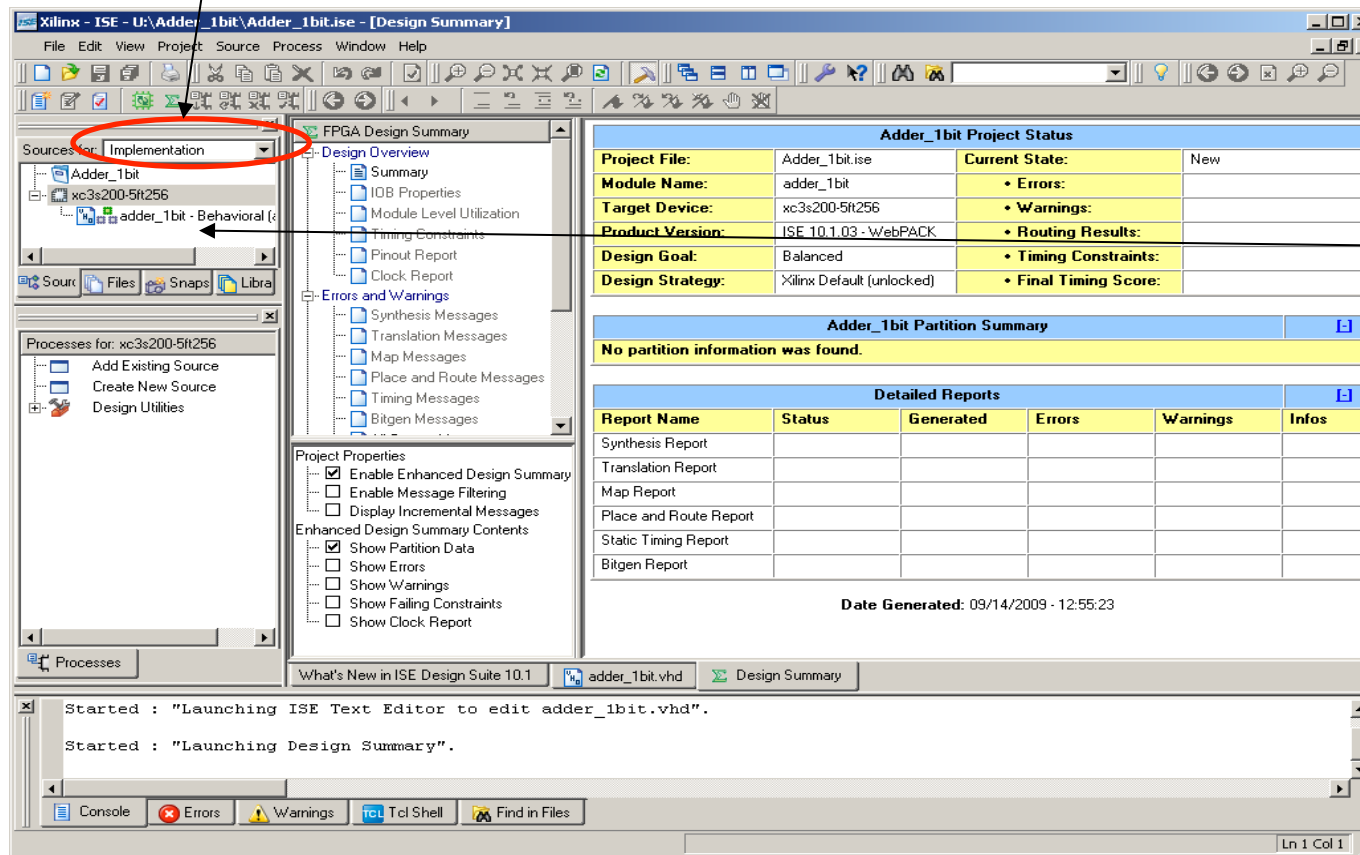
Specify the port names on the entity as well as the type

Port Name	Direction	Bus	MSB	LSB
A	in	<input type="checkbox"/>		
B	in	<input type="checkbox"/>		
Carry_in	in	<input type="checkbox"/>		
Sum	out	<input type="checkbox"/>		
Carry_out	out	<input type="checkbox"/>		
LEDG	out	<input type="checkbox"/>		
	in	<input type="checkbox"/>		
	in	<input type="checkbox"/>		
	in	<input type="checkbox"/>		
	in	<input type="checkbox"/>		



# Design work

Assure that Implementation is selected

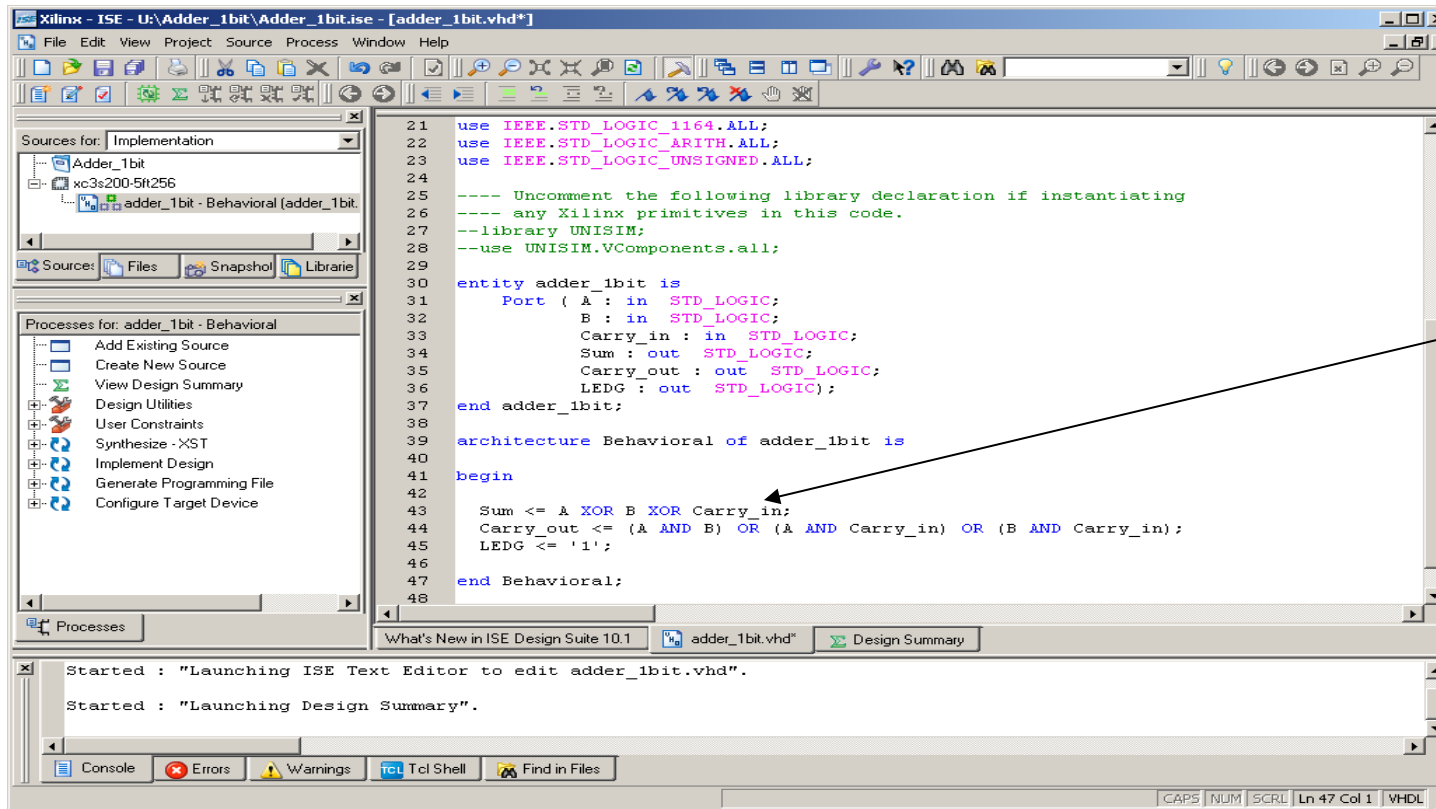


double click on  
**adder1\_bit**  
to open a editor





# Include a behavioral model

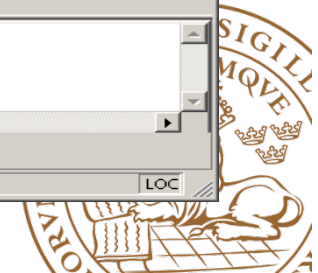
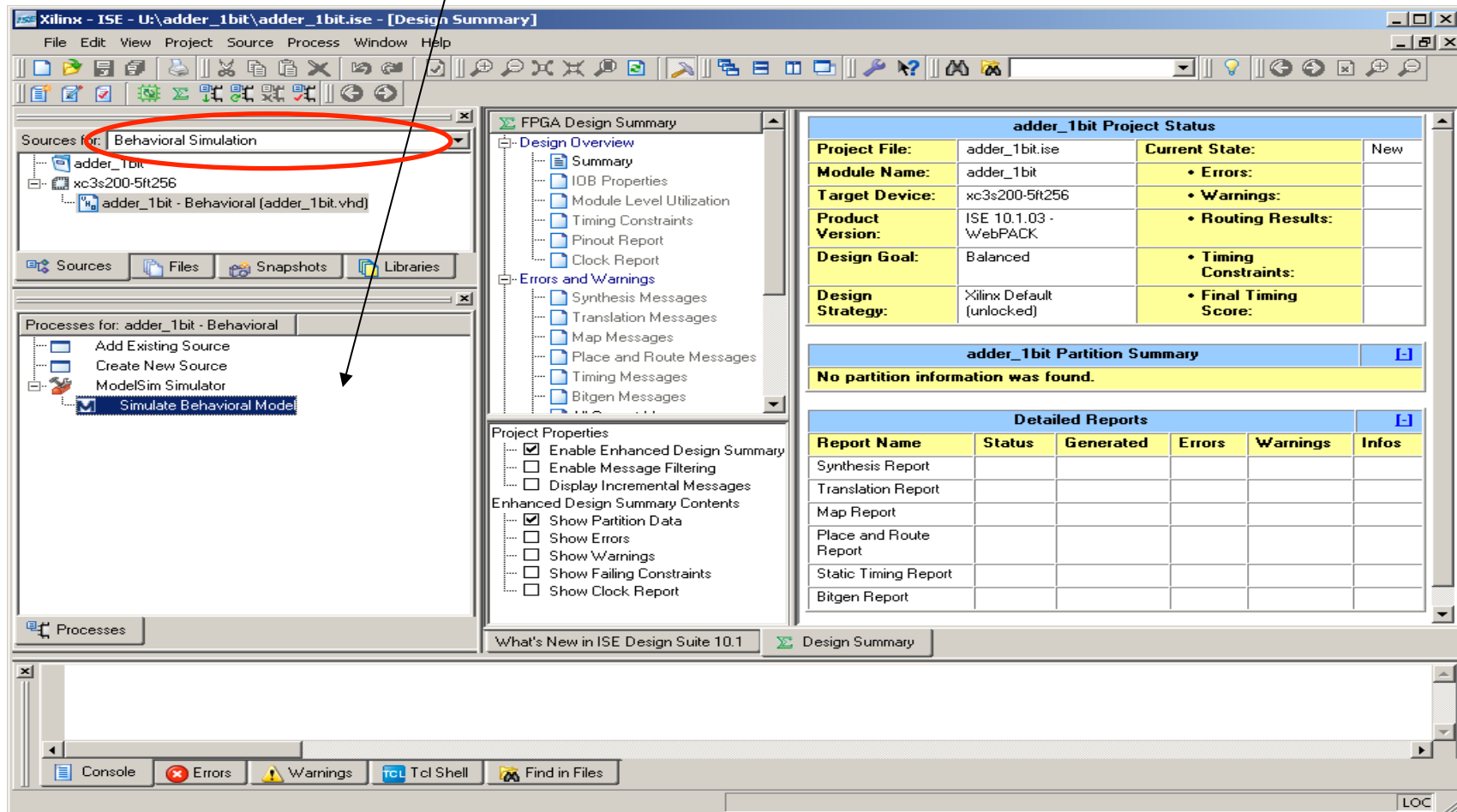


Put the behavioral model in the architecture body



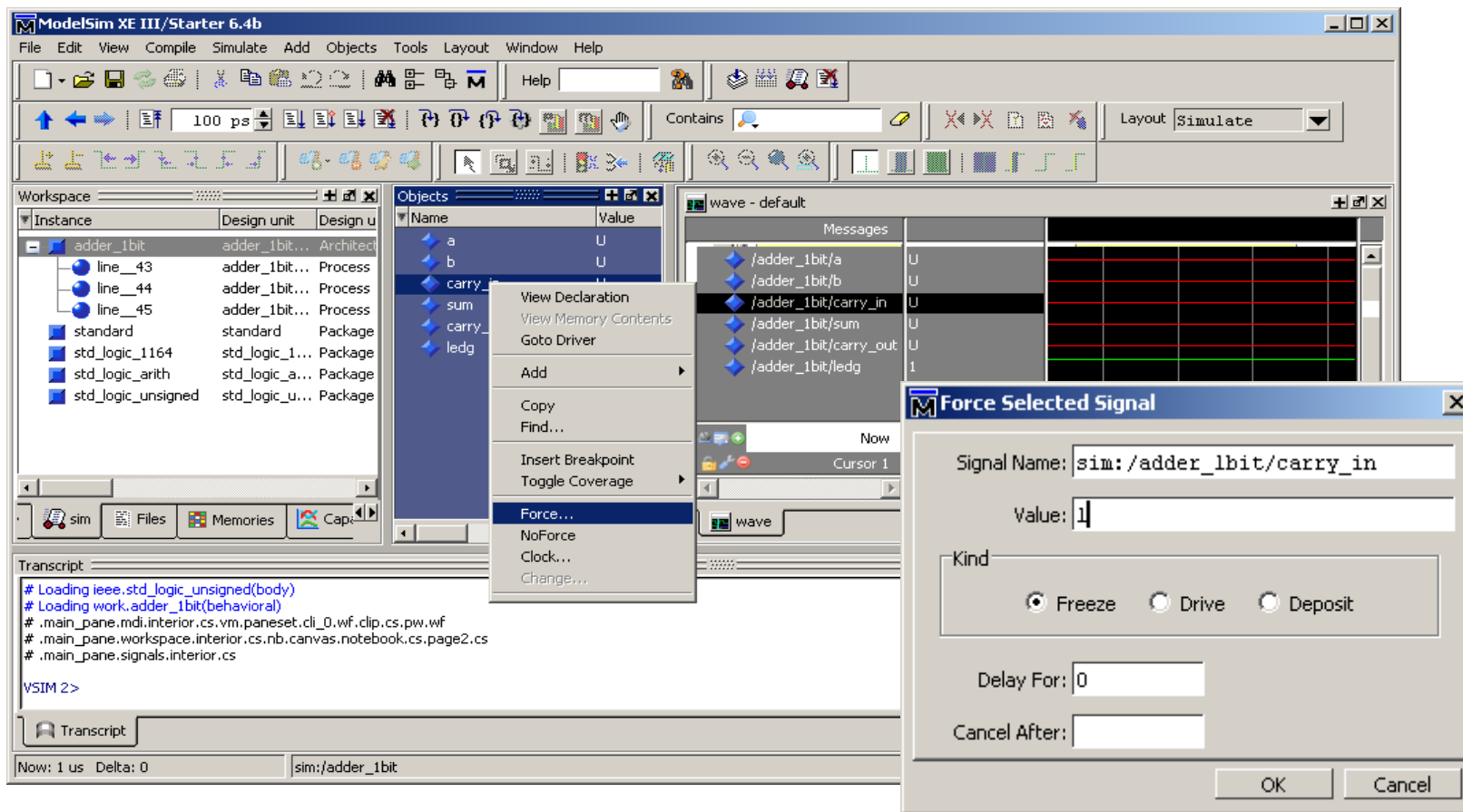
# Simulation

Switch to *Behavioral Simulation*  
and double-click on Modelsim



# Modelsim

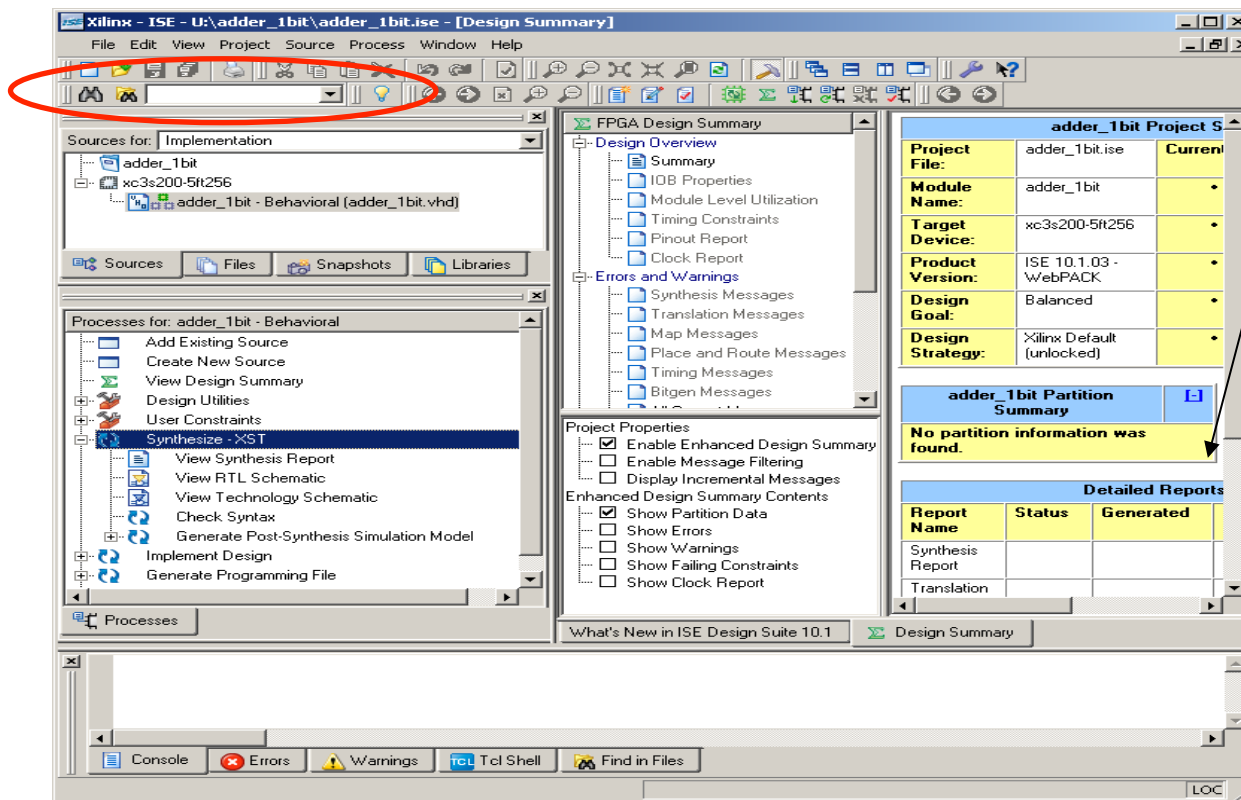
Force the signals and confirm that the signals respond as expected



# Synthesis

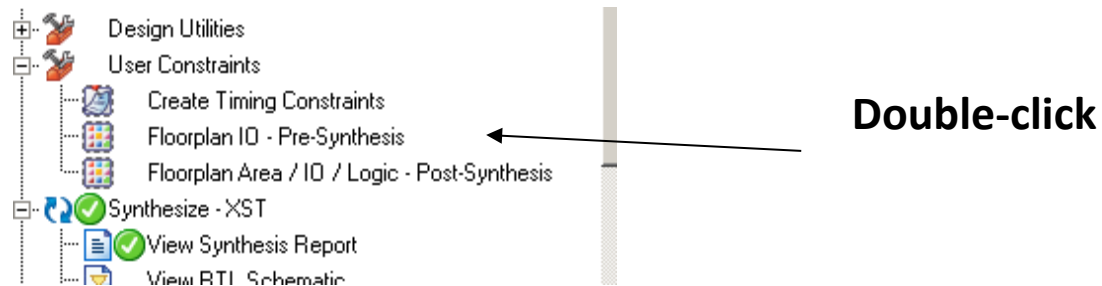
Switch to *Implementation*  
and double-click on Synthesize

Check that the synthesis  
went error free.

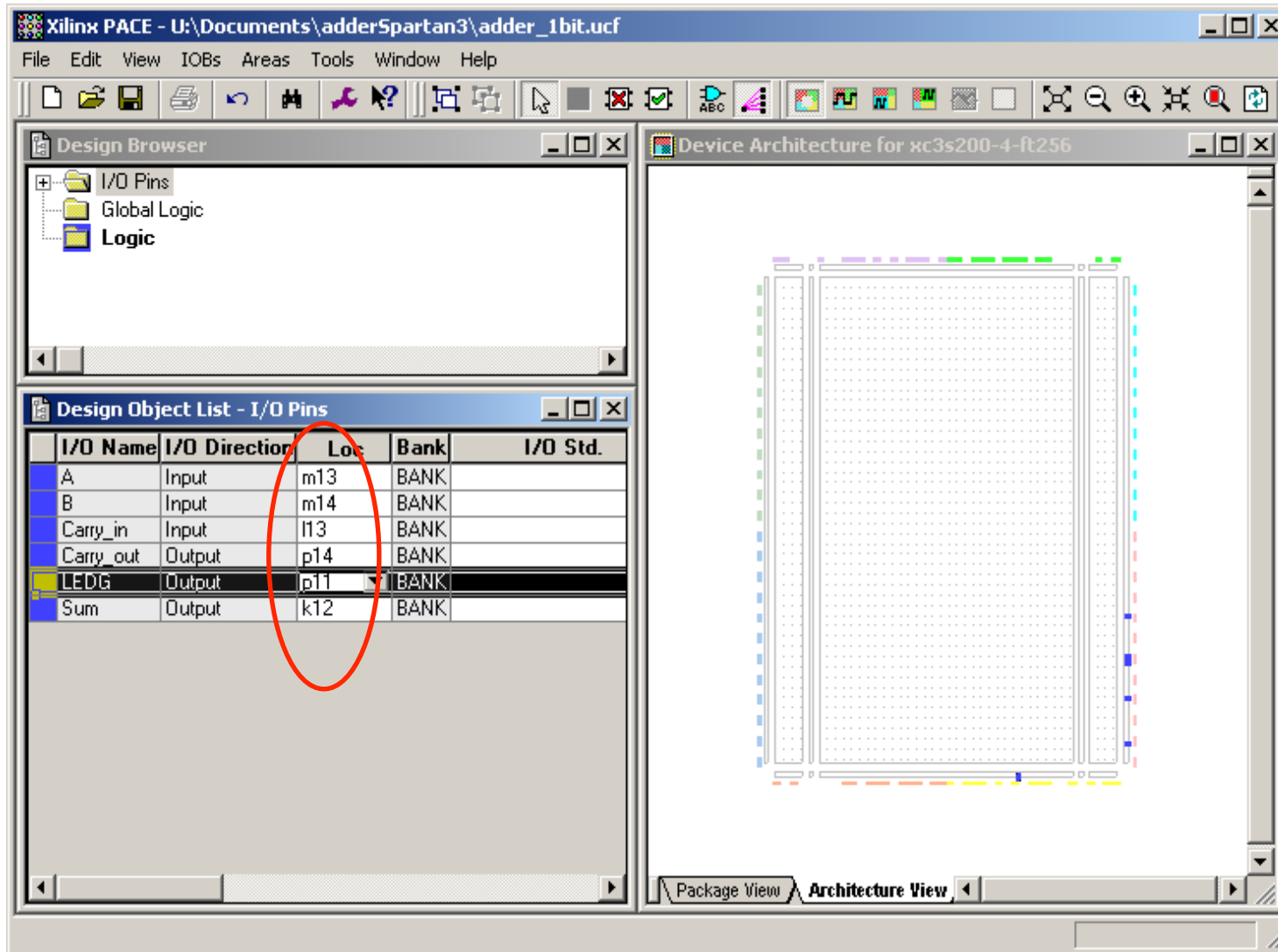


# Button and LED selection

- After functionality is proved on the waveforms in Modelsim, the physical connections need to be defined.



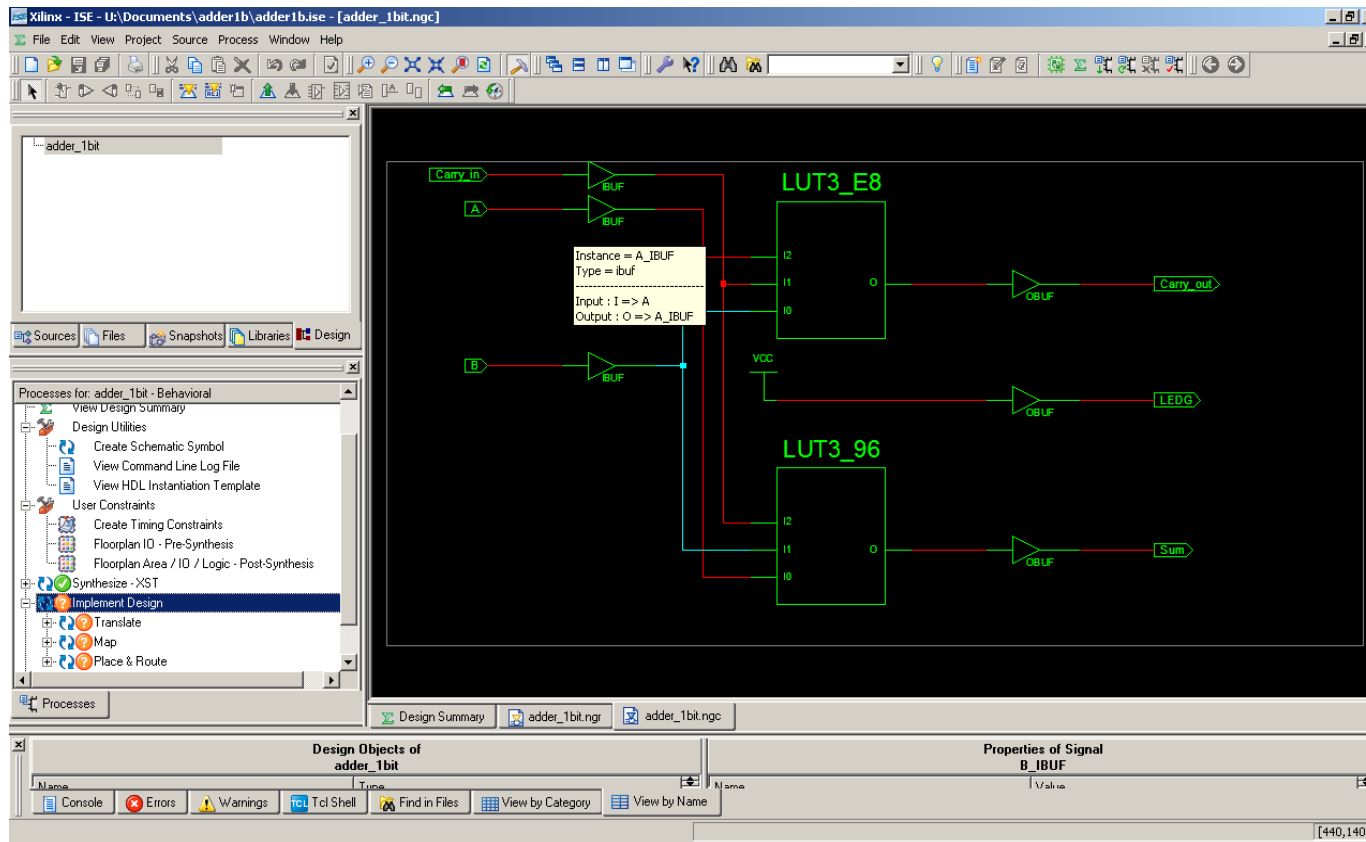
# Specify Connections



Save the specification.  
A .ucf file will be created.



# Mapping

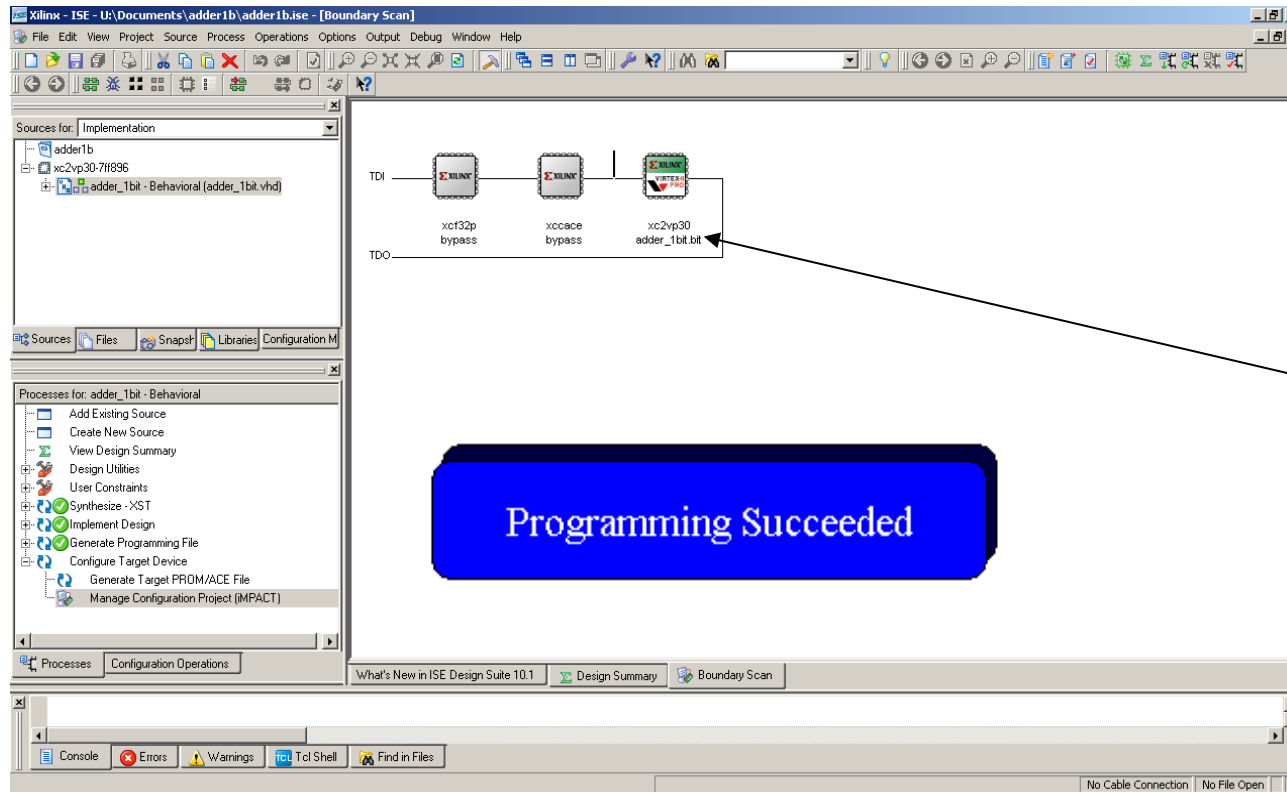


Select:

- Synthesize
- Implement Design
- Generate Programming File



# Programming



If everything went fine select:  
***Manage configuration project***  
and finish, and assign the bit file to the FPGA.

Your device is ready to use.

Try the buttons and monitor the LEDs

