Introduction to Structured VLSI Design

- 1-bit Adder FPGA Example

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Purpose

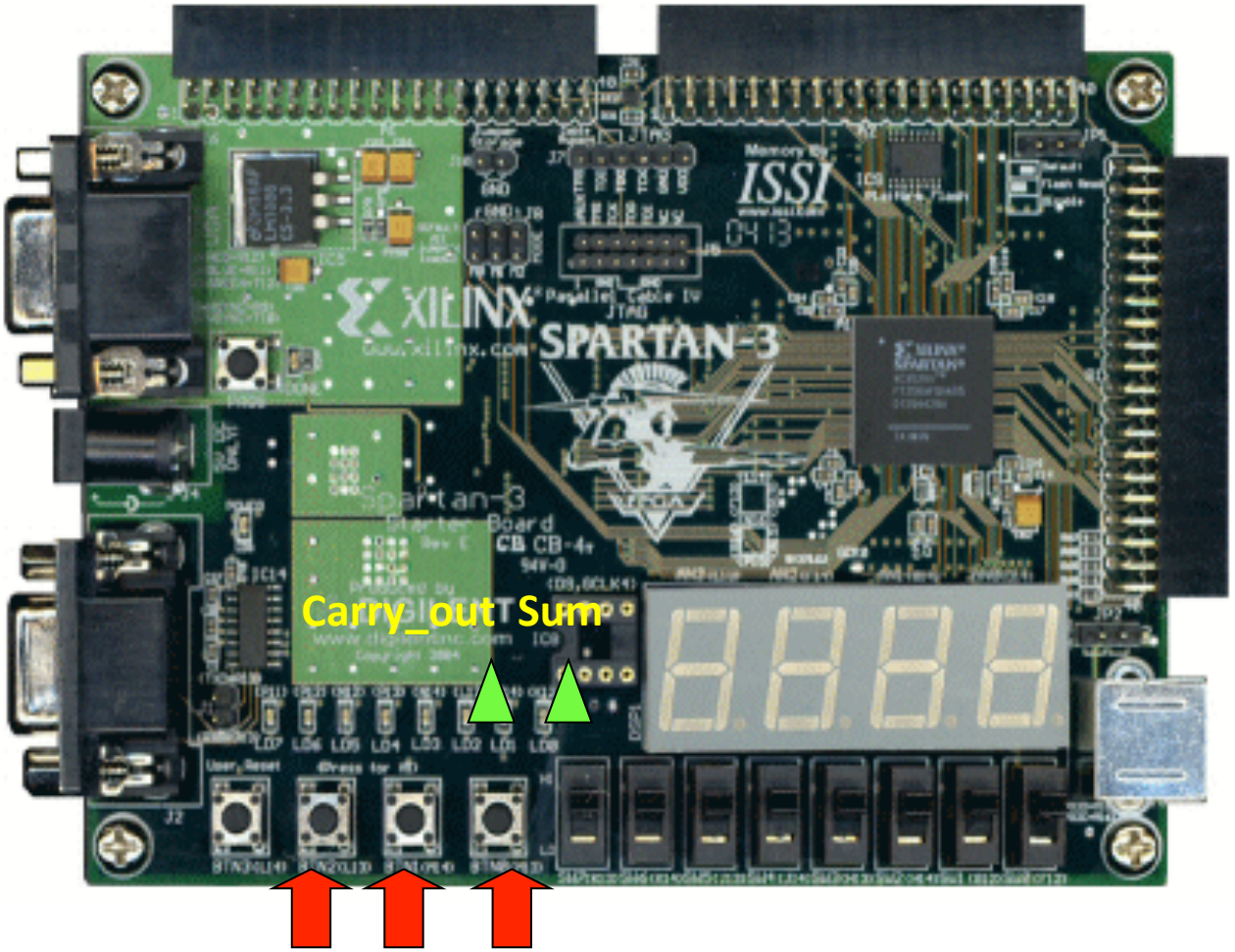
Graphical guide the supplements ISE Quick Start

1-bit Full adder will be

- designed
- simulated in Modelsim
- synthesized (mapped)
- placed
- Programmed
- Executed

on a Spartan 3

In Practice

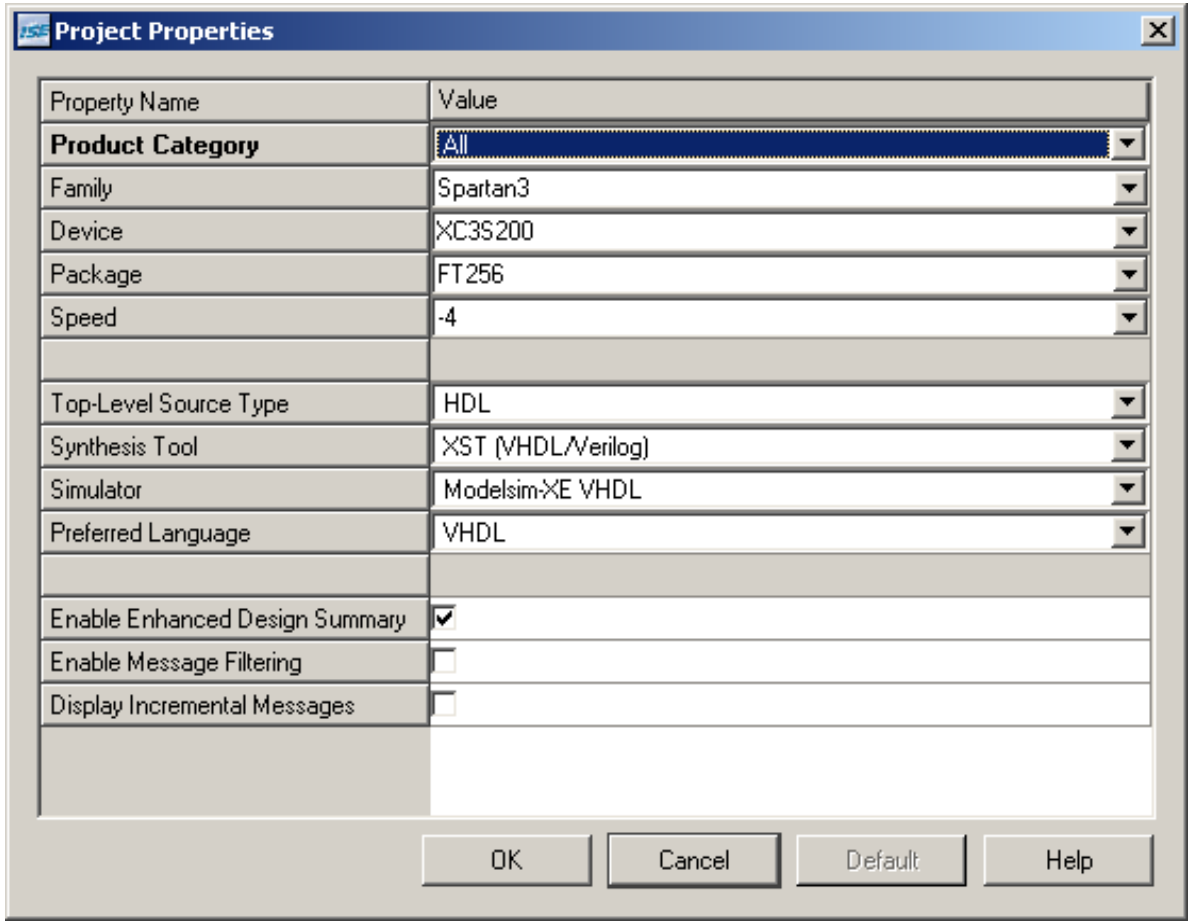


Get started

- Start XILINX ISE
- Select Help-> Tutorials-> ISE Quick Start
- Choose
  - File
  - New Project

  and continue

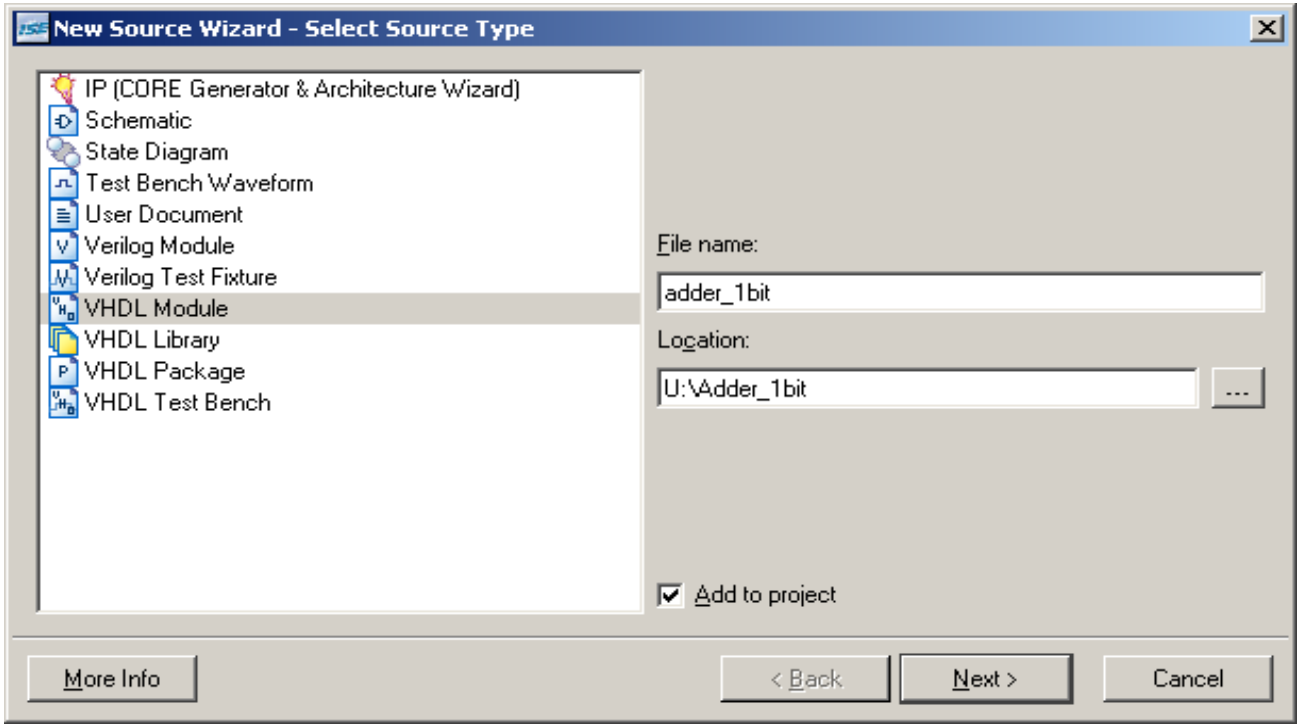
Device Properties



Make sure that the right FPGA is selected

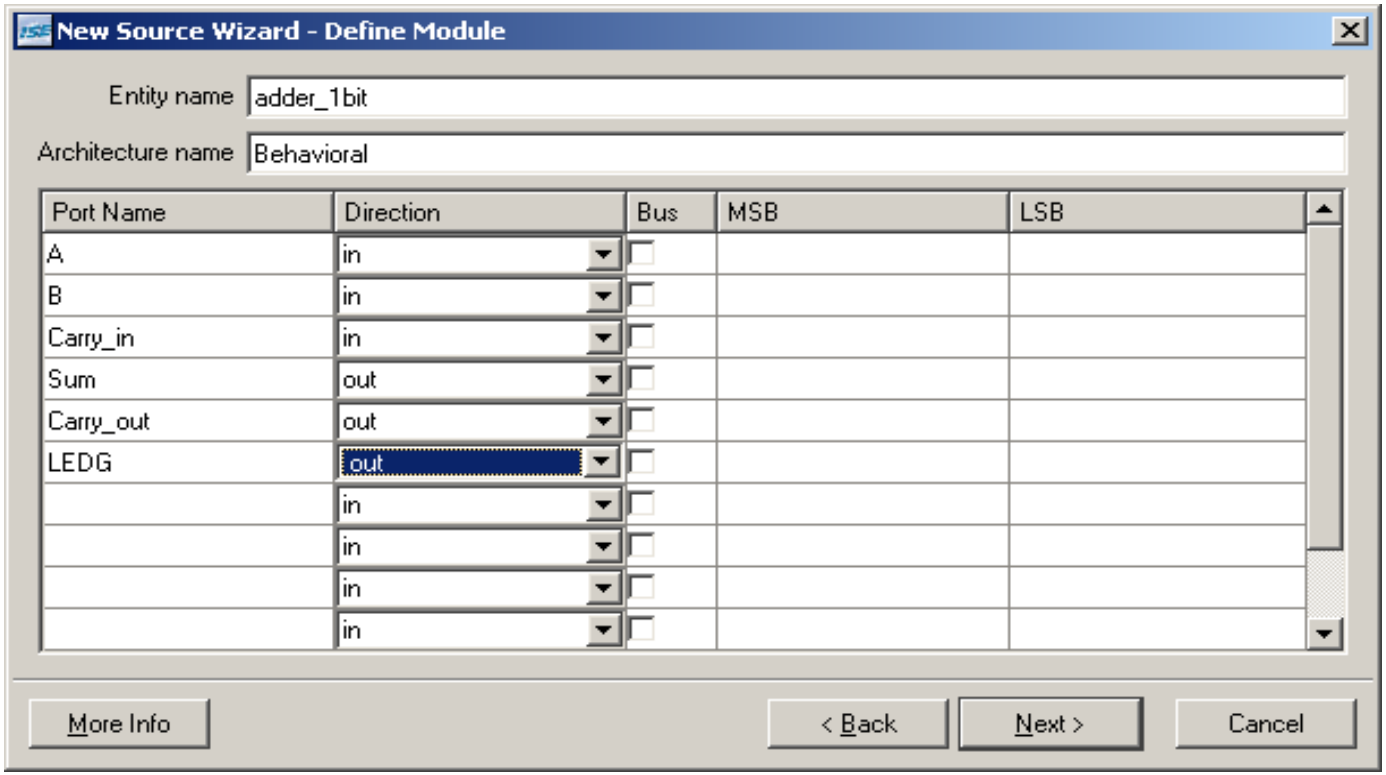
Use Modelsim as the simulator

Create New design



Create a new file and save it at a Convinient location

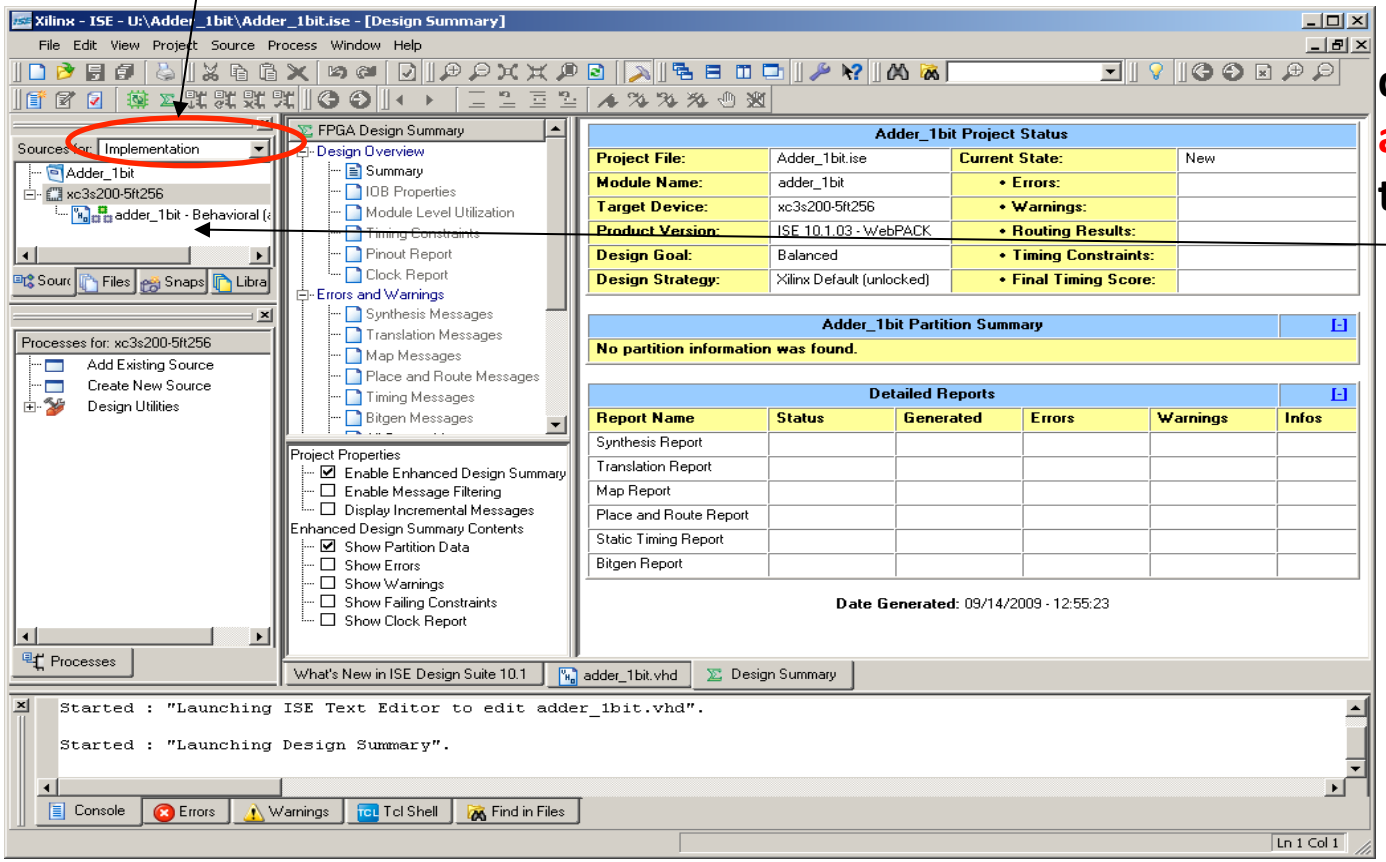
Specify Entity



Specify the port names on the entity as well as the type

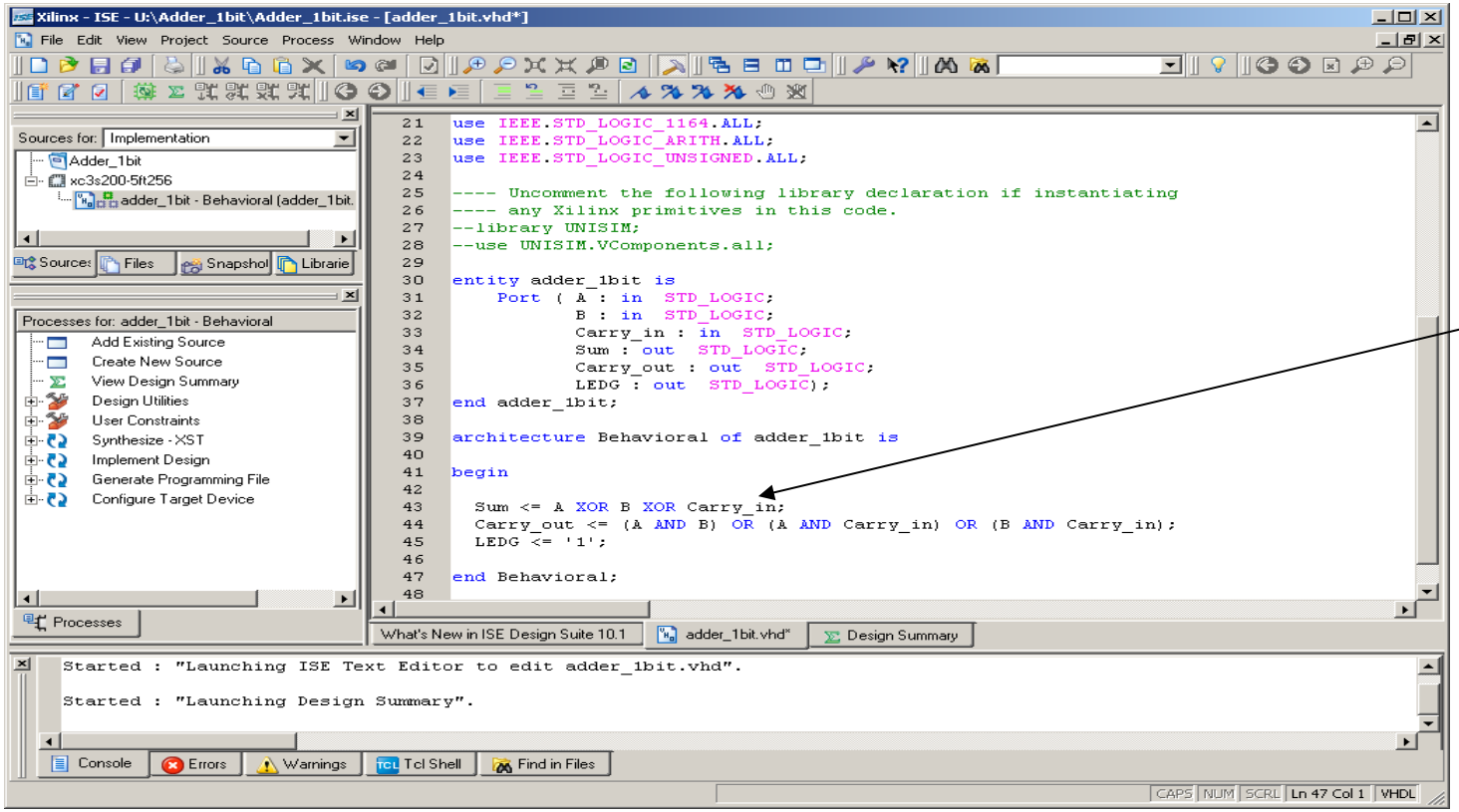
Design work

Assure that Implementation is selected



double click on adder1_bit to open a editor

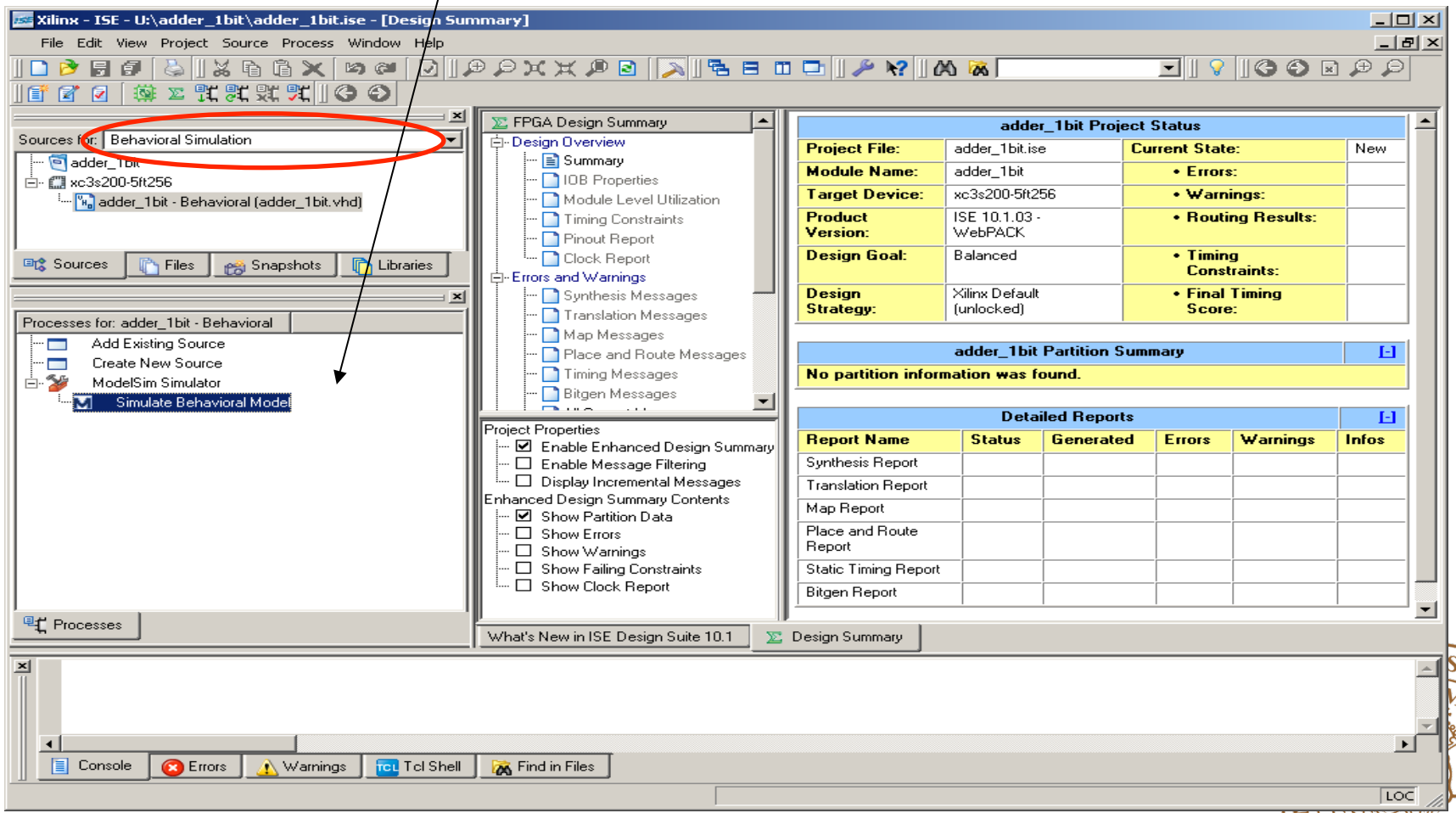
Include a behavioral model



Put the behavioral model in the architecture body

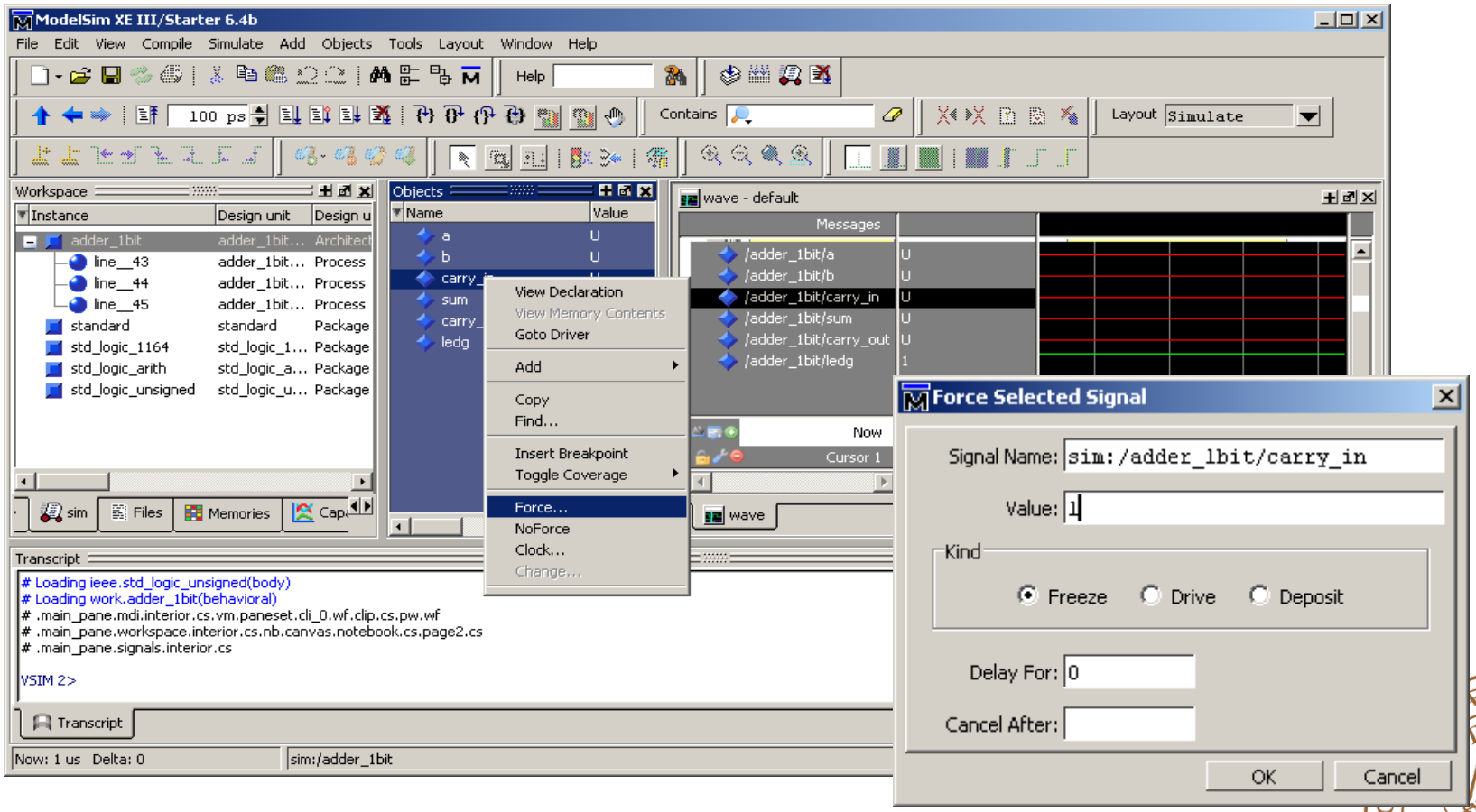
Simulation

Switch to *Behavioral Simulation*
and double-click on Modelsim



Modelsim

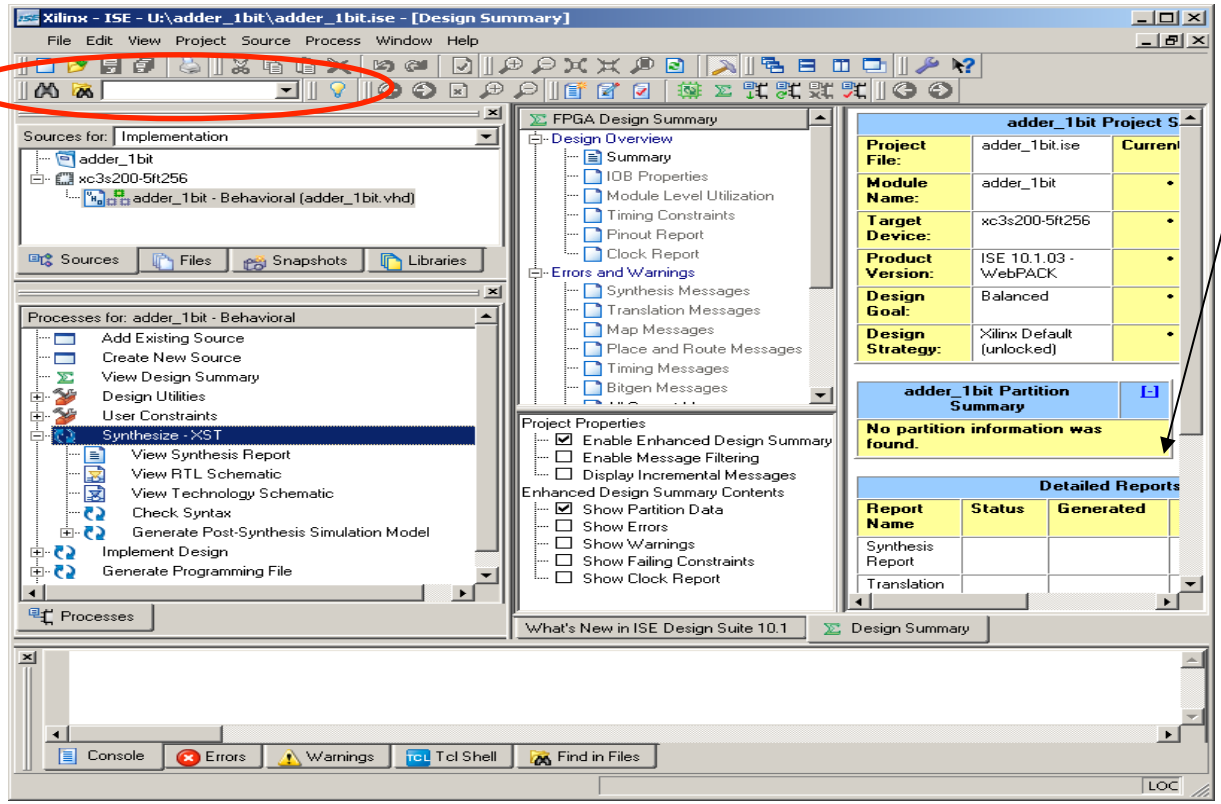
Force the signals and confirm that the signals respond as expected



Synthesis

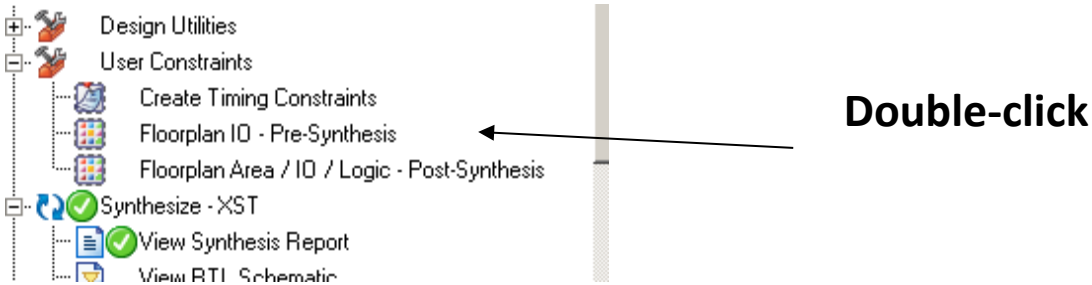
Switch to *Implementation*
and double-click on Synthesize

Check that the synthesis went error free.

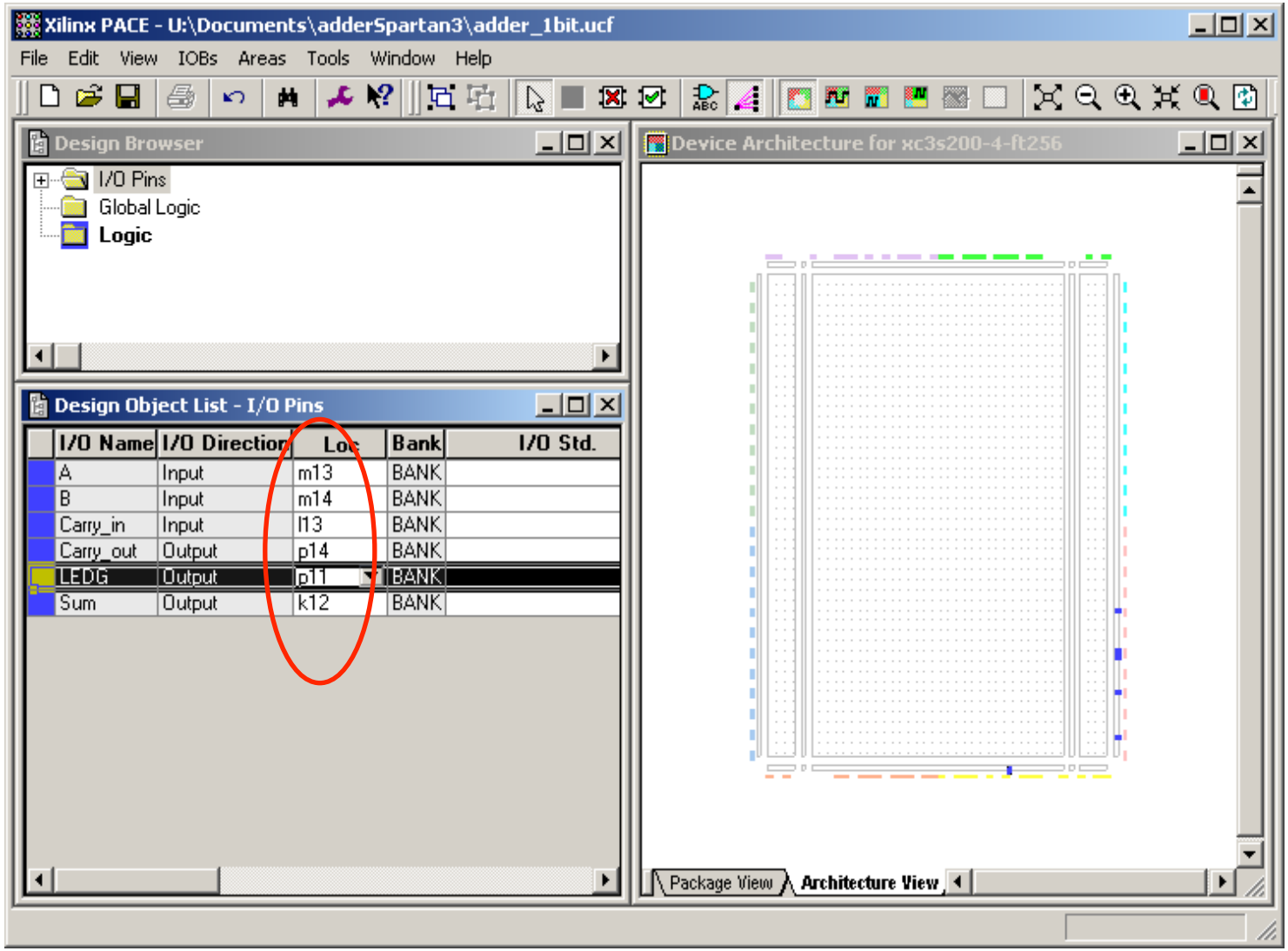


Button and LED selection

- After functionality is proved on the waveforms in Modelsim, the physical connections need to be defined.

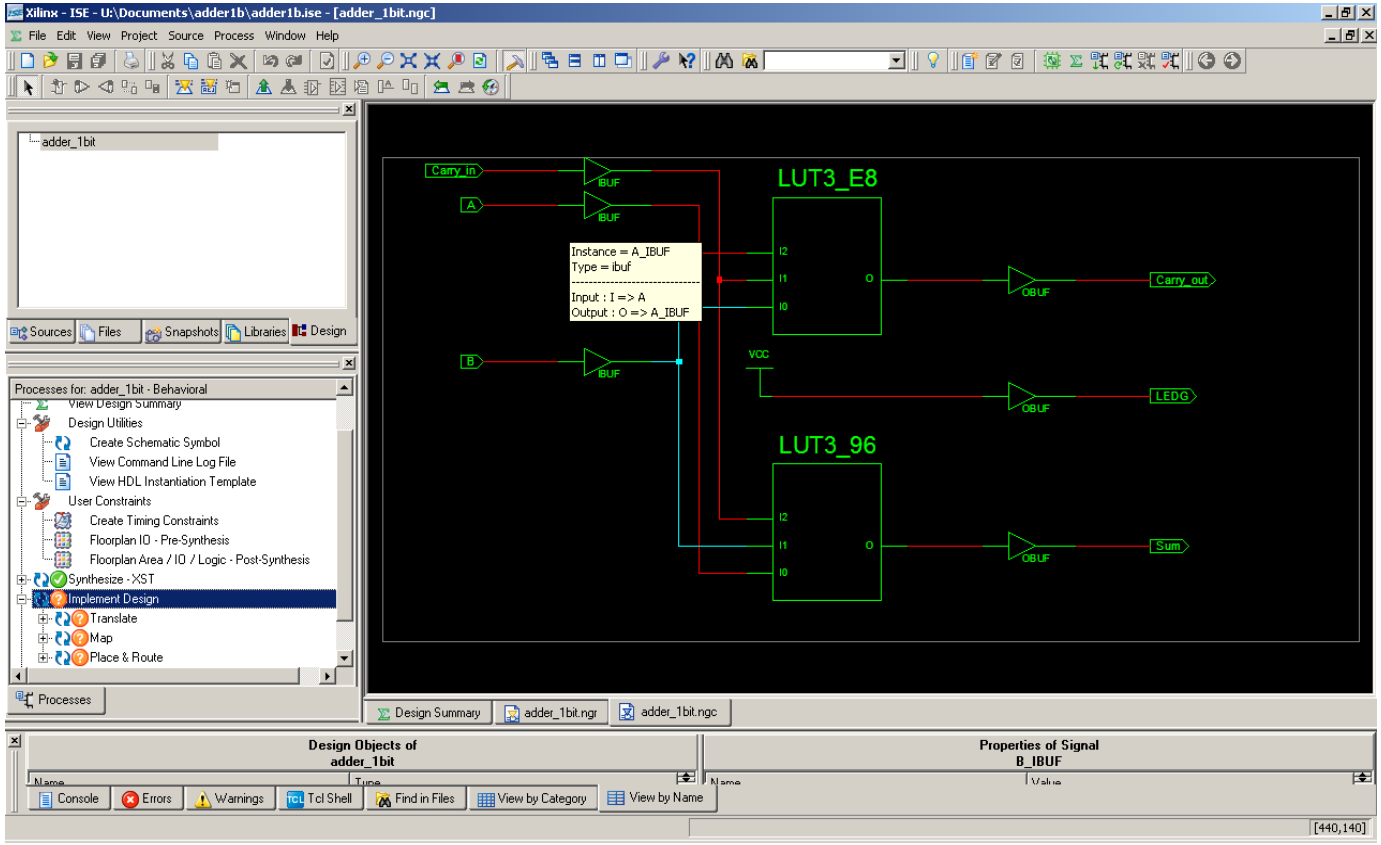


Specify Connections



Save the specification. A .ucf file will be created.

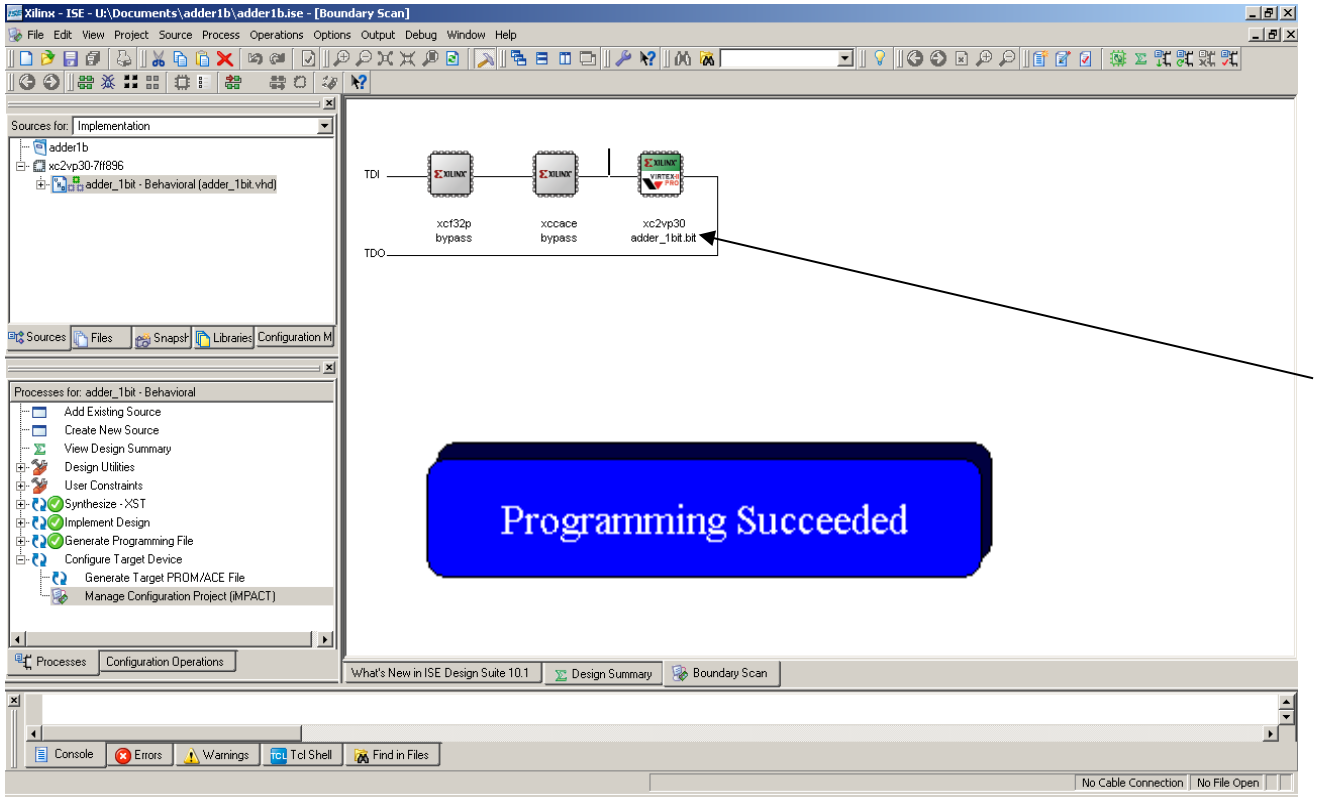
Mapping



Select:

- **Synthesize**
- **Implement Design**
- **Generate Programming File**

Programming



If everything went fine select:
Manage configuration project
and finish, and assign the bit file to the FPGA.

Your device is ready to use.

Try the buttons and monitor the LEDs