VHDL

Very High Speed Integrated Circuit Hardware Description Language

Enkel och-grind

```
--detta är en kommentar
--enkel 3-ingångars och funktion
--föreläsning ht-06
-- språket är inte casesensitivt(skiljer inte på stora och SMÅ bokstäver)
library IEEE;
use IEEE.std_logic_1164.all;

entity och3 is
   port( a,b,c: in std_logic;ut: out std_logic);
end entity och3;

architecture beteende of och3 is
begin
     ut<=a and b and c;
end architecture beteende;
```

Kombinatoriskt nät sid 44

```
library IEEE;
use IEEE.std_logic_1164.all;
-- Detta är en kommentar!
entity Grind2 is
        port(a,b,c:in std_logic;
        x,y:out std_logic);
end entity Grind2;

architecture beteende of Grind2 is
begin
        x<=a and b and c;
        y<= not( a and b and c);
end architecture;
```

MUX2-1 med if-sats(Process)

```
--MUX2-1 med process och if sats. sid 404.
library IEEE;
use IEEE.std_logic_1164.all;

entity MUX2_1 is
   port(d_in0,d_in1, adress:in std_logic;
      d_ut:out std_logic);
end entity MUX2_1;
architecture beteende of MUX2_1 is
begin
  process(d_in0,d_in1, adress)--sensitivity list
  begin
     if adress='0' then
      d_ut<=d_in0;
    else
      d_ut<=d_in1;
    end if;
  end process;
end architecture beteende;
```

Parallella satser sid 399

```
library IEEE;
use IEEE.std_logic_1164.all;

entity mux2_1_p is
   port(d_in0, d_in1, adress:in std_logic;
      d_ut:out std_logic);
end entity mux2_1_p;

architecture beteende  of mux2_1_p is
begin

    d_ut<=(not adress and d_in0) or (adress and d_in1);--obs! parenteserna!!

end architecture beteende;
```

MUX 4-1

```
    --MUX4_1 sid 405
library IEEE;
use IEEE.std_logic_1164.all;

entity MUX4_1 is
   port(data_in:in bit_vector(3 downto 0);
      a:in bit_vector(1 downto 0);
      data_ut:out bit);
end entity MUX4_1;

architecture beteende of MUX4_1 is
begin
   process(data_in,a)--sensitivity list
   begin
      case a is
         when "00"   =>data_ut<=data_in(0);
         when "01"   =>data_ut<=data_in(1);
         when "10"   =>data_ut<=data_in(2);
         when "11"   =>data_ut<=data_in(3);
         --when others  =>data_ut<=null;
      end case;
   end process;
end architecture beteende;
```

MUX2-1x8

```
--MUX2_1, som hanterar en byte.
library IEEE;
use IEEE.std_logic_1164.all;

entity MUX2_1x8 is
   port(d_in0, d_in1: in std_logic_vector(7 downto 0); adress :in std_logic;
         d_ut: out std_logic_vector(7 downto 0));
end entity MUX2_1x8;

architecture beteende of MUX2_1x8 is
begin
   process(d_in0, d_in1, adress)
   begin
      if adress='0'then
         d_ut<=d_in0;
      else
         d_ut<=d_in1;
      end if;
   end process;
end architecture beteende;
```