Encounter Workshop 1

What you will learn

Setting up Encounter the environment

Importing a design

Using the Design Browser

Learning floorplanning

Editing floorplan objects

Adding Power/Ground stripes and rings

Routing Power/Ground

Running Amoeba Placement

Reordering scan chain

Running Trial Route

Viewing the design

Extracting RC data

Generating simulation files and wire load models

Calculating delays and generating SDF file

Building setup timing graph and generating slack report

Fixing setup timing violations by In-Place Optimization (IPO)

Running clock tree synthesis

Building hold time timing graph and generating slack report

Fixing hold timing violations by IPO

Discussing, preventing, analyzing, and fixing SI problems

Running power analysis (Optional)

1. DTMF Design Information

DTMF information - The design in this workshop is a Dual Tone Multi-Frequency (DTMF) receiver which is one of the common forms of in-band signaling in a telephone network. For an example, DTMF signals are generated by a touch tone telephone.

The DTMF design contains almost 6,000 instances, 57 IO pads, and about 6,274 nets. The netlist format is hierarchical Verilog. It has several clock sources and their hierarchical net names are:

DMA System Clock:	DTMF_INST/clk
Serial Port Interface Clock:	DTMF_INST/spi_clk
Scan Clock:	scan_clk

The design contains 2 scan chains.

The process used is the Artisan 180 nanometer process technology with 6 layers of metal. These Artisan library files, such as the timing libraries and LEF, must be downloaded from the Cadence Learning Management System website.

Workshop overview - Virtual prototyping is used to quickly determine the feasibility of the DTMF design. The design inputs are the netlist, floorplan, clock sources, and timing constraints. The process/technology inputs are the physical libraries, timing libraries, process technology libraries. The design is:

- Imported,
- Floorplanned
- Amoeba placed
- Scan chain optimized
- Trial routed
- Wire parasitic extracted
- Timing analyzed
- In-Place optimized to close timing
- Clock tree synthesized
- Trial routed
- Timing analyzed
- Signal integrity analyzed

2. Setting up Encounter and the work directory

The following is the instruction to setup and use the Encounter design tool. You need to find the installed Encounter directory to get access to the both the Encounter software and the DTMF design. It is located in the '<install_dir>/share/fe/gift/tutorials/dtmf' directory.

Checklist -

a. Locate the Encounter install directory.
b. Create a work directory to run the DTMF design.
c. Login to the Cadence Learning Management System at:
http://learning.cadence.com

Setting the Encounter environment -

You must set the installation directory in your path and set the environment variable for the cdslmd license:

```
set path=(<install_dir>/tools/bin $path)
setenv LM_LICENSE_FILE                    \
<install_dir>/share/license/<cdslmd_lic>
which encounter (to see if the path is set properly?)
```

Setting up your work directory for the workshop –

This requires three steps.

1) Copying the DTMF design data –

Copy all the contents (files and directories) from the '~fe/gift/tutorial/' directory to your work directory. Use the UNIX commands:

```
mkdir <work_directory_name>
cd <work_directory_name>
cp –r <install_dir>/share/fe/gift/tutorials/dtmf/* .
```

2) Downloading the Artisan 180nm libraries –

To obtain the libraries, you must login to Learning Management System website at http://learning.cadence.com. After registering with your name, email address, and your own password, you can download the libraries. The libraries are listed under products for Digital IC Design and look for "Encounter Tutorials - v3.3." There is no charge for the libraries, but you must accept an Artisan License Agreement.

After downloading the library tar file, move the tar file to your work directory, and untar (GNU version) the tar file. Now, there are two new sub directories in your work directory and they are "lef" and "tlf."

3) Running the DTMF design –

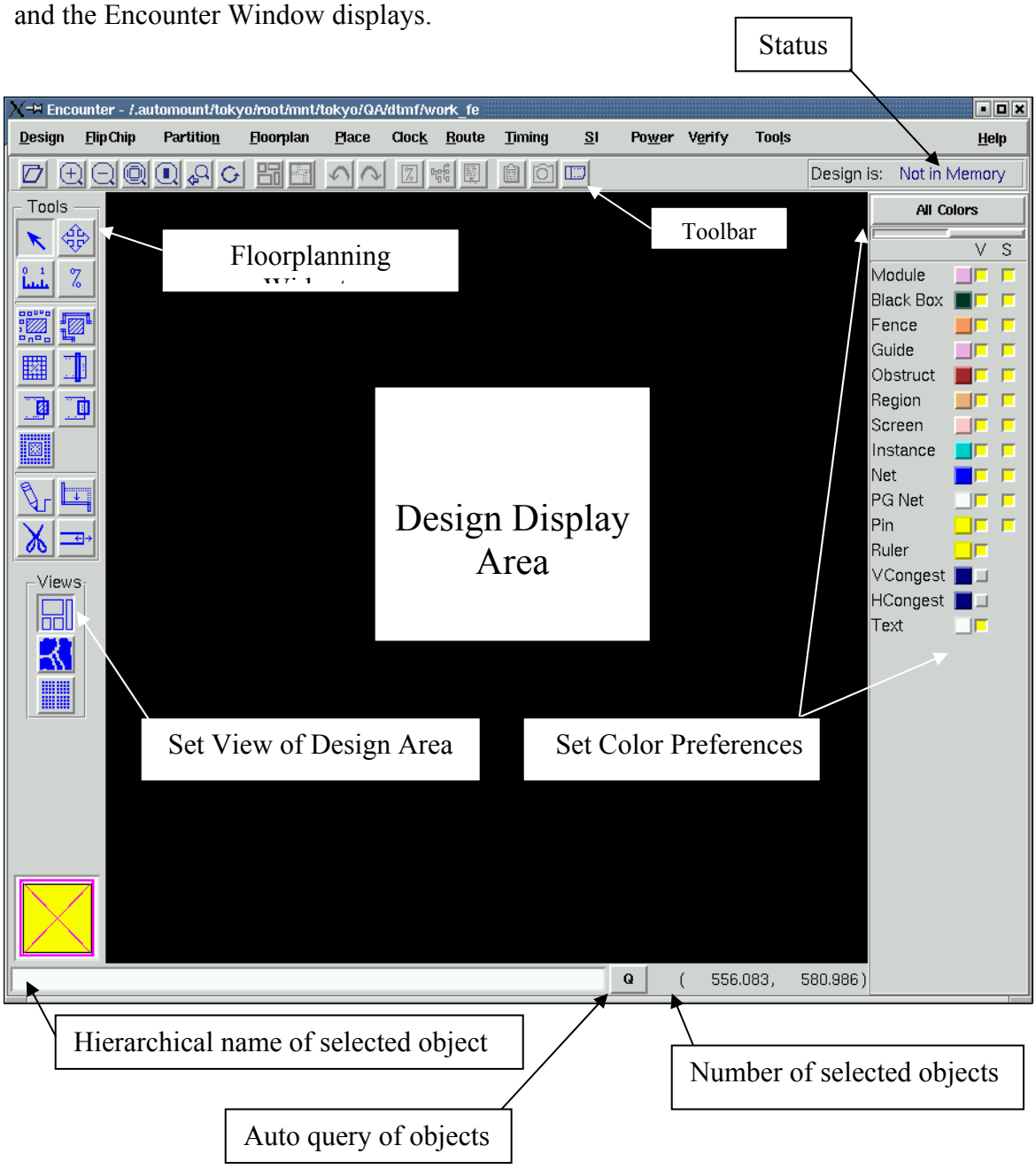
Your work directory is complete by copying the design, downloading the Artisan library, and untaring the library file. Now, you are ready to start an Encounter session.

3. Starting an Encounter Session

In the `dtmf/work_fe` work directory, type:

```
encounter
```

and the Encounter Window displays.



Encounter Mouse and Keyboard Usage

Left Mouse Button (LMB)
Click – Selects/Highlights an object.
Double Click – Opens the Object Editor form.

Middle Mouse Button (MMB)
Click-and-Drag – Pans the display.

Right Mouse Button (RMB)
Click-and-Drag – Zooms in the display.

Editing a Floorplan Object
Space Bar – Change focus on an object to be edited.

Encounter General Binding Keys

Key	Action	Description
q	Attribute	Display the object attribute editor form on selected object.
f	Fit Display	Zooms the display to fit the core area.
g	Group	Moves up the hierarchy on the highlighted Hinstance.
u	Ungroup	Moves down the hierarchy on the highlighted Hinstance.
v	View DB	View the attributes of highlighted object.
z	Zoom-in	Zooms in the display, 2x.
R	Redo	Returns the design to state to last Undo command.
U	Undo	Returns the design to state to previous command.
Z	Zoom-out	Zooms out the display, 2x.
Shift	Selects	Allows multiple selections of objects.
Arrows	Pans	Pans the display in direction of arrow.
Delete	Ruler	Removes last ruler displayed.
Space Bar	Focus	Changes the focus of overlapping objects

Auto Query Q Binding Keys

Key	Action	Description
n	Focus	Changes the focus of overlapping objects.
p	Focus	Changes the focus of previous overlapping object.
F2	Prints	Prints object information in the Encounter console

Edit Route Form Binding Keys

Key + Mouse Button	Action	Description
Esc button	Ends	Ends the drawing mode for creating special route.
Delete	Deletes	Removes last point/segment.
Arrows	Moves	Moves the current segment in direction of arrow.

Binding Key Help

To display or change the Binding Keys, traverse the Menu – *Design -> Preference*, and on the Design tab/page, click the Binding Key button. This displays all the binding key and commands.

Encounter User Guide and Command Help

Help is available by using an internet browser. Click the left mouse button (LMB) on the Help button in the upper right corner of the Encounter console. Or click on the Help button in the individual forms and the browser displays the related page from the Encounter User Guide.

The Encounter Command help is available by Man pages. Type:

`man commandName` or

`help keyword` and a list of commands displays pertaining to the keyword.

Keywords:

```
analysis
buffer
clock
crosstalk
design
eco
fix
floorplan
import
partition
place
preference
power
route
timing
verify
voltage
```

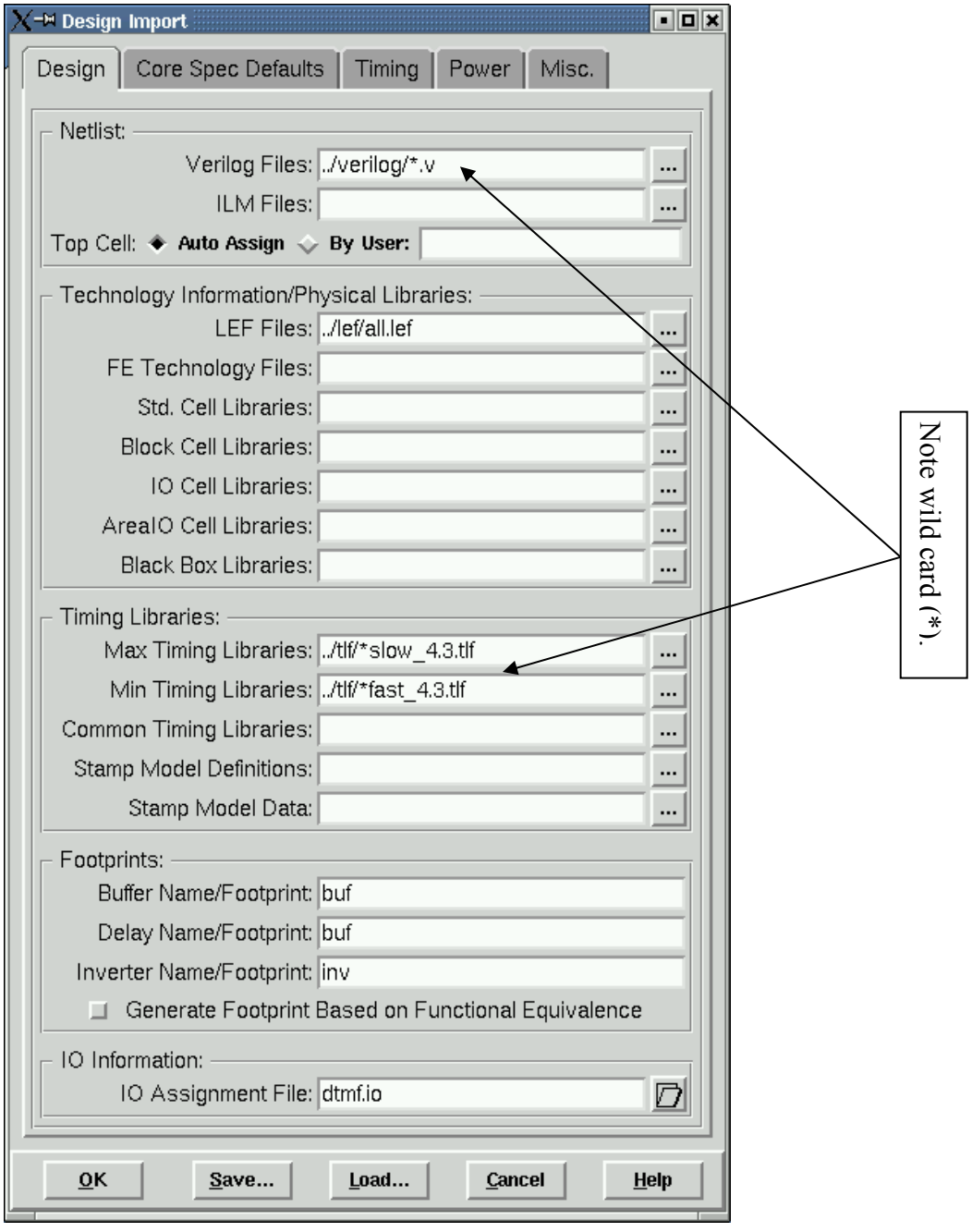
4. Importing the Design

Importing the design - The Design Import form is used to load the Verilog netlist, physical libraries, process technology libraries, timing libraries, and timing constraints. Other important items are also loaded during design import and they are contained in the 5 tabs of the Design Import form. Open the *Design Import* form and make the following entries.

Form - *Design -> Design Import*

Complete the Design tab as shown Figure 1. Important: You must enter the file names with wild card character (`*`) and use the file widget [...] to browse and select the other file names. Do not click the [OK] button yet.

Figure 1 - Completed Design Tab of the Design Import Form



If you want, you can click the [Load] button, and select the import configuration file, `dtmfLefSlow.conf`, to completely set up the Design Import form.

Now, click on the *Core Spec Default* tab of the Design Import form to only view the core related design default values. We will do some floorplanning later. Do not click the OK button yet.

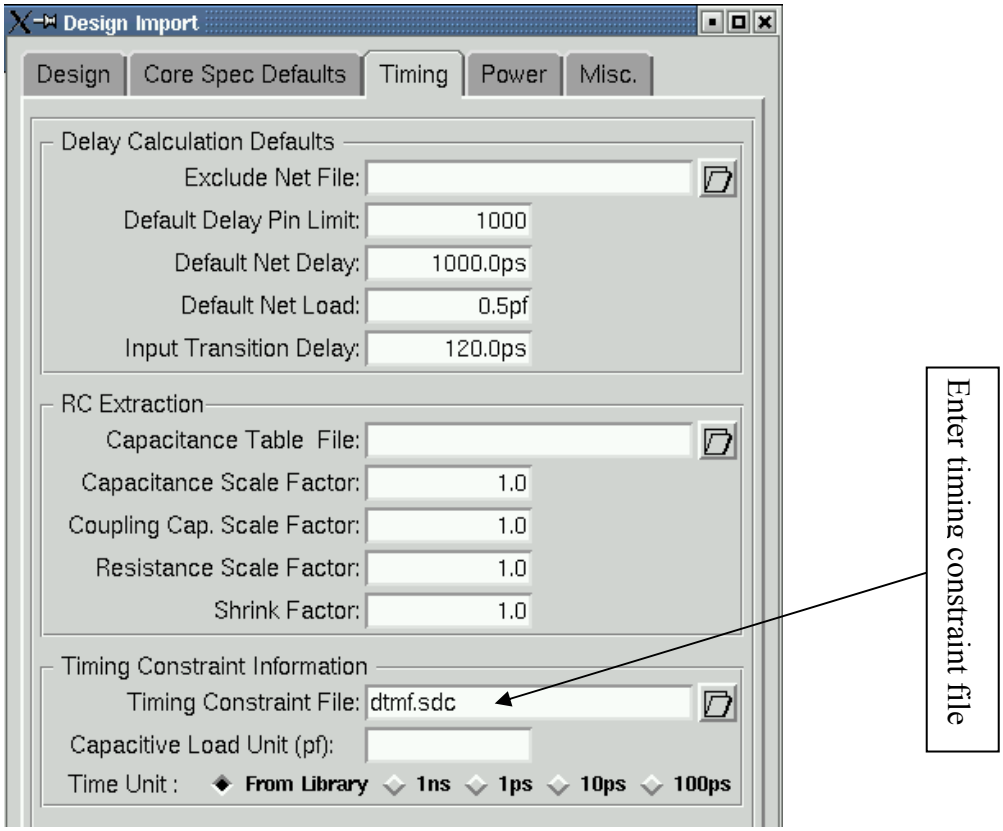
Next, complete the Timing page.

Click the *Timing* tab and make the entries as in Figure 2:

Enter – Timing Constraint File: `dtmf.sdc`

View the delay calculation and RC extraction scaling default values used in our workshop. Do not click the OK button yet.

Figure 2 - Completed Timing Tab of the Design Import Form



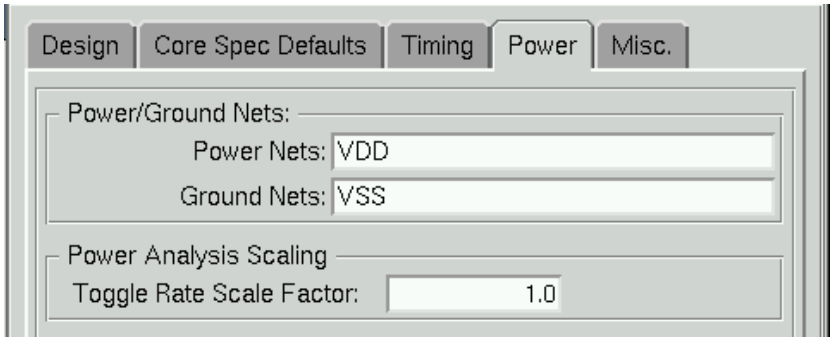
Last, complete the Power page.

Click the *Power* tab and make the entries as in Figure 3:

Enter – Power Nets: VDD
Enter – Ground Nets: VSS

Click OK when ready to import the design.

Figure 3 - Completed Power Tab of the Design import Form



Design Import information – The entries in of the Design Import form depends on the design's library sources. The design's library sources are the physical libraries and process technology library information, and these sources are usually available in LEF format and GDS with technology (tf) formats. 1) As in this workshop exercise, enter the LEF file in the Design Import form since this LEF file is complete with all the physical library information and the process technology information. Then no entries are necessary for the Encounter Technology Files, Std. Cell Libraries, Block Cell Libraries, and IO Cell Libraries. 2) GDS physical libraries need to be translated to Cdump format files and the technology file needs to be translated to the Encounter Technology format file. The Cdump files are translated by the `readgds` program and Encounter Technology file is translated by the `tf_reader` program. To view a Design Import form with Cdump and Encounter Technology file entries, load the configuration file, `dtmfCdump.conf`.

Note there were 2 timing libraries loaded during import and these are the maximum and minimum timing libraries. These 2 libraries allow selecting the operating conditions for the setup time analysis and hold time analysis in the same Encounter session.

Viewing the imported design – First, get to know the Toolbar widgets. The Toolbar is the row of widgets directly under the Menus. To see what each widget is, slowly move the cursor over each widget to display their labels. For example, the folder widget on the far left side is the Design Import form. Click (LMB) this widget and the Design Import form opens. Other useful widgets are zooming, redrawing, traversing the design hierarchy, undoing, redoing, and the Design Browser.

Now, zoom out by clicking (LMB) the *Zoom Out* widget (magnify glass with minus sign) in the Toolbar (or enter the `Shift + z` keys). The single large pink colored object on the left side of the core area is the top-level module from the imported Verilog netlist, and the 4 green-grayish colored objects on the right side are all the blocks (hard macros) in the design. The core area appears in the Design Display Area after a design is imported and the size core area can be change by using the *Floorplan -> Specify Floorplan* form. The IO pads are located outside of the core area.

Click (LMB) on the pink colored top-level module, DTMF_INST. This selects / highlights the module and note the blue color connection flylines and yellow color highlighted blocks. The blue flylines display the number of connections between the selected module and other instance such as other modules and blocks. The blocks are highlighted yellow because they are child instances of DTMF_INST. Now, click (LMB) the *Hierarchy Down* widget in the Toolbar or enter the `u`-key (ungroup). Note that the top-level module contains 2 submodules, DTMF_INST/TDSP_CORE_INST and DTMF_INST/RESULTS_CONV_INST. If you want to traverse further down into a submodule, select DTMF_INST/TDSP_CORE_INST and continue entering the `u`-key. To traverse back up the hierarchy, click the *Hierarchy Up* widget in the Toolbar or enter the `g`-key (group). Leave the submodules displayed for an exercise later.

> **Floorplanning a submodule information** – At times there is a need to preplace submodules in the floorplan rather than the top-level module. In the above exercise, it demonstrates graphically how to traverse down a module's hierarchy so the submodule can be displayed and then preplaced (floorplanned).

Now, double click on one of the blocks to view the block's properties. Remember that each floorplan object has properties and these properties can be changed in their Attribute Editor form.

> **Block orientation information** – When a block is selected / highlighted, the flylines are displayed to each pin of the block instead to the center of the block. This feature helps in determining the proper orientation of a block. For example, it helps with route congestion and timing when most of the block pins face the center of the chip or adjacent block pins of face each other.

Using the Design Browser – There are 2 ways to open the *Design Browser* form.

1) **Menu** - *Tools -> Design Browser* or
2) **Toolbar** - (5th widget from the right)

In the Design Browser form, click on the module, `DTMF_INST`, to highlight it. How many instances does it contain? Now, click on (+) sign next to `DTMF_INST` to expand down one level of hierarchy, and you will see the 15 instances under the `DTMF_INST`. You can do the same to the plus sign (+) in front of Terms' to view the 57 terminals.

You can double click on an instance names and traverse down the hierarchy until either the primitive cell or a block is reached.

If you want to find or highlight a net name, notice the stepper button, Instance. To find a net, just enter the net name and change the stepper selection to *Net* or a <CR> will also work. We will do this exercise later.

5. Learning Floorplanning

Changing the core, IO, or die size is done with the Specify Floorplan form.

Specifying die size - Use the *Specify Floorplan* form to set the core box, IO box, and die box sizes. Make the following entries:

Form – *Floorplan -> Specify Floorplan*

Use the default setting for *Core Size by*: *Aspect Ratio*.
Under the section of *Core Margins by*: *Core to IO Boundary*, make the following entries:

Enter – Core to Left: `100`
Enter – Core to Right: `100`
Enter – Core to Top: `100`
Enter – Core to Bottom: `100`

Click Apply.

This moves the IO pads 100 Microns from the outside edge of the core box and this sets the IO box. Now the die box size is set by the height of the IO pad instances.

To modify the core's aspect ratio of height/width (H/W), change the 1.0 default value to `0.5` and click Apply. Now the core shape has been changed to a width that is twice the dimension of the height. Make sure to change the core aspect ratio to 1.0 since will need this in the next exercise.

Learning floorplan widgets/tools - Get to know the floorplan widgets under the *Tools* (left side of the Encounter form) by displaying the labels of each widgets/tools. This is done by slowly moving the cursor over each widget to display their labels.

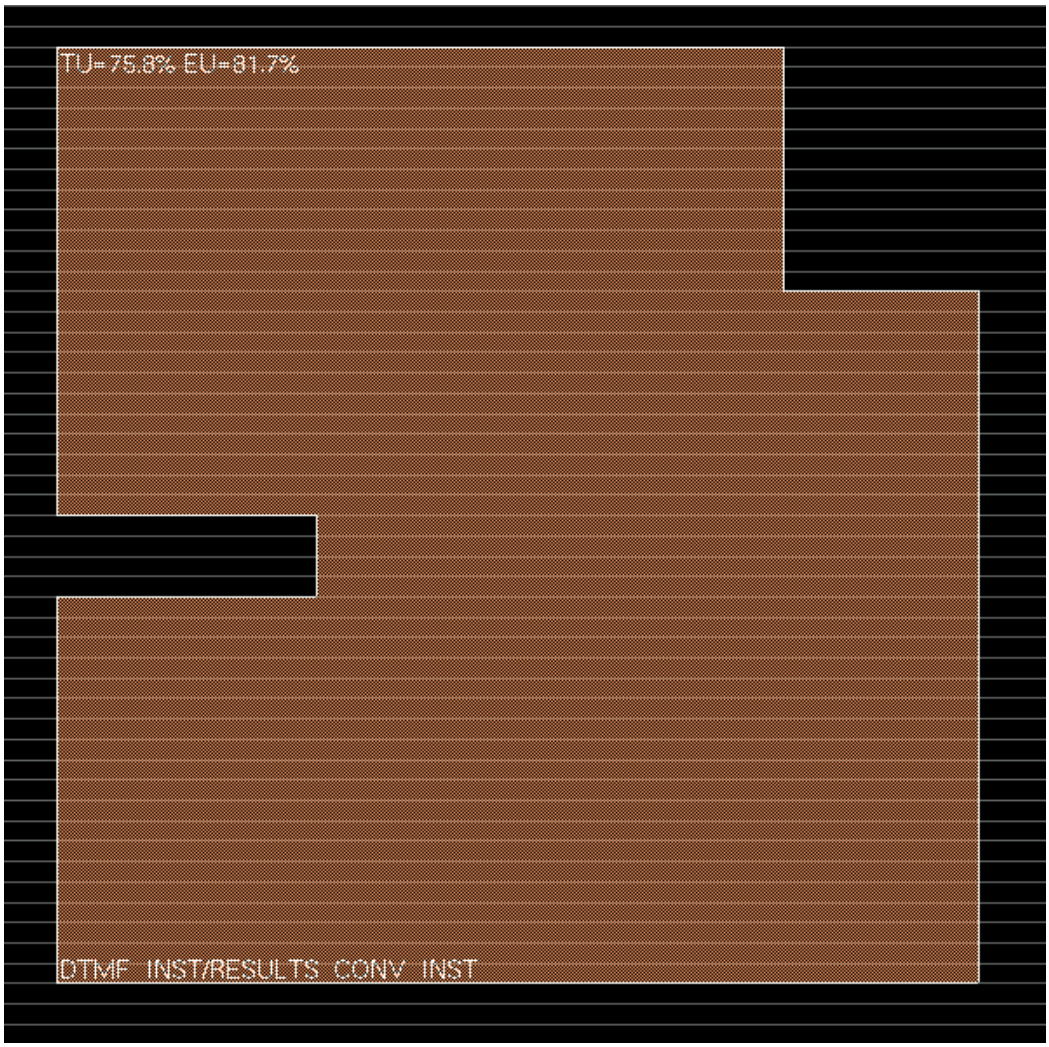
Moving objects – Under the Tools (left side of the Encounter form), click (LMB) on the *Move/Resize/Reshape* widget so you can start moving the module guide into the core area. Moving is done by clicking (LMB) on the module guide, dragging, and then dropping. You use the *Move/Resize/Reshape* widget to reshape a module guide, say to a rectangular shape. To reshape a module guide and to keep the area constant, hold down the `Shift-` key + (LMB) while reshaping. Also, use the *Move/Resize/Reshape* widget to move a block into the core area.

> **Moving multiple objects information** – When moving multiple floorplan objects, the `Shift`-key is used. First, hold-down the `Shift-`key to make multiple selections of objects, second, click the *Move/Resize/Reshape* widget, and third, hold-down the `Shift`-key while moving the group of objects with the (LMB).

Designing a rectilinear module, fence, or region – Move one of the submodules into the core area. To create a corner cut, place the cursor at the corner of the submodule so the cursor changes to a L-shape. Now, hold down the `Ctrl`-key plus click (LMB) and drag the corner. To create a slot cut, move the cursor to an edge so the cursor changes to a bar. Now, do the `Ctrl`-key plus click (LMB).

To change the submodule to a fence, change the cursor selection to Select (arrow widget) and double click the submodule to display the Attribute Editor form. Now use the *Constraint Type* button to the change Guide to Fence. After clicking the OK button, the color of the submodule changed from pink to orange. See fence example in Figure 4.

Figure 4 – Rectilinear Fence Example



TU and EU values information – The TU (Target Utilization) value represents the physical design size (area of the module, fence, or region) and is a rough estimation, since only the module's child standard cells and blocks are calculated. The use of the TU value is to judge the area size while resizing or reshaping a module. The initial TU value is calculated during design import. Resizing or reshaping a module changes the TU value. This new calculated value is displayed immediately.

The EU (Effective Utilization) value represents placement utilization for the all standard cells and blocks plus all floorplan objects, such as placement blockage, routing blockage, density screen, and partition objects. EU values also includes non-child standard cells and blocks preplaced inside a fence or region. To display the EU value for a fence or region, you must click the Display/Calculate Effective Utilization % button in the Toolbar. The EU value calculation and display is done on-demand, since this calculation is time consuming for very large designs. After designing your fences and regions, it is very important to update the EU values on the fences and regions before running Amoeba Placement. The EU value must never be greater than 100%, since greater than 100% means the fence or region is physically too small and the design cannot fit.

Creating floorplan objects – Use the widgets to create floorplan objects such as Placement Blockages, Density Screens, and Route Blockages. After creating the objects, double click on several of these created objects to view their properties or use the q-key after highlighting the object. This form allows you to change their properties and save the property changes. For example, once a Density Screen object is created, open the *Attribute Editor* form to change the Area Density default value of 50% to another value.

Clearing floorplan objects - Floorplan objects can be removed from the core area by using the *Clear Floorplan* form and this form has several clearing categories and options.

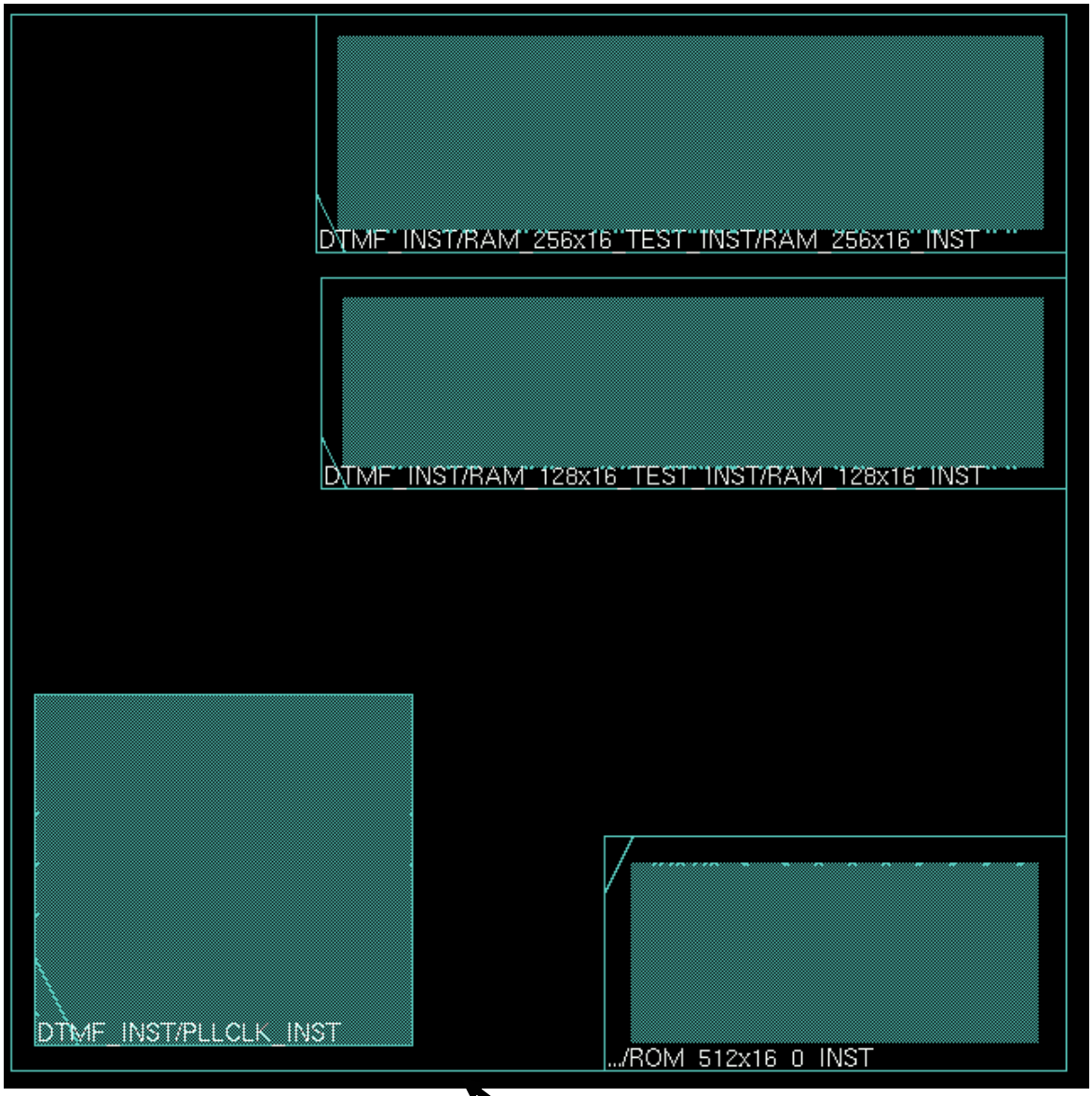
Form – *Floorplan -> Clear Floorplan*

Make your selection and

Click OK or Apply when ready.

Creating a floorplan with Relative Floorplan – Designing a floorplan by accurately moving blocks into the core area is important. Accurate preplacing of instances can be done with the Relative Floorplan form, and this form allows placing an instance inside the core area, inside a module, or relative to another preplaced instance. For this exercise will place the 4 blocks as in Figure 5 - Sample Floorplan.

Figure 5 - Sample Floorplan



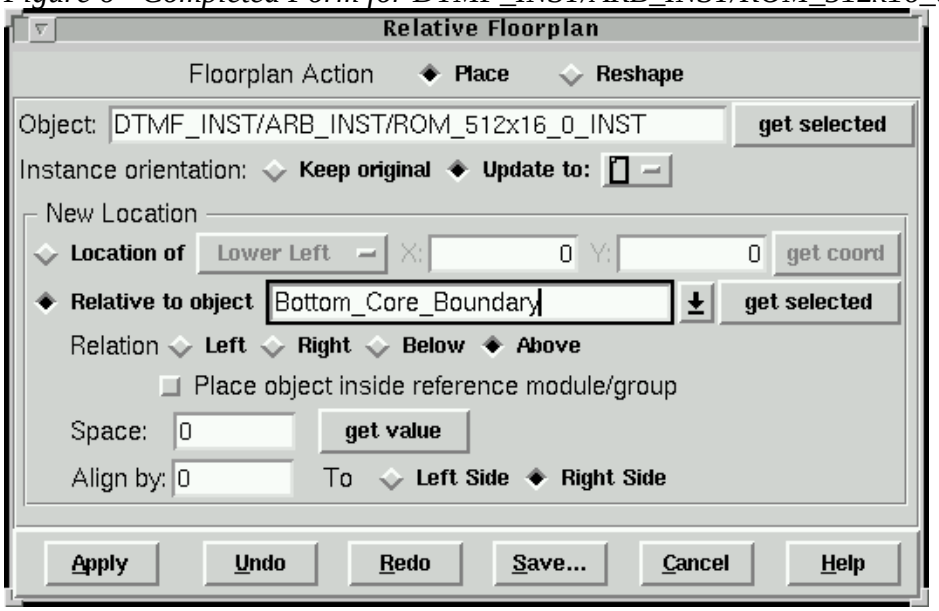
Make the following entries: Core Box

Form - *Floorplan -> Relative Floorplan*

Follow instructions below:
Place the 1st block, DTMF_INST/ARB_INST/ROM_512x16_0_INST, instance in the bottom-right location of the core area, as in Figure 3, and an added requirement is to orientate the block so that the pins face towards the center of the die. Try completing the form, and if the placement is not satisfactory, use the Undo and try again. Also, make use of the get selected and down-arrow stepper buttons. Or see Figure 6 for an example.

Click Apply when ready.

Figure 6 - Completed Form for DTMF_INST/ARB_INST/ROM_512x16_0_INST Block



The setting for placing the 3 remaining blocks are below (Figures 7 through 9).

Figure 7 - Completed Form for DTMF_INST/RAM_256x16_TEST_INST/RAM_256x16_INST Block

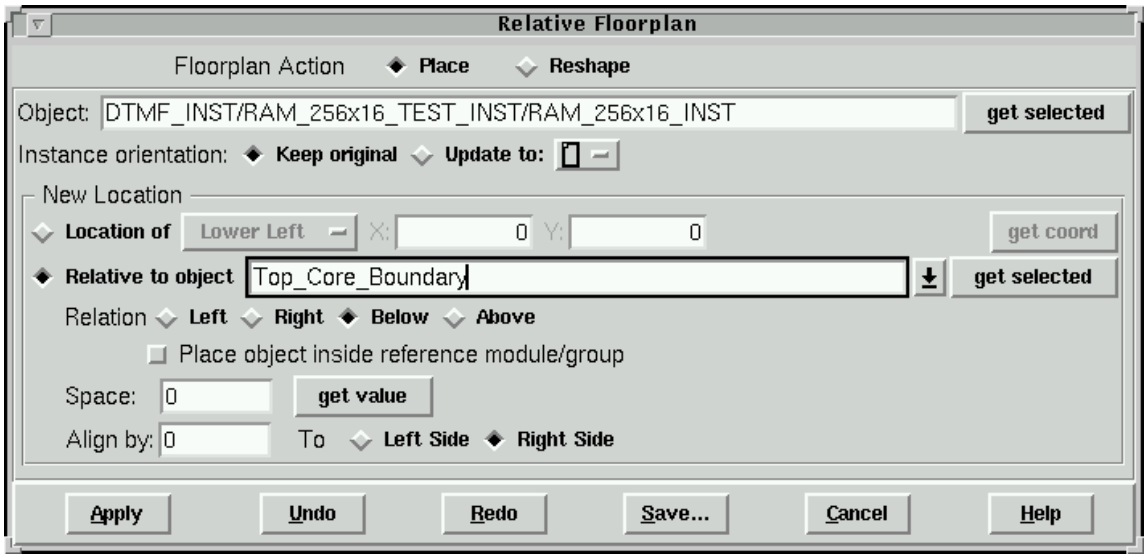


Figure 8 - Completed Form for DTMF_INST/RAM_128x16_TEST_INST/RAM_128x16_INST Block

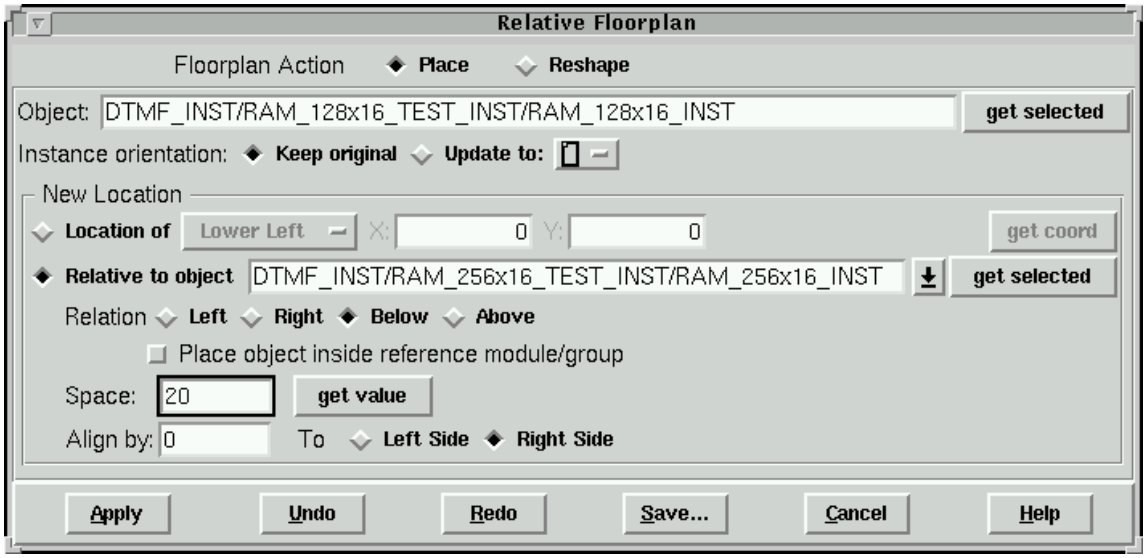
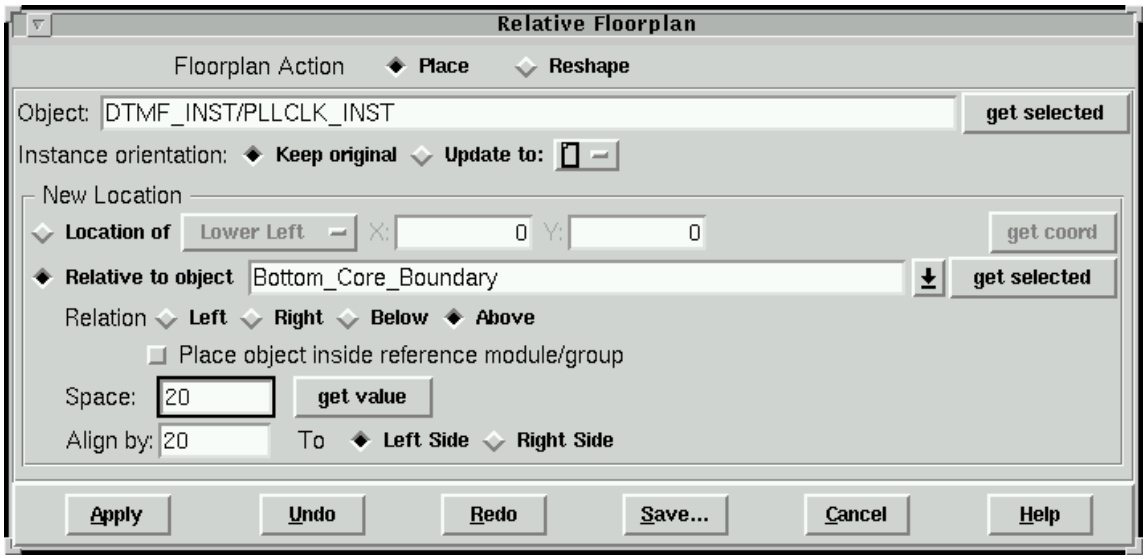


Figure 9 - Completed Form for DTMF_INST/PLLCLK_INST Block



Loading a floorplan file information: If you can not preplace the 4 blocks as in the sample floorplan, you can load the floorplan file, `dtmf.sample.fp` by using the *Design -> Load -> Floorplan* form.

Creating block halos – Once you have all the blocks preplaced, block halo can be created for each block by using the *Edit Block Halo* form. A block halo prevents (placement blockage) the placement program from placing standard cells in the halo area and away from the block.

To add placement blockage around the 4 blocks, first, select the 4 blocks by holding down the `Shift`-key and click (LMB) on each block. Second, make the following entries:

Form – *Floorplan -> Edit Block Halos*

Enter – Top: `20`
Enter – Bottom: `20`
Enter – Left: `20`
Enter – Right: `20`

Since 3 of the blocks have power/ground pin rings, be sure to:

Select – ♦ From Instance Block option.

Click OK when ready.

Note that created block halos can also be removed by using this form.

Viewing Block Information – There are 3 things to note. 1) Selecting a block while preplaced in the core area will display the connectivity flylines directly to the pins of the block. This display feature allows one to determine if the block is orientated properly. 2) The created block halo is a property of the block and if the block is moved, the block halo will follow. 3) The 3 rectangular blocks have power pins in a form of a ring. The power pins/rings are displayed by turning-on the *Pin* visibility buttons. This is done by 1st clicking the Slider underneath the All Color button, which displays addition visibility selections. Click the *Inst Pin* visibility button and now, the power rings display.

Creating power/ground rings – Before designing any power and ground rings or stripes, we must assign the global nets of power and ground, and this is done with the *Global Net Connections* form. There are 6 sets of entries required and they are shown in the table below.

Form – *Floorplan -> Global Net Connections*

For Set 1:
Enter – Set 1 from table (follow Figure 10).
Click the Add to List button.

Continue for Sets 2 through 6 and when done, the completed form looks like Figure 11.

Click Apply when all 6 sets appear in the Connection List.

Entry	Set 1	Set 2	Set 3	Set 4	Set 5	Set 6
Pins	VDD	n/s	vdd!	VSS	n/s	gnd!
In Instance	*	*	*	*	*	*
Tie High	n/s	Selected	n/s	n/s	n/s	n/s
Tie Low	n/s	n/s	n/s	n/s	Selected	n/s
Apply All	Selected	Selected	Selected	Selected	Selected	Selected
To Global Net	VDD	VDD	VDD	VSS	VSS	VSS

n/s = not selected.

Figure 10 - Completed Global Net Connections form for Set 1

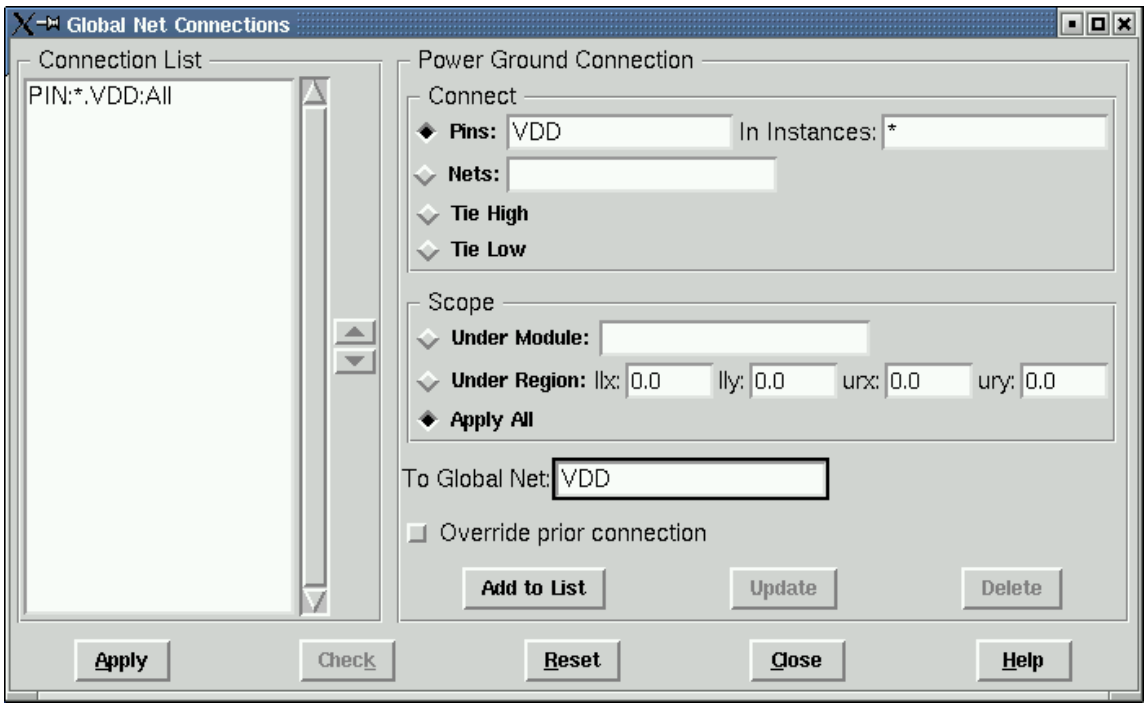
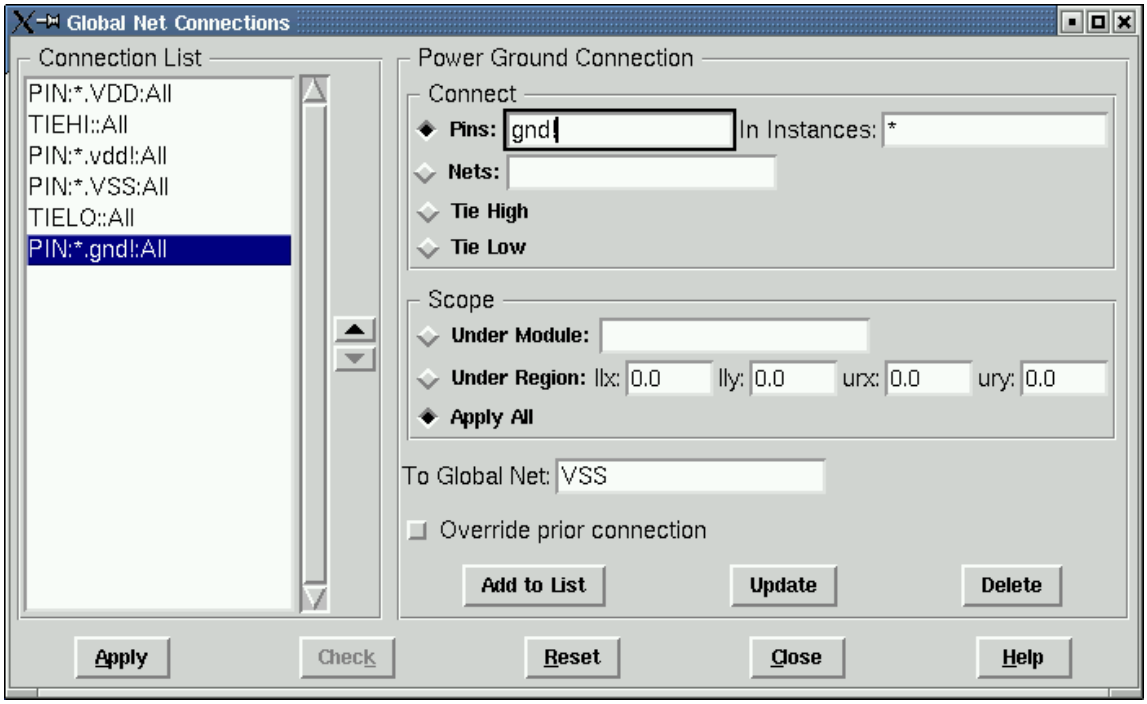


Figure 11 - Completed Global Net Connections form for the 6 Sets



After applying the 6 sets, click Check. The only warnings are for the power/ground pins of all the IO pad instances which are not connect to global special net. These warnings can be ignored for this workshop.

Viewing Block Information – Notice that once you have completed the Global Net Connections form, the power and ground rings display their VDD and VSS net names in the 3 rectangular blocks.

Now we are ready to create power and ground rings around the core area and around one of the blocks. Power and ground ring are added the core area and blocks by using the *Add Rings* form. Make the following entries:

Form - *Floorplan -> Power Planning -> Add Rings*

Make sure the *Ring Type* section defaults are:

Select – ♦ Core ring(s) contouring option
Select – ♦ Around core boundary option

Change the Ring Configuration section to:

Change – Top: Metal5
Change – Bottom: Metal5
Change – Left: Metal6
Change – Right: Metal6
Enter – Top/Bottom/Left/Right Width: 8
Enter – Top/Bottom/Left/Right Spacing: 1
Select – ♦ Center in channel option.

Leave the remaining defaults.

Click Apply when ready.

Zoom-in to a corner of the rings to see the vias. A created power/ground ring can be removed by using the *Undo* widget in the Toolbar.

Now, to add the power and ground ring around a block, use the same Add Rings form. First, click (LMB) on the DTMF_INST/PLLCLK_INST block that is in the core area to add power/ground rings. Second, change the form entries from the above work to:

Form – *Floorplan -> Power Planning -> Add Rings*

Change the *Ring Type* section to:

Select – ♦ Block ring(s) around option
Select – ♦ Each selected block and/or group of core rows option

Change the *Ring Configuration* section to:

Select – ♦ Specify option
Enter – Offset Top/Bottom/Left/Right: 1

Click Apply or OK when ready.

Now you should see to power and ground rings around the DTMF_INST/PLLCLK_INST block.

> **Creating Multiple Rings Information** – Multiple power and ground rings can be created around the core area or around block. The default power and ground net names (VSS and VDD) are extracted from the Design Import (Power page) form. To create multiple power and ground ring, enter the net names in the Net(s) entry box and in the order you want. Note that VSS is the inside ring.

Creating power/ground strips – To create power and ground stripes, use the *Add Stripes* form. Now, we will create vertical power and ground stripes. Make the following entries:

Form – *Floorplan -> Power Planning -> Add Stripes*

Make the changes in the Set Configuration section:

Change – Layer: Metal6
Select – Direction: ♦ Vertical option
Enter – Width: 8
Enter – Spacing: 1

Leave the default Set Pattern section at:

Select – ♦ Set-to-set distance: 100

Change the Stripe Offset boundary section to:

Select – ♦ Relative from core or area option
Enter – X from left: 100
Enter – X from right: 100
Leave the remaining default settings.

Click the *Advanced* tab and in the Ring and Block Handling section, change selections to:

Select – ■ Break stripes at block rings option
Select – ■ Break stripes that overlap same direction ring pins on different nets option
Use the remaining defaults.

Click Apply when ready.

The vertical power and ground stripes are created and connected. You may have to click the *Redraw* button in the Toolbar to see the added stripes.

Creating Multiple Stripes Information – Multiple power and ground stripes can be created in the core area. The default power and ground net names (VSS and VDD) are extracted from the Design Import (Power page) form. To create multiple power and ground stripes, enter the net names in the Net(s) entry box and in the order you want. Note that VSS is the left most stripe.

Routing the power/ground structures – To route the remaining power and ground structure, use the *SRoute* form. The SRoute program routes the block pins, pad pins, pad rings, standard cell pins, and unconnected stripes. For our exercise, we will be routing block pins, pad pins, and standard cell pins. Make the following entries:

Form – *Route -> SRoute*

In the Basic page, make the changes in the Route section to:

Unselect – ■ Pad rings option and
Use the remaining defaults in the Basic page.

Click the *Advanced* tab and then click *Extension control* from the list. Make 2 selection changes as follows:

In the Primary Connection for: and under Standard Cell Pins and stripe section, change selection to:

Select – None ♦ option

In the Secondary Connection/Stripe (Standard Cell Pins Only) (if the primary connection fails) section, change selection to:

Select – Last cell in the row ♦ option

Click OK when ready.

Now the power and ground rings around the core area are connected to the power and ground pads, block pins are connected, power rings are all connected, and standard cell follow pins are connected.

Verifying connectivity and geometry – After designing the power and ground for the design, the connections and geometries can be verified (DRC). These 2 tools are in the Verify menu. To verify the power and ground connectivity, make the following entries:

Form – *Verify -> Verify Connectivity*

Change selection to:

Select – ♦ Special only option

Click OK when ready.

There are violations markers because of antenna warnings and these warning can be ignored since these are power and ground.

Identifying violation marker information – There are 2 ways to identify violation markers: 1) Click the Q button at the bottom in the Encounter window which enables auto query of objects. Moving the cursor exactly on top of a violation marker displays the violation type in the bottom selected object text box. You may have to zoom-in very closely to have the violation type displayed. 2) Open the *Verify -> Violation Browser* to display the violations.

The violation markers are cleared using *Verify -> Clear Violation* menu item.

To verify the geometries, use the *Verify Geometry* form and make the following entries:

Form – *Verify -> Verify Geometry*

Use the form defaults which does not check for antenna geometries.

Click OK when ready.

Clear the DRC markers if any.

Editing wires - You can also interactively create or edit stripes by using the *Route -> Edit Route* form. To use this form, you must first enter the power/ground net names, such as `VDD` and `VSS`, and click on the *Route* tab to change the metal layers and enter the route width and spacing. Click the *Pencil* button (in *Tools* area) to start drawing the power/ground routes. The `Esc`-key ends the drawing of a route. The `Delete`-key removes the last route segment drawn.

Routes can be moved by selecting the segment, and then selecting the *Move Wires* button in the *Tools* Area. The moving of the selected segment is done by 2 mouse clicks. The first click marks the start distance point and second click mark the end distance point. The selected segment moved after the second click.

Pre-placing a standard cell - Now, a standard cell is pre-placed by using the Design Browser. First, open the Design Browser and make the following entries:

Form – *Tools -> Design Browser*

Enter – Instance: `DTMF_INST/DIGIT_REG_INST/digit_out_reg_3` followed by a <CR>. It is a standard cell of cell type SDFFSHQX1.

Now to pre-place this standard cell, it takes 4 steps.

1) **Click** the *Attribute Editor* button (text page with an arrow) to display the form for the instance.
2) **Click** the *Mouse* button in the Attribute Editor form and note the cursor has changed to cross hair when pointed in the core area.
3) **Click** the location in the core area where the standard cell is to be pre-place and this will fetch the coordinates.
4) **Change** – Status from Unplaced to Fixed in the Attribute Editor form.

Click OK when ready.

Now, you can see the pre-placed standard cell Double click the standard cell in the Physical view to display the connection flylines. The Fixed status means the Amoeba Placement or any other program cannot move the instance.

Before continuing, remove the standard cell by 1st double clicking the instance in the Physical view, and 2nd change the Status to Unplaced in the Attribute Editor form. Click OK when ready, and the standard cell instance is unplaced.

6. Running Placement

Supplied floorplan – This is optional. You can use your designed floorplan but as an option there is a workshop supplied floorplan file. To use your floorplan, skip following step.

Loading the floorplan file – Use the *Load Floorplan* file form and make the following entries:

Form – *Design -> Load -> Floorplan*

Select file – `dtmf.fp` and

Click Open after selecting the file.

Now you see the loaded floorplan which is a result of work in the Learning Floorplanning section.

Second, open the *Placement Blockage* form to specify that no standard cell will be placed under power and ground stripes. This is to avoid routing congestion that may occur under the power and ground stripes.

Form – *Place -> Specify -> Placement Blockage*

Select – ■ M2
Select – ■ M3
Select – ■ M4
Select – ■ M5
Select – ■ M6 options and

Click OK when ready.

Running Amoeba Placement – Use the *Place* form to run placement program and make the following entries:

Form – *Place -> Place*

Select – ♦ Medium Effort option
Select – ■ Ignore Scan Connection option.

Click OK when ready.

Note that scan information have not been loaded.

> **Scan handling information** – The Ignore Scan Connection option ignores all scan pin connections while running placement. There are 2 scan groups in the design. The scan pins for the scan cells are read from the timing library during design import.

Viewing the design after Placement – Once the placement program is done, you can view the placed design in the Amoeba and Physical views. Note the placed standard cells in the Physical view.

Generating a floorplan guide – Since placement is run, the submodule guides can be generated and displayed by using the *Generate Floorplan Guide* form.

First select the top-level module (DTMF_INST) and enter the u-key to ungroup. You will see several submodule guides. Now, make the following entries:

Form *– Floorplan -> Generate FP Guide*

Use the defaults and

Click Apply when ready.

Now, you are going to view how the placement program placed the submodule guides that were not pre-placed during floorplanning. Now select one of the submodules and switch to the Amoeba and Physical views to observer all the child instances. All standard cell instances and blocks that are highlighted belong to selected submodule.

If you want to view submodules that contain less than 100 instances, use the *Preference* form.

Form – *Design -> Preferences*

Click the *Display* tab and

Enter – Min. Floorplan Module Size: 25

Click OK when ready.

In the *Generate Floorplan Guide* form, click Apply. Now smaller size submodule guides are displayed, such as ARB_INST. You may have to click the *Redraw* button in the Toolbar to refresh the display.

Loading scan chain information and reordering the scan chain - Scan chain information is loaded by using the *Load Scan File* form. Make the following entries:

Form – *Design -> Load -> Scan*

Select file – `dtmf.scan.tcl` and

Click Open after selecting the file.

Scan chain checking information – When a scan information file is loaded, each scan chain is checked by tracing the chain from start to end and any scan edge that can not be reordered are marked fixed. Note that scan group2 has 16 edges that marked as fixed, and this means that these edges are not reordered. Scan chain information can be load in 2 formats, Encounter Tcl format and DEF format.

View the 2 scan chains before reordering them. This is done by the *Display Scan Connections* form:

Form – *Place -> Display -> Display Scan*

Click OK when ready.

Note the scan connection flylines.

Next, scan chains are reordered (optimized) by using the *Reorder Scan* form. Make the following entries:

Form – *Place -> Reorder Scan*

Select – ♦ Skip two pin cell option and

Click OK when ready.

Again, use the *Display Scan Chain* form again to view the optimized scan connections. When done viewing, use the *Place -> Display -> Clear Scan Display* menu item to clear the core area.

Scan reorder information – The Skip two-pin cell option is used because scan group1 has inverters in the chain. The newly reordered scan chain information can be dumped out in DEF format by using the Design -> Save -> DEF form.

7. Running Trial Route

Running Trial Route – We need to route the remaining nets of the design and Trial Route is used. Trial Route is a combination of global routing and track assignment and correlates well to detail routers. In this workshop, Trial Route is run twice. The first run will demonstrate route congestion by limiting the number of metal routing layers to 3 instead of 6 layers. The second run will use all 6 metal layers to complete the prototyping of the design. Make the following entries:

Form – *Route -> Trial Route*

Change – Max: Route Layer to 3

Click OK when ready.

Or you can type the Encounter command, `trialRoute –maxRouteLayer 3`, in the Encounter console to run trial route.

Once trial route completes, there are two things to look for. First, a visual view of route congestion. This is done looking for the red color diamond shapes. If you can locate the red diamond markers, zoom-in to view the congestion markers. There are two sets of numbers. The first set (#-top/#-bottom) is for the vertical connection where #-top is the required routes and #-bottom is the available routes. The second set of numbers is for the horizontal connections. These diamond shaped congestion locators represent an average in the area.

Second, view the log file or the Encounter console for the congestion table produced by trial route. The label of the table is *Congestion distribution*:. Just before this table, look for the last line with label *Overflow*:. If both numbers in the (#% H) and (#% V) are less than 0.5%, then this design is good for any detail router. The less than 0.5% is good for three (3) layers of metal and less than 1.0% is usually good for five (5) or more layers of metal.

Now, run Trial Route with 6 metal routing layers.

Form – *Route -> Trial Route*

Change – Max: Route Layer to 6

Click OK when ready.

Or you can type the Encounter command, `trialRoute`, in the Encounter console to run trial route

Viewing the Design after Trial Route – You can see connection flylines in the *Floorplan view*, but in the *Amoeba view*, the routed interconnections can be displayed. This is done by double clicking a module or block (this also opens the Attribute Editor form). More interestingly, this double clicking can be used in the *Physical view*. The actual routed interconnect for specific nets can be viewed. You must zoom-in to see the connections or use the (RMB) to zoom-in. The Zoom-in tool is located in the Toolbar.

Finding and highlighting a net – To locate and highlight a net in the core area, the Design Browser is used. Make the following entries:

Form – *Tool -> Design Browser*

Enter – Find text box `DTMF_INST/TDSP_CORE_INST/MPY_32_INST/n_334`, followed by a <CR>.

After the net is displayed in the Design Browser,
Select the net by clicking *Clear Magnifier* button.

Click the *Black Rectangle Magnifier* button to zoom-in to the highlighted net.

To zoom-in and get a closer view of the net, use *Zoom In* widget in the Toolbar or use the (RMB).

Displaying path information – Note the paths end with either an X or an O. The X marks an input and O marks an output. The Xs and Os display better in the Floorplan view.

Displaying design objects in the Design Browser information – You can also select a net or instance in reverse with the Design Browser. First, highlight a net or an instance in the core area, and then in the Design Browser, click the *Get Selected* button (button with several rectangles), and now the name of the highlighted object is displayed.

Viewing Different Objects – Click All Colors to open the *Color Preference* form to see all the objects in Encounter. The color of each object can be changed, the display of these objects can be turned off or on, and the selectivity of objects can be changed.

Note the slider button directly under the All Colors button. Click on the slider button to toggle the display the most commonly used general objects and route objects. There are 2 forms that can be displayed.

8. Extracting RC Data and Generating Wire Load Models

Extracting RC Data – The lumped capacitance values for all the nets in the design are extracted by the Extract RC form. Since the design is still being prototype, the native Encounter RC extraction which is the default. The RC extraction mode can be changed by the *Specify Analysis Condition -> Specify RC Extraction Mode* form. While extracting RC data, note in the form the various simulation format files that can be generated. The files are written to your work directory.

Form – *Timing -> Extract RC*

Use the Default Mode.

Select simulation formats of interest and

Click OK when ready.

Extracting RC information – Extracting RC data is required to perform delay calculation, timing analysis and power analysis. In the case where you are not interested in generating any simulation files but need to extract RC, you have 2 choices. 1) Do not select any simulation file format including the Cap format and Click OK or enter the Encounter Command, `extractRC`, in the Encounter terminal.

Generating Wire Load Model - Wire load models can be generated at every level of the hierarchy and this is done by using the *Generate Wireload Model* form.

Form – *Timing -> Generate Wireload Model*

Select – ♦ Cell Based Wireload Model option or
Select – ♦ Instance Based Wireload Model option and

Click the OK when ready.

Several output files are generated.

Wireload Model file information – There are 6 wireload files created in your work directory. There are 2 data files: `DTMF_CHIP.wl.hier` and `DTMF_CHIP.wl.flat`. There are Design Compiler 2 load script files: `DTMF_CHIP.wl.hier.scr` and `DTMF_CHIP.wl.flat.scr`. There are 2 BuildGates and RTL Compiler load script files: `DTMF_INST.hier.sdc` and `DTMF_INST.flat.sdc`.

Calculating Delays – The delays are calculated for each wire (routes) and the delays include instance delay. To see what delay default is used for large nets, open the *Design -> Design Import's* Timing page. Make the following entries:

Form – *Timing -> Calculate Delay*

Select – ■ Ideal Clock option if clock tree synthesis was not run.

Click OK when ready.

The output file is in SDF format.

The Calculate Delay mode is defaulted to Encounter. This default mode can be change by the *Timing -> Specify Analysis Condition -> Specify Delay Calculation Mode* form.

9. Running Setup Timing Analysis

Setting Operating Conditions – The maximum (slow) and minimum (fast) timing libraries were loaded during design import and there are temperature, process, and voltage conditions that are modeled. Since we are analyzing for both setup timing and hold timing of the design, the slow and fast process conditions are selected by default. To view the default operating conditions, make the following entries:

Form – *Timing -> Specify Analysis Condition -> Specify Operating Condition/PVT*

Note the default selection for both the Max and Min tabs.

Click the OK button and view the Encounter console for the slow and fast operating conditions. These conditions are the process (P), temperature (T), voltage (V) values.

Running Setup Timing Analysis and Generating a Slack Report – Timing analysis can be run after extracting RC. The result of running setup timing analysis is a timing graph from which several kinds of timing reports are generated (i.e., slack report and detail timing report). The timing analysis is run for setup timing. Since clock tree synthesis was not run, an ideal clock is used and the ideal clock transition delay value is 120 ps (from the Timing page of the Design Import form). Make the following entries:

Form – *Timing -> Timing Analysis*

Select – ♦ Setup Timing Analysis option which is default.

Use the remaining defaults and

Click OK when ready.

When timing analysis is done, the slack report is viewed by using the Slack Brower. Make the following entries:

Form – *Timing -> Timing Debug -> Slack Browser*

Select file – `DTMF_CHIP.slk`

Click Open when ready.

Note that there are a couple of paths that have negative slack value. Also, a detailed timing report file, `DTMF_CHIP.tarpt`, is generated and it lists all the instances in the path.

> **Explaining the slack report information** – Note in the slack report, the vclk1 and vclk2 cycle times (timeReq) are reported as 7.75 ns and 15.75 ns, respectively even though in the timing constraint file their periods are 8.0 ns and 16.0 ns, respectively. This 0.25 ns difference in the timeReq is because of the timing constraint, set_clock_uncertainty of 0.25 ns for both clocks.

To graphically highlight a path reported in the Slack Browser, do the following:

Make sure the Physical view is selected

Double-click on a path in the Slack Browser.

The path is highlighted.

10. Running IPO to Fix Setup Timing Violations

Once the setup violating paths are identified, in-place optimization (IPO) is run to fix the violating paths by buffer insertion, inverter insertion, instance resizing (including flip-flops), and instance cloning. Also, non timing critical instances are downsized. The IPO timing fix is for setup. In the case where there is no reported timing violation, IPO can be still run by specifying an aggressive target slack value. Make the following entries:

Form – *Timing -> In-Place Optimization*

In the Timing Analysis Type section:

Select – ♦ Setup option which is default.

In the Settings section:

Enter – Target Slack (ns): 0.5 (this is optional when no violating path is not reported)

Click Advanced option to view the default setting and

Click OK when ready.

The IPO will run through several iterations and when timing is met, the program will stop. Again, use the *Timing -> Timing Debug -> Slack* Browser to view the IPO slack report, `DTMF_CHIP_ipo/DTMF_CHIP_ipo.slk`.

An IPO message may be outputted due to timing design rule violations. There are fanout violations after IPO and most violations involve the clocks. IPO will not touch/fix the clocks. To see the fanout violations, type `reportFanoutViolation` in the Encounter console.

11. Running Clock Tree Synthesis (CTS)

Clock Tree Synthesis is run after fixing setup timing violations with IPO.

Loading the Clock Specification file - Clock Tree Synthesis is run with a clock specification file. Look at the file `dtmf.cts`. The clock specification file has several clock roots. In the *Specify Clock Tree* form, make the following entries:

Form – *Clock -> Specify Clock Tree*

Select file – `dtmf.cts` and

Click OK after selecting the file.

To run clock tree synthesis, use the *Synthesize Clock Tree* form, and make the following entries:

Form – *Clock -> Synthesis Clock Tree*

Use the default settings and

Click OK when ready.

To view the results of clock tree synthesis, use the *Display Clock Tree* form, and make the following entries:

Form – *Clock -> Display -> Display Clock Tree*

In the Route Selection section,
Select – ♦ Pre-Routes

In the Display Selection Section,
Select – ♦ Display Clock Tree option,
Select – ♦ All Levels option and

Click Apply when ready.

Next,

Select – ♦ Display Clock Phase Delay option and

Click OK when ready.

Note the multi-color clock instances, which represent the delay in the clock path. Several clock report file are generated and they are in the created DTMF_CHIP_cts/ directory. The ASCII text version is DTMF_CHIP_cts.ctsrpt.

Displaying CTS information – Note the color coding used to represent the delayed clock instances. To display a gated clock structure such as clock, DTMF_INST/TEST_CONTROL_INST/i_150/Y, the *All Level* option must be selected.

There is also a clock browser (*Clock -> Clock Tree Browser*) that can be used to display the schematic of the synthesized clock tree. You must 1st select one of the clocks and then click OK. Then the clock schematic displays.

To clear the display, use the *Clock -> Display -> Clear Clock Tree Display* menu item.

12. Running Hold Timing Analysis after Clock Tree Synthesis (CTS)

Before running hold time analysis, Trial Route and extract RC must be run. This can be done by typing 2 commands in the Encounter console:

```
trialRoute
extractRC
```

Running Hold Timing Analysis and Generating a Slack Report – At this point of the design, IPO was run to fix setup timing and then the clocks are synthesized. Now timing analysis is run check the hold timing with skew analysis. Make the following entries:

Form – *Timing -> Timing Analysis*

Select – ♦ Hold Time Analysis option.
Select – ♦ Skew Analysis option since the clock tree was synthesized.
Select – ♦ Clock Tree Exist option
Enter – Slack Report File: `DTMF_CHIP.hold.slk`
Enter – Detailed Violation Report File: `DTMF_CHIP.hold.tarpt`.
Use the remaining defaults and

Click OK when ready.

When hold timing analysis is done, the slack report is viewed by using the Slack Brower. The paths with negative slack value have hold time violations.

13. Running IPO to Fix Hold Timing Violations

IPO is run to fix the hold time violating paths by delay insertion. Make the following entries:

Form – *Timing -> In-Place Optimization*

In the Timing Analysis Type section:

Select – ♦ Hold option.

In the Settings and Report sections:

Enter – Target Slack (ns): 0 (only if the value was changed for set timing analysis).
Enter – Save to Directory: `DTMF_CHIP_ipo.hold`
Enter – Base Name: `DTMF_CHIP_ipo.hold`

Click OK when ready.

All hold time violations should be fixed. Use the *Timing -> Timing Debug -> Slack* Browser to view the IPO slack report, `DTMF_CHIP_ipo.hold/DTMF_CHIP_ipo.hold.slk`.

At this point in the prototyping, the design has met setup and hold timing constraints. Timing is really not closed on a design unless crosstalk is prevented and then analyzed. We will do this exercise next.

14. Saving Your Design Work

Saving the Design - It is a good idea to save the design work as you progress and the most notable steps are after floorplanning, running placement, running route. It is best to use the *Save Design* form but the Menu allows saving to an individual file. For an example, the *Design -> Save -> Route* allows saving the route data to a file. To save the design, make the following entries:

Form – *Design -> Save Design*

Enter your own archive file name or use the default.

Click the Save when ready.

Now you can restore your work in a future Encounter session.

15 Preventing Crosstalk

Timing is not closed on a design unless crosstalk is prevented, analyzed, and then fixed. Elimination of crosstalk problems after running IPO to fix setup and hold time will help to reduce number of crosstalk violations at the post route stage but also will help to converge on signal integrity (SI) closure. For global and detail routing, NanoRoute is used. When running NanoRoute, be sure to select the SI Driven option in the NanoRoute form. This option reduces coupling between adjacent wires during routing without sacrificing routability.

Running NanoRoute – Since the design prototyping has met timing using Trial Route, we will now use NanoRoute for global and detail routing. Make the following entries:

Form – *Route -> NanoRoute*

Select – ■ SI Driven option.

Use the remaining defaults.

Click OK when ready.

Running Crosstalk Analysis (discussion only) – The Encounter SI now uses CeltIC to perform crosstalk analysis, but CeltIC requires the cdB noise library file. Since this library is foundry supplied, there is no cdB library available in this tutorial at this time. The cdB library file is assigned in the Misc. page of the Design Import form. Also, the Encounter capacitance table must be available and the table is assigned in the Timing page of the Design Import form. The crosstalk analysis is run and switching windows are selected using the SI -> Run CeltIC Crosstalk Analysis form.

Fixing Crosstalk – Fixing crosstalk (and glitch noise) violations are fixed by driver resizing, buffer insertion, downsizing aggressor, or soft spacing routing, and the SI -> Fix Crosstalk form is used.

Displaying Noise – Displaying the victim nets with specific parameters is done using the SI -> Display Noise Net form. Once the Apply or OK button is pushed, this opens the CeltIC Result Browser form. To view a victim net in the design display area, double-click on one of the nets in the Browser list, and this action highlight the nets. Clicking the Browse Aggressor button in the CeltIC Result Browser will highlight the victim and aggressor nets.

Rerunning Timing Analysis – After fixing the crosstalk violations, timing analysis should be rerun. This is to verify the SI fixing does not change the critical paths.

Running Power Analysis Section

Power analysis can be run immediately after extracting RC or even after running IPO or at anytime in the design flow. The Power Analysis tool can be easily set up to run in Statistical mode. The clock rates and net toggle probabilities for the 2 clock domains are specified individually while running power analysis. Further, you can decide when to run power analysis, before or after running clock tree synthesis or before or after running IPO fixing setup or hold time. See Sections A through D below for the steps to run Power Analysis.

A. Preparing to Run Power Analysis for VDD

First, be sure the correct timing model is loaded before running power analysis. For this workshop, the design must be imported using the `dtmfLef.conf` file to set up the Design Import form. If you are currently in the running this workshop, power analysis can be run anytime after RC extraction has been completed.

Second, the power reference points must be created on the power rings around the core area. Make sure you are in the Physical view and then, open the *Power -> Edit Pad Location* form. Also, click on the Auto Query Q button at bottom of the Encounter window to help you locate the power and ground points.

To add VDD power reference points next to the VDD pads, this can be easily done by 1st, click the Get Coord button, 2nd , click on the location near the VDD pad, 3rd, select the metal layer, and then click the Add button. Now you should see a yellow colored circle representing the VDD reference point. Complete adding the 5 VDD pad reference points.

Or you can click the Load button to load the VDD pad file, `dtmf.vdd.pp`. This file works for Workshop 1. You should see the yellow colored circle pads in the Physical view.

B. Running Statistical Power Analysis

A more realistic power analysis for this design is to set a toggle value for nets in each clock domain and these clocks are defined in the timing constraint file. To run in this clock domain mode, the Edit Net Toggle Probability and Power Analysis Statistical Mode must be completed.

First, open the *Power -> Edit Net Toggle Probability* form and click the Get Clock button and note that 2 clocks appear. Select one clock at a time and add the net toggle probability. This is done by clicking the Edit button, entering `0.2` (20%) in the Net Toggle Probability box, and finish by clicking the Add/Replace button. When done editing both clocks, save your entries to a file.

Or, you can click the Load button and load the file `dtmf.tg` to complete the Edit Net Toggle Probability form.

Second, open the *Power -> Power Analysis -> Statistical* form. Enter `VDD` in the Net Names box. Select either Pre-CTS Clock or Post-CTS Clock depending on whether clock tree synthesis was run. Enter or select the Net Toggle Probability file `dtmf.tg`. No file entry is needed for Instance Power Data. In the Rail Analysis section, enter or select `dtmf.vdd.pp` in the Pad Location Files box and select *Layout* and *Average* since we have power / ground strips and have run SRoute. Last, enter a Report File name before clicking OK button. Now power analysis will run.

C. Viewing Power Analysis Results

First, view your power report file or view the Encounter console messages to see the power supply value, average power dissipation, worst IR drop, and worst EM violation in the design.

Second, to display the IR drop, open the *Power -> Display -> Display Rail Analysis Results* form. Enter `VDD` for the Net Name and select IRD (V) option. Enter an IRD Threshold value at 10 per cent (`0.01`) of the power supply, click the Update filter range button, and then click the Apply button. Now, the color coded IR drop displays. To get a more detail and colorful display of the IR drop, change the IRD (V) Threshold value to `0.005` and click the Update filter range button. This threshold is closer to reported worst IR drop value. For a better view of the power rails, deselect the Net, and Instance visibility in the color display area (right side of the Encounter form). To clear the IR drop display, use the *Power -> Display -> Clear Rail Analysis Display* menu item.

Besides the power report file, power analysis creates the file `instance.power`. This file contains the power dissipation (mWatts) for all instances in the design, and this file is used to customize the instance power by superseding the power from the timing library. You can use Rail Analysis with the `instance.power` file to run subsequent power analysis, the analysis runs fast since all the instances' power is read from this file.

Third, to display the Macro Current Source location, open the *Power* -> Display -> *Display Macro I Source Location* form. Enter `VDD` for the Net Name and click OK. Now the white colored circle shaped current sources for the blocks are displayed. These sources represent the current source points at the power pins (VDD) of the blocks.